Texas Instruments

SRC4194EVM

Evaluation Module

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the absolute operating conditions shown in Table 2−1.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +70°C. The EVM is designed to operate properly with certain components above +70°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This document contains the information required to setup and operate the SRC4194EVM evaluation module. For a more detailed description of the SRC4194, please refer to the product datasheet available from the Texas Instruments web site at http://www.ti.com. Additional support documents are listed in the sections of this guide entitled ***Related Documentation from Texas Instruments*** and ***Additional Documentation***.

How to Use This Manual

Throughout this document, the term **EVM** and the phrase **evaluation module** are synonymous with the SRC4194EVM.

Chapter 1 provides a product overview for the SRC4194 four-channel asynchronous sample rate converter. The SRC4194EVM block diagram and primary features are also discussed.

Chapter 2 provides general information regarding EVM handling and unpacking, as well as absolute operating conditions for power supplies and input/output connections.

Chapter 3 provides general hardware descriptions and configuration information for the EVM. The information in this chapter is designed to guide the user in the setup of the EVM.

Chapter 4 includes the EVM electrical schematic, printed circuit board (PCB) layout, and the bill of materials

Information About Cautions

This document contains cautions. The information in a caution is provided for your protection. Please read each caution carefully.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instrument integrated circuits used in the assembly of the SRC4194EVM. These documents are available from the TI web site at http://www.ti.com. The last character of the literature number corresponds to the document revision, which is current at the time of the writing of this User's Guide. Newer revisions may be available from the TI web site, or by calling the Texas Instruments Literature Response Center at (800) 477−8924 or the Product Information Center at (972) 644−5580. When ordering, identify the document(s) by both title and literature number.

Data Sheets:	Literature Number:
SRC4194	SBFS025A
DIT4192	SBOS229B
PLL1705	SLES046A
REG1117	SBVS001B
SN74ALVC125	SCES110E
SN74ALVC244	SCES188B
SN74ALVC245	SCES271B
SN74LVC1G04	SCES214M
SN74LVC1G08	SCES217L
SN74LVC244A	SCAS414U

Additional Documentation

The following documents or references provide information regarding selected non-TI components used in the assembly of the SRC4194EVM. These documents are available from the corresponding manufacturer.

Document:	Manufacturer:
CS8414 Data Sheet	Cirrus Logic, web site: http://www.cirrus.com
HCM49 Series Crystals	Citizen, web site: http://www.citizencrystals.com

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644−5580 or visit the TI Semiconductor Online Technical Support pages at http://www.ti.com.

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Chapter 1

Introduction

This chapter provides a brief technical overview for the SRC4194 four-channel audio asynchronous sample rate converter, as well as a general description and feature list for the SRC4194EVM.

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1.1 SRC4194 Product Overview

The SRC4194 is a four-channel, asynchronous sample rate converter (ASRC), implemented as two stereo sections referred to as SRC A and SRC B. Operation at input and output sampling frequencies up to 212kHz is supported, with a continuous input/output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and THD+N are achieved by employing high performance, linear phase digital filtering with better than 140dB of image rejection. The digital filters provide settings for lower latency processing, including low group delay options for the interpolation filter and a direct down-sampling option for the decimation filter. Digital de-emphasis filtering is also included, supporting 32kHz, 44.1kHz, and 48kHz input sampling frequencies.

The audio input and output ports support standard audio data formats, as well as a time division multiplexed (TDM) format. Word lengths of 24, 20, 18, and 16 bits are supported. Input and output ports may operate in Slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port may operate in Master mode while the other remains in Slave mode. In Master mode, the LRCK and BCK clocks are derived from the reference clock inputs, either RCKIA or RCKIB. The flexible configuration options for the input and output ports allows connection to a variety of audio data converters, digital audio interface devices, and digital signal processors.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through compressed or encoded audio data, as well as non-audio data (that is, control or status information).

A soft mute function is available for the SRC4194 in both Hardware and Software modes. Digital output attenuation is available only in Software mode. Both soft mute and digital attenuation functions provide artifact-free operation. The mute attenuation is typically −144dB, while the digital attenuation function is programmable from 0dB to −127.5dB in 0.5dB steps.

The SRC4194 includes a four-wire SPI port, which is used to access on-chip control and status registers in Software mode. The SPI port facilitates interfacing to microprocessors or digital signal processors that support synchronous serial peripherals. In Hardware (or Standalone) mode, dedicated control pins are provided for the majority of the SRC4194 functions. These pins can be either hardwired or driven by logic or host control.

1.2 SRC4194 Functional Block Diagram

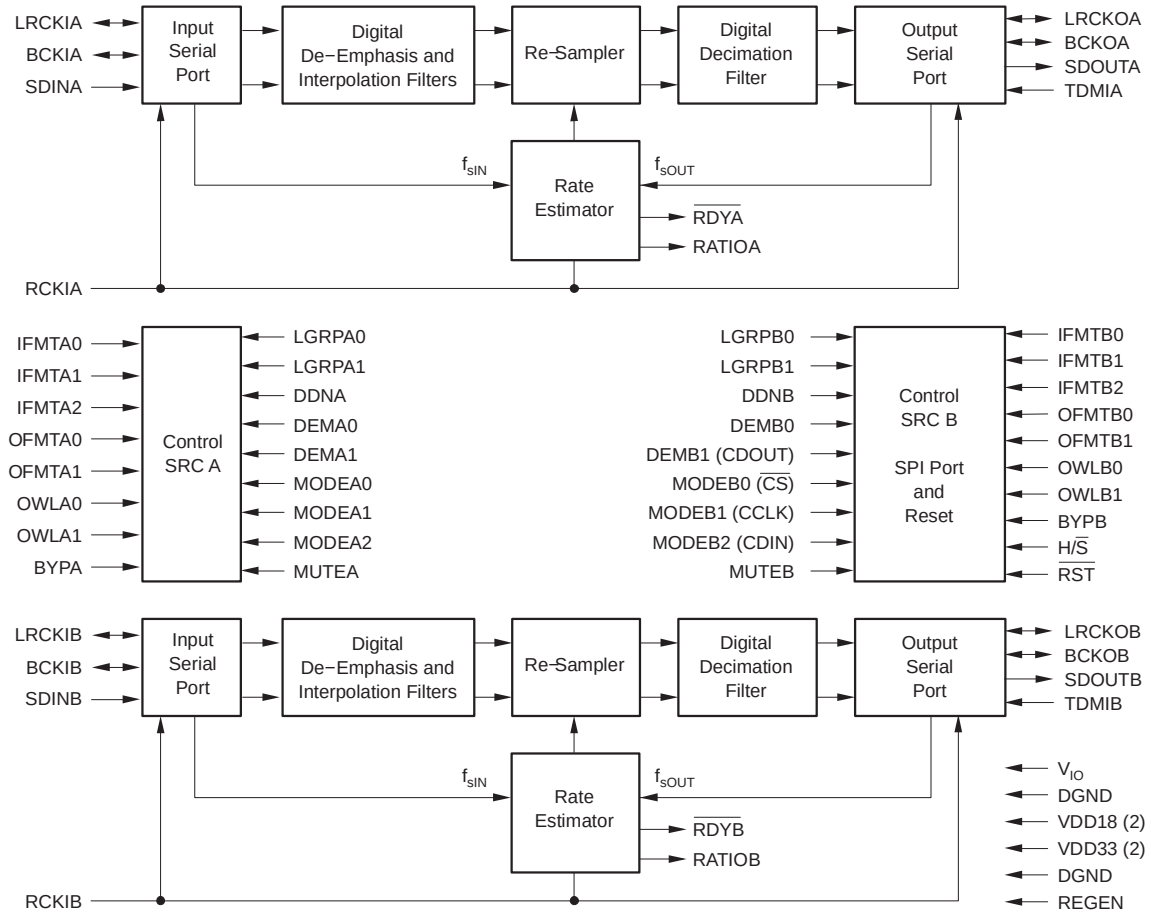
Figure 1−1 shows a functional block diagram of the SRC4194. The SRC4194 is segmented into two stereo SRC sections referred to as SRC A and SRC B. Each section can operate independently from the other. Each section has its own set of configuration pins in Hardware mode, and its own bank of control and status registers in Software mode.

SRC A and SRC B have identical operations. Audio data is received at the input serial port, clocked by either the audio source device in Slave mode, or by the SRC4194 in Master mode. The output port data is clocked by either the audio output device in Slave mode, or by the SRC4194 in Master mode. The input data is passed through interpolation filters that up-sample the data, which is then passed on to the re-sampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results of the rate estimation are used to configure the re-sampler coefficients and data pointers.

The output of the re-sampler is passed on to either the decimation filter or direct down-sampler function. The decimation filter performs down-sampling and antialias filtering functions, and is required when the output sampling frequency is equal to or lower than the input sampling frequency. The direct down-sampling function does not provide any filtering, and may be used in cases when the output sampling frequency is greater than the input sampling frequency. The advantage of the direct down-sampling function is a significant reduction in the group delay associated with the decimation function, allowing lower latency processing.

For additional information regarding the SRC4194, please refer to the product datasheet available from the TI web site, located at http://www.ti.com.

Figure 1−1. SRC4194 Functional Block Diagram



1.3 SRC4194EVM Features

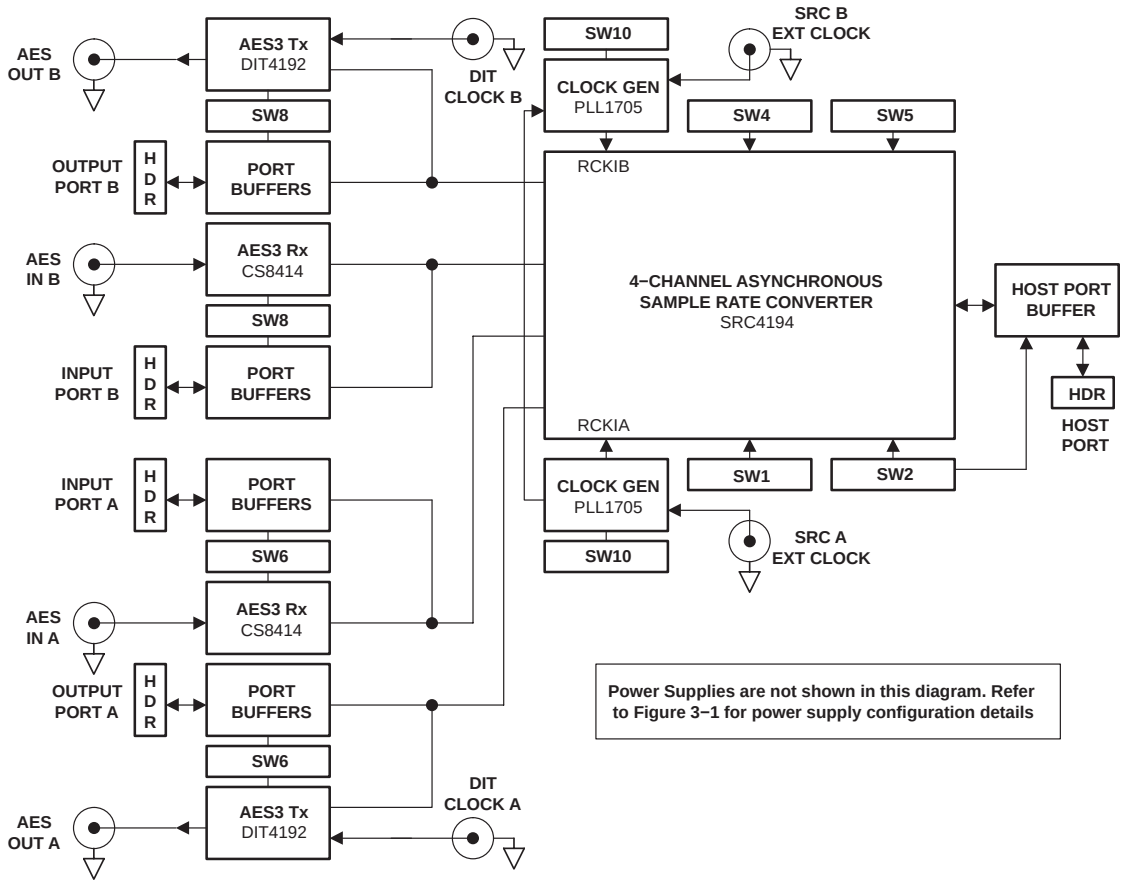
The SRC4194EVM provides a convenient platform for evaluating the performance and functionality of the SRC4194 product. Key EVM features include:

- ❑ Supports operation from a single +5V power supply
- ❑ Flexible power-supply configuration using either onboard voltage regulators or external supplies
- ❑ Buffered input and output serial ports support connection to external hardware and test systems
- ❑ Two 75Ω AES3 inputs with onboard receivers supporting input sampling rates up to 108kHz
- ❑ Two 75Ω AES3 outputs supporting sampling rates up to 192kHz
- ❑ Flexible SRC reference clock generation using onboard PLL circuitry or external clock sources
- ❑ Supports hardware mode operation using onboard switches
- ❑ Supports software mode operation using the buffered host port interface

1.4 SRC4194EVM Functional Block Diagram

The SRC4194EVM functional block diagram is shown in Figure 1−2. Besides the SRC4194, there are multiple audio input and output port interfaces, reference clock generation circuitry, switches for Hardware mode configuration and logic functions, and a buffered host port interface for communications with the SRC4194 SPI port when configured for Software mode operation. Chapter 3 provides operational and configuration details for the various hardware functions included on the EVM board.

Figure 1−2. SRC4194EVM Functional Block Diagram



Chapter 2

Getting Started

This chapter provides information regarding SRC4194EVM handling and unpacking, as well as absolute operating conditions.

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2.1 Electrostatic Discharge Warning

Failure to observe proper ESD handling precautions may result in damage to EVM components.

Many of the components on the SRC4194EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling procedures when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation. Failure to observe ESD handling procedures may result in damage to EVM components.

2.2 Unpacking the EVM

Upon opening the SRC4194EVM package, please check to make sure that the following items are included:

- ❑ One SRC4194EVM
- ❑ One printed copy of the SRC4194 data sheet
- ❑ One printed copy of the SRC4194EVM User's Guide

If any of these items are missing, please contact the Texas Instruments Product Information Center nearest you to inquire about replacements.

2.3 Absolute Maximum Operating Conditions

CAUTION

Exceeding the Absolute Operating Conditions may result in damage to the evaluation module and/or the equipment connected to it.

The user should be aware of the absolute operating conditions for the SRC4194EVM. Exceeding these conditions may result in damage to the EVM and possibly the equipment connected to it. Table 2−1 summarizes the critical data points.

Table 2−1. Absolute Operating Conditions

	MIN	MAX	UNIT
Power Supplies			
+5V	+4.5	+6.0	V
EXT +1.8V	+1.65	+2.0	V
EXT +3.3V	+3.0	+3.6	V
EXT VIO(1)	+1.65	+3.6	V
Input Port A and B, Output Port A and B, Host Port, SRC A and B EXT Clock, and DIT Clock A and B(1)			
V_{IH}		VIO + 0.3	V
V_{IL}	−0.3		V
AES IN A and B Ports			
V_{IH}		+7.0	V
V_{IL}	−0.5		V

(1) VIO may be set to +1.8V or +3.3V using onboard regulators, or +1.65V to +3.6V using an external power supply connected to the EXT VIO terminal located on connector J14.

Chapter 3

Hardware Description and Configuration

This chapter provides hardware description and configuration information for the SRC4194EVM.

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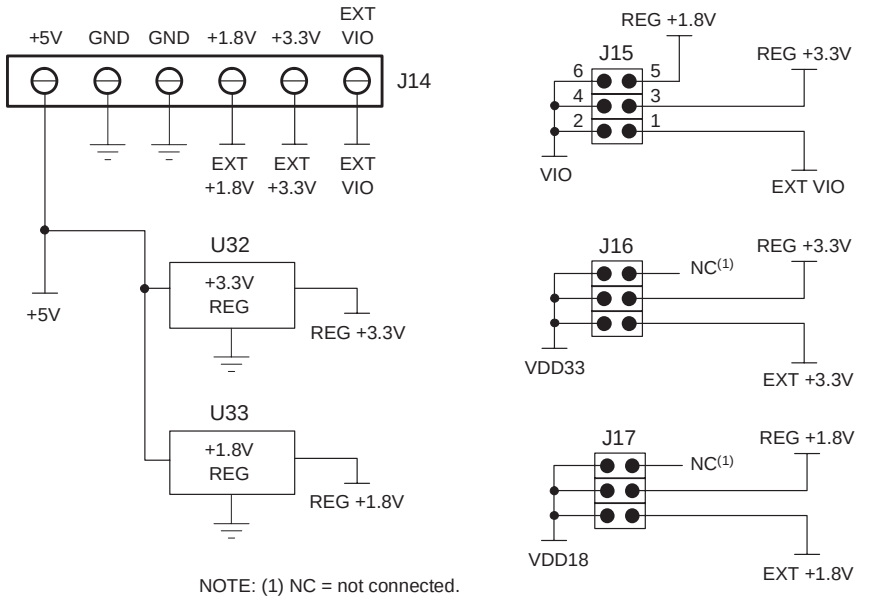
3.1 Power Supply Configuration

Changes to settings for jumpers J15 through J17, as well as changes to the state of the REGEN element of switch SW2, should be performed with all power supplies connected to terminal block J14 powered off, thereby avoiding potential damage to the EVM and external components.

The SRC4194EVM provides several options for power-supply configuration using onboard regulators and/or external supplies. Onboard jumpers and a switch are used to select the available options. Figure 3−1 illustrates the EVM power-supply configuration using jumpers J15 through J17 and terminal block J14. Table 3−1 summarizes the common jumper configurations based upon a setup using a +5V supply and an optional EXT VIO supply.

Figure 3−1. SRC4194EVM Power Supply Configuration and Jumpers



NOTE: (1) NC = not connected.

Referring to Figure 3−1, the SRC4194EVM includes two onboard linear voltage regulators, U32 and U33, which are used to derive +1.8V and +3.3V from a single +5V external power supply. The outputs of the two regulators may be connected to the onboard VDD18, VDD33, or VIO power busses using jumpers J15 through J17. The jumpers also allow for connection to external power supplies using terminal block J14.

Table 3−1 summarizes five common supply configurations for the SRC4194EVM. Jumper settings for J15 through J17 are indicated, as well as the state of the REGEN element of switch SW2. The user is reminded to power down all supplies connected to terminal block J14 of the EVM before changing the jumper and switch configurations.

Table 3−1. Common Configurations using a +5V Supply and an Optional EXT VIO Supply

Case	Description	J15	J16(1)	J17(1)	REGEN (SW2)
1	Core Voltage = +1.8V using onboard regulator (U33)	—	NC	REG + 1.8V	LO
	VIO = +1.8V using onboard regulator (U33)	REG + 1.8V			
2	Core Voltage = +1.8V using onboard regulator (U33)	—	NC	REG + 1.8V	LO
	VIO = +3.3V using onboard regulator (U32)	REG + 3.3V			
3	Core Voltage = +3.3V using onboard regulator (U32)	—	REG + 3.3V	NC	HI
	VIO = 3.3V using onboard regulator (U32)	REG + 3.3V			
4	Core Voltage = +1.8V using onboard regulator (U33)	—	NC	REG + 1.8V	LO
	VIO = +1.65V to 3.6V using EXT VIO supply	EXT VIO			
5	Core Voltage = +3.3V using onboard regulator (U32)	—	REG + 3.3V	NC	HI
	VIO = +1.65V to 3.6V using EXT VIO supply	EXT VIO			

1) NC = not connected.

3.2 SRC4194 Configuration Modes

The SRC4194 can be set to one of two configuration modes: Hardware (or Standalone) or Software (via a four-wire SPI port). The H/$\overline{S}$ element of switch SW2 is used to set the mode. Table 3−2 summarizes the H/$\overline{S}$ mode switch settings.

Table 3−2. Setting the Configuration Mode

H/$\overline{S}$ Switch Setting	SRC4194 Configuration Mode
LO	Software Mode
HI	Hardware (or Standalone) Mode

3.2.1 SRC4194 Hardware (or Standalone) Mode Configuration

In Hardware mode, switches SW1, SW2, SW4, and SW5 are used to set the dedicated control pins to either a low or high logic level. The switches correspond one-to-one with the pin names of the SRC4194 device. Table 3−3 summarizes the switch functions and available settings for each element of switch SW1, SW2, SW4, and SW5.

In addition to the switches already mentioned, a momentary pushbutton switch (SW3) is used for the SRC4194 reset function. The $\overline{RST}$ input (pin 21) of the SRC4194 is normally pulled high via an external 10kΩ resistor connected to the VIO supply bus. When the pushbutton is pressed, the switch shorts the $\overline{RST}$ pin to ground. Releasing the switch then causes the $\overline{RST}$ pin to be pulled high again. By momentarily pressing and then releasing SW3, the user can generate a reset pulse for the SRC4194.

Table 3−3. Hardware Mode Setup Matrix Using Switches SW1, SW2, SW4 and SW5 (x = A or B)

IFMTx0	IFMTx1	IFMTx2	OFMTx0	OFMTx1	OWLx0	OWLx1	BYPx	LRGPx0	LGRPx1	DDNx	DEMx0	DEMx1	MODEx0	MODEx1	MODEx2	MUTEx	Function/Description
																	Input Port Data Format
LO	LO	LO															24-bit Left Justified
HI	LO	LO															24-bit I^2S
LO	HI	LO															Unused
HI	HI	LO															Unused
LO	LO	HI															16-bit Right Justified
HI	LO	HI															18-bit Right Justified
LO	HI	HI															20-bit Right Justified
HI	HI	HI															24-bit Right Justified
																	Output Port Data Format
			LO	LO													Left Justified
			HI	LO													I^2S
			LO	HI													TDM
			HI	HI													Right Justified
																	Output Port Word Length
					LO	LO											24 bits
					HI	LO											20 bits
					LO	HI											18 bits
					HI	HI											16 bits
																	Bypass Mode
							LO										Disabled
							HI										Enabled
																	Interpolation Filter Group Delay
								LO	LO								Buffer 64 samples before resampling
								HI	LO								Buffer 32 samples before resampling
								LO	HI								Buffer 16 samples before resampling
								HI	HI								Buffer 8 samples before resampling
																	Decimation Mode
										LO							Decimation Filter Enabled
										HI							Direct Downsampling Enabled
																	De-Emphasis Filter Function
											LO	LO					Disabled
											HI	LO					Enabled for fs = 48kHz
											LO	HI					Enabled for fs = 44.1kHz
											HI	HI					Enabled for fs = 32kHz
																	Input & Output Serial Port Mode
													LO	LO	LO		Input and Output Ports are Slave
													HI	LO	LO		Output Port is Master w/ RCKI =128fs
													LO	HI	LO		Output Port is Master w/ RCKI =512fs
													HI	HI	LO		Output Port is Master w/ RCKI =256fs
													LO	LO	HI		Input and Output Ports are Slave
													HI	LO	HI		Input Port is Master w/ RCKI =128fs
													LO	HI	HI		Input Port is Master w/ RCKI =512fs
													HI	HI	HI		Input Port is Master w/ RCKI =256fs
																	Output Soft Mute
																LO	Disabled
																HI	Enabled

3.2.2 SRC4194 Software Mode Configuration Via The Host Port

In Software mode, the SRC4194 relies upon an external host device to program the internal control registers via the four-wire SPI port. The SPI port is accessed using the Host Port header, connector J1. The header is buffered by U2, an octal buffer IC with tri-state outputs. The buffer outputs are enabled only when the H/$\overline{S}$ element of switch SW2 is set to the LO state. When H/$\overline{S}$ is HI, the buffer outputs are set to a high-impedance state.

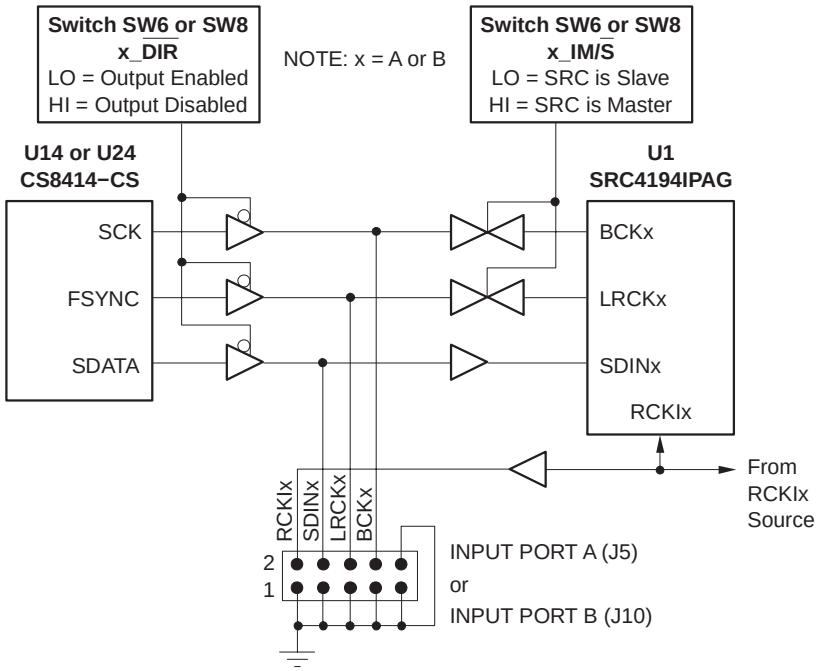
The Host Port header provides a convenient interface point for connection to an external host device, such as a microprocessor, a digital signal controller/processor, or a digital input/output card installed in a PC.

Refer to the SRC4194 datasheet for a description of the SPI port protocol and control register definitions.

3.3 Audio Input Ports

The SRC4192EVM includes four audio input ports, two each for the SRC A and SRC B sections of the SRC4194. Each section is provided with an AES3/SPDIF-compatible input, along with a buffered I/O header. Figure 3−2 illustrates the input port external connections and associated switch settings.

Figure 3−2. Input Port External Connections and Configuration



The SRC A section input port selection and Master/Slave mode operation are configured using the A_$\overline{DIR}$ and A_IM/$\overline{S}$ elements of switch SW6. The SRC B section input port selection and Master/Slave mode operation are configured using the B_$\overline{DIR}$ and B_IM/$\overline{S}$ elements of switch SW8.

The AES IN A (J6) and AES IN B (J11) connectors accept 75Ω coaxial cable connections terminated with RCA plugs. The onboard AES3 receivers (U14 and U24) recover audio clocks and data from the AES3 encoded input stream. The receivers are configured to output 24-bit I^2S-formatted audio data with a serial bit (or data) clock rate of $64f_S$ and a left/right word clock rate of f_S, where f_S is the frame or sampling rate of the incoming AES3-formatted data stream. Sampling rates up to 108kHz are supported. The AES IN A and B input ports provide a convenient, standard interface to consumer and professional audio equipment, as well as common audio test systems.

The buffered input serial ports INPUT PORT A (J5) and INPUT PORT B (J10) support Left-Justified, Right-Justified, and I^2S-formatted audio data with word lengths up to 24 bits and sampling rates up to 212kHz. The input ports may be operated in either Slave or Master mode, but must match the input port set-up for the SRC4194 device, as defined in Table 3−3. The buffered serial input ports provide a convenient method for interfacing to audio devices that support an audio serial data interface, including external digital audio receivers, audio data converters, and digital signal processing components.

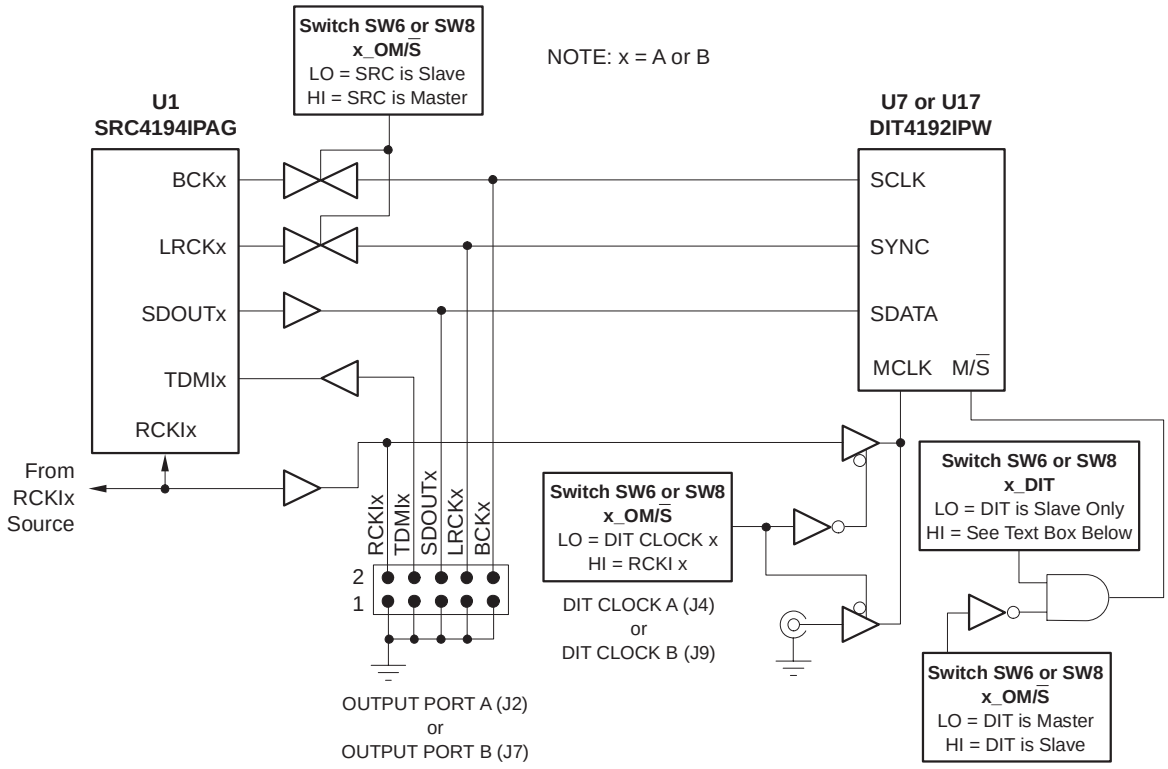
3.4 Audio Output Ports

The SRC4192EVM includes four audio output ports, two each for the SRC A and SRC B sections of the SRC4194. Each section is provided with an AES3/SPDIF-compatible output, along with a buffered I/O header. Figure 3−3 illustrates the output port external connections and associated switch settings.

The SRC A section output port selection and Master/Slave mode operation are configured using switch SW6. The SRC B section output port selection and Master/Slave mode operation are configured using switch SW8.

The AES OUT A (J3) and AES OUT B (J8) connectors accept 75Ω coaxial cable connections terminated with RCA plugs. The onboard AES3 transmitters (U7 and U17) provide the AES3 encoded data streams for each output. Both transmitters are configured to accept 24-bit I^2S-formatted audio data at sampling rates up to 192kHz. The AES OUT A and B output ports provide a convenient, standard interface to consumer and professional audio equipment, as well as common audio test systems.

Figure 3−3. Output Port External Connections and Configuration



The DIT4192 transmitters (U7 and U17) have additional configuration switches, summarized in Table 3−4 and Table 3−5. For the clock divider, the corresponding control pins need to be set dependent upon the incoming master clock (MCLK) and output sampling rates, f_{Sout}. The master clock (MCLK) rate is set by either reference clock RCKIA or RCKIB, or by the corresponding DIT CLOCK input at connector J4 or J9 (dependent upon the clock configuration; see Figure 3−3 and Figure 3−4).

Stereo mode operation is the default for most test cases. The Mono mode configuration is utilized primarily to support testing at 176.4kHz and 192kHz output sampling rates using an Audio Precision System Two Cascade or Cascade Plus test system with Dual Channel mode support.

The buffered output serial ports OUTPUT PORT A (J2) and OUTPUT PORT B (J7) support Left-Justified, Right-Justified, I^2S, and time division multiplexed (TDM) formatted audio data with word lengths up to 24 bits and sampling rates up to 212kHz. The output ports may be operated in either Slave or Master mode, but must match the output port setup for the SRC4194 device as defined in Table 3−3. The buffered serial output ports provide a convenient method for interfacing to audio devices which support an audio serial data interface, including external digital audio transmitters, audio data converters, and signal processing components.

Table 3−4. Transmitter Clock Divider Configuration

If MCLK Rate Equal To:	Set Transmitter Clock Divider Switches To:
$128 \times f_{sOUT}$	x_CLK0 = LO, x_CLK1 = LO
$256 \times f_{sOUT}$	x_CLK0 = HI, x_CLK1 = LO
$384 \times f_{sOUT}$	x_CLK0 = LO, x_CLK1 = HI
$512 \times f_{sOUT}$	x_CLK0 = HI, x_CLK1 = HI
Where f_{sOUT} = the output sampling rate	Where x = A (switch SW6) or B (switch SW8)

Table 3−5. Transmitter Stereo/Mono Mode Configuration

Transmitter Output Mode	Set Mode Switches To:
Stereo	x_MONO = LO, x_MDAT = LO
Mono with Left Channel Data Source	x_MONO = HI, x_MDAT = LO
Mono with Right Channel Data Source	x_MONO = HI, x_MDAT = HI
	Where x = A (switch SW6) or B (switch SW8)

3.5 Reference Clock Generation

The SRC4194EVM supports a flexible configuration for the SRC4194 reference clock generation. Figure 3−4 illustrates the PLL and clock connections used for the reference clocks.

Both SRC A and SRC B have their own reference clocks, referred to as RCKIA and RCKIB, respectively. The reference clocks may be derived by onboard PLL clock generators (U25 and U28), or by external clock sources applied at connectors J12 and J13. Table 3−6 summarizes the output rates available from the onboard PLL circuits.

The reference clocks are also used by the transmitter sections of the EVM, and are made available at the audio input and output ports for use by external hardware.

Figure 3−4. Reference Clock Generation, Connections, and Configuration

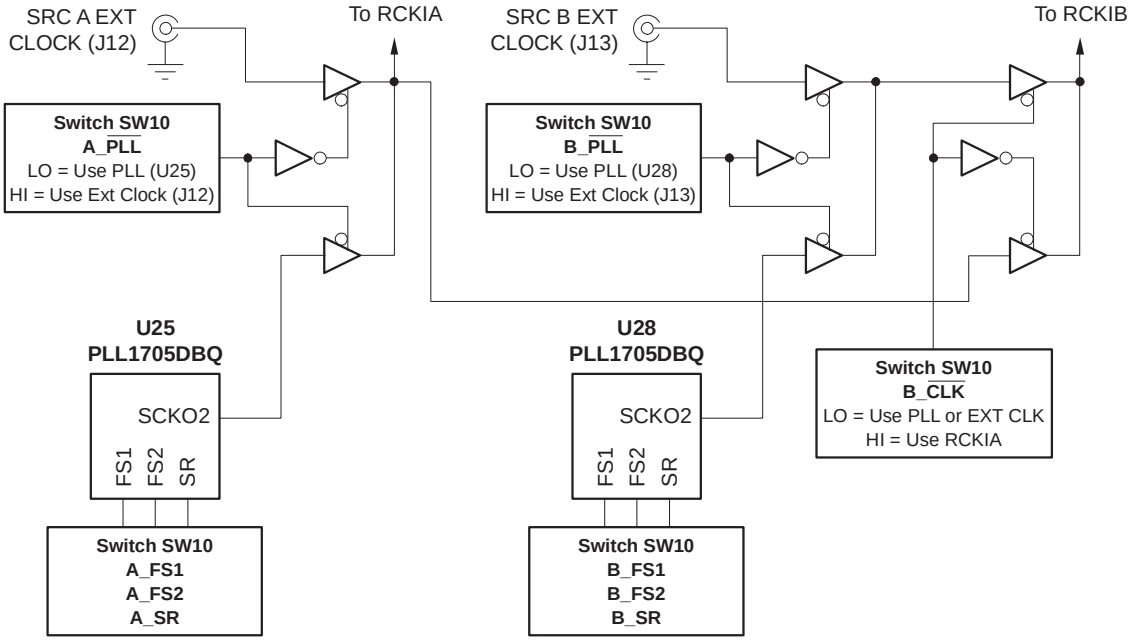


Table 3−6. PLL Configuration for U25 and U28

x_SR (switch SW10)	x_FS2 (switch SW10)	x_FS1 (switch SW10)	PLL Output Rate
LO	LO	LO	12.288 MHz
LO	LO	HI	11.2896 MHz
LO	HI	LO	8.192 MHz
LO	HI	HI	Reserved
HI	LO	LO	24.576 MHz
HI	LO	HI	22.5792 MHz
HI	HI	LO	16.384 MHz
HI	HI	HI	Reserved
Where x = A or B	Where x = A or B	Where x = A or B	

3.6 TDM Test Mode

Jumper J18 is provided to allow a simple onboard connection between SDOUTA (pin 64) and TDMIB (pin 52). This provides a test mode for evaluating the TDM output data format. When J18 is shorted, the TDMIB pin at header J7 should be floating, with no external connection.

Chapter 4

Schematic, PCB Layout, and Bill of Materials

This chapter provides the electrical schematic and physical layout information for the SRC4194EVM. The bill of materials is included for component and manufacturer reference.

Topic **Page**

4.1 Schematic 4-2
4.2 PCB Layout 4-5
4.3 Bill of Materials 4-11

4.1 Schematic

The electrical schematic for the SRC4194EVM is shown in Figure 4−1 and Figure 4−2. Descriptions of the components shown on the schematics are listed in Table 4−1.

Figure 4−1. SRC4194EVM Schematic Diagram, Page 1 of 2

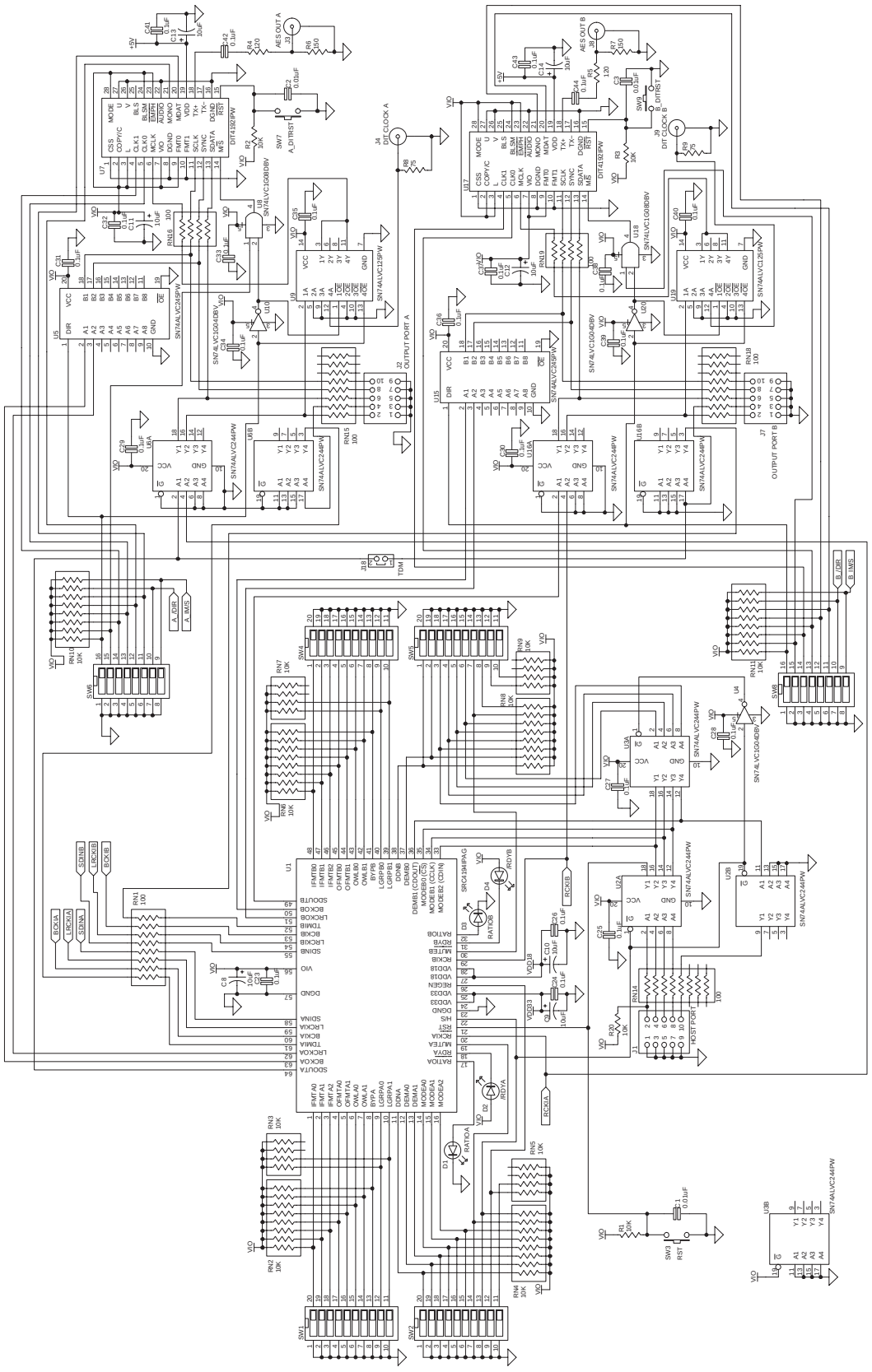
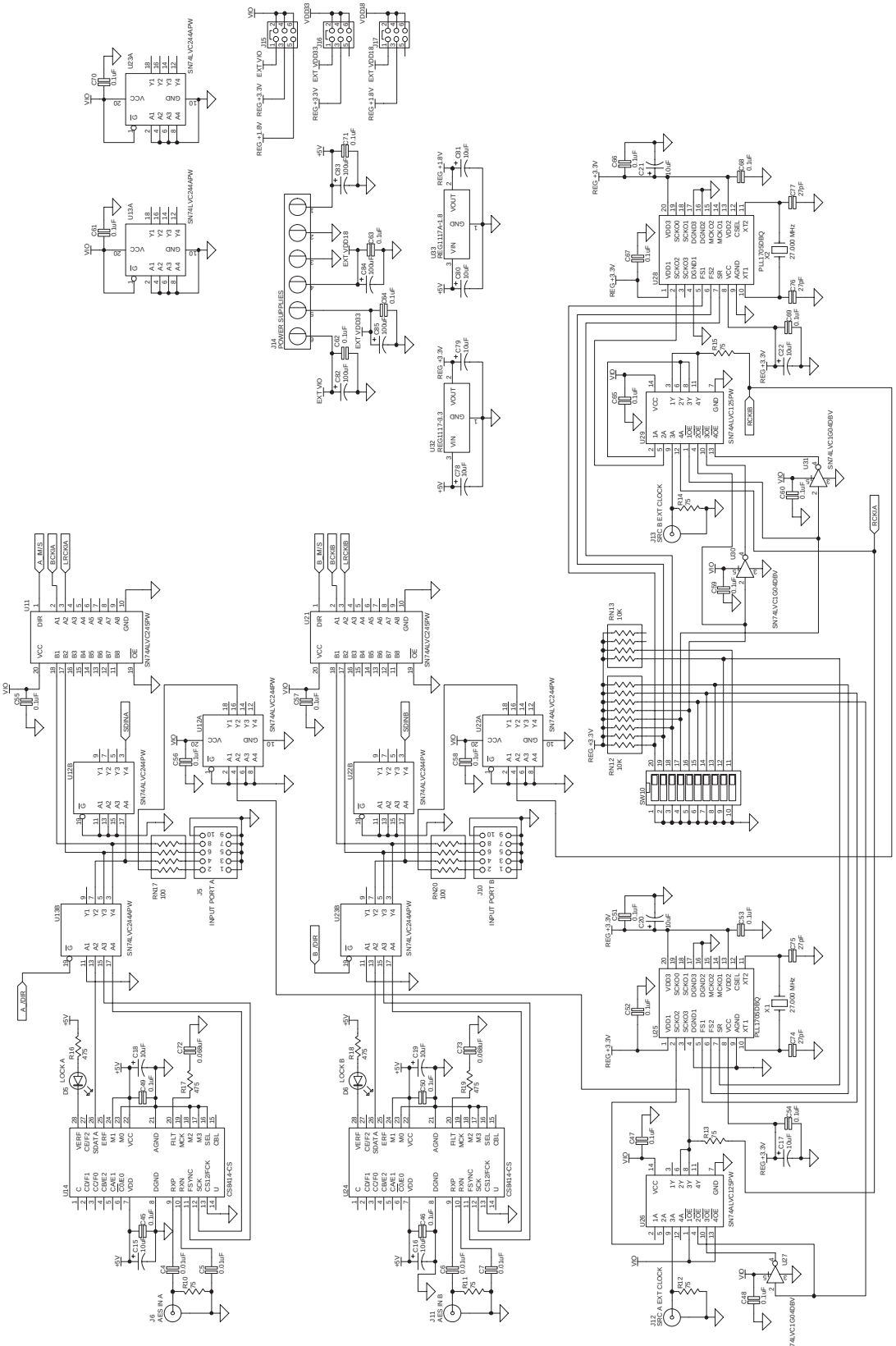


Figure 4−2. SRC4194EVM Schematic Diagram, Page 2 of 2



4.2 PCB Layout

The SRC4194EVM is a four-layer printed circuit board (PCB) with the following layer structure:

- Layer 1: Top (Component Side)
- Layer 2: Ground Plane
- Layer 3: Power
- Layer 4: Bottom (Solder Side)

Figure 4−3 through Figure 4−8 show the top side silk screen, along with the top, ground plane, power, and bottom layers of the printed circuit assembly.

Figure 4−3. Top Side Silk Screen

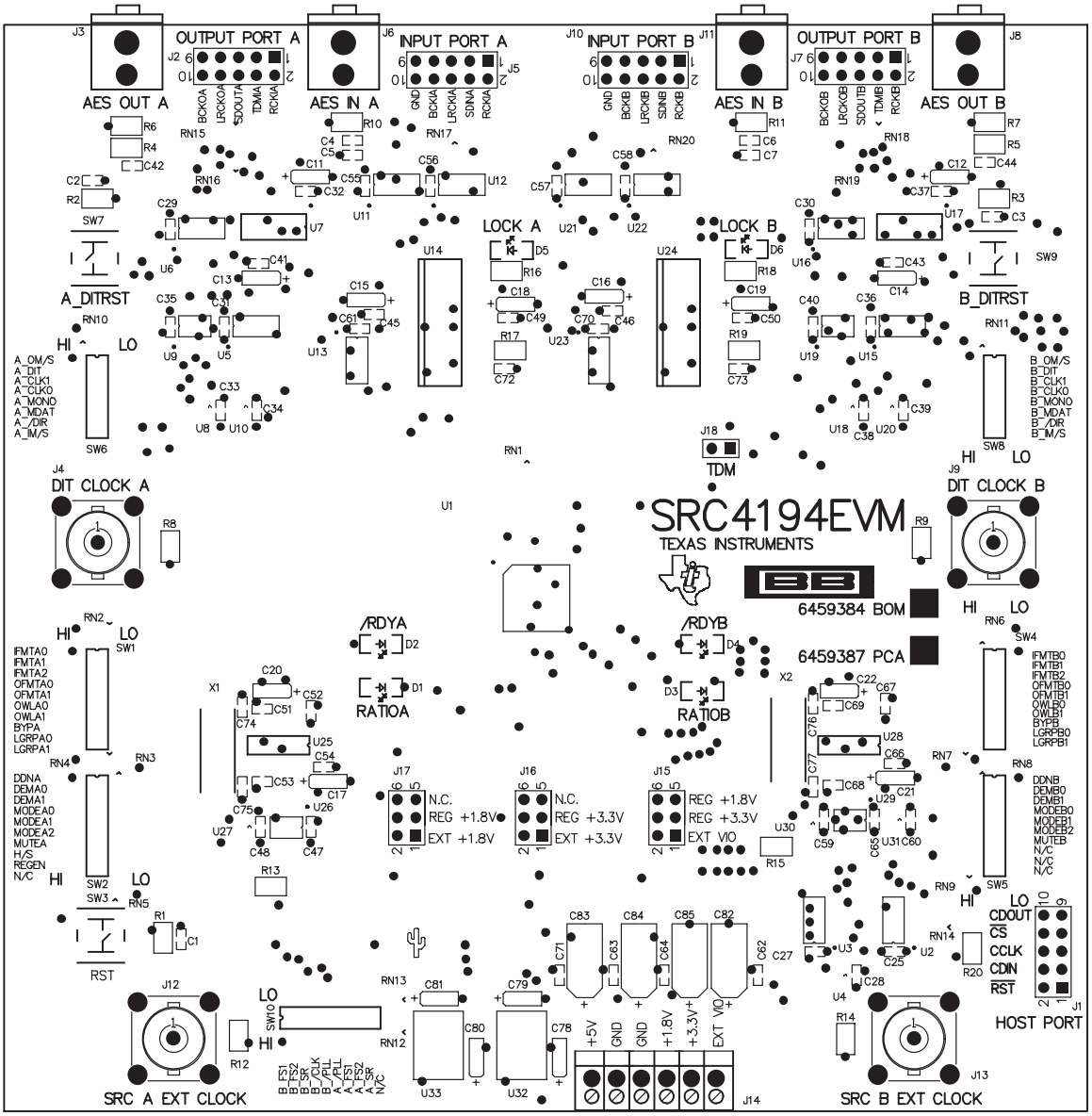


Figure 4−4. Bottom Side Silk Screen

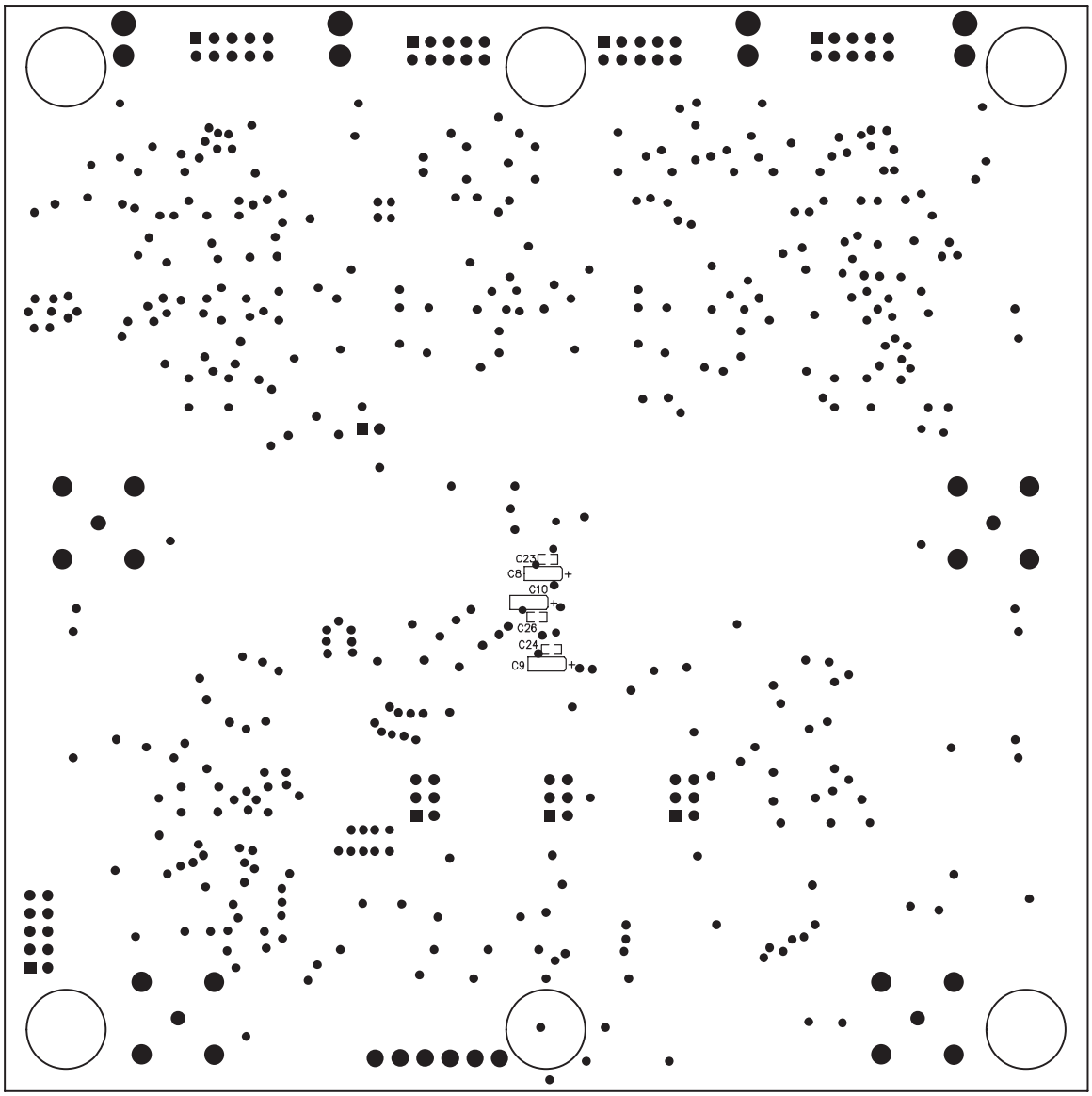


Figure 4−5. Top Layer (Component Side)

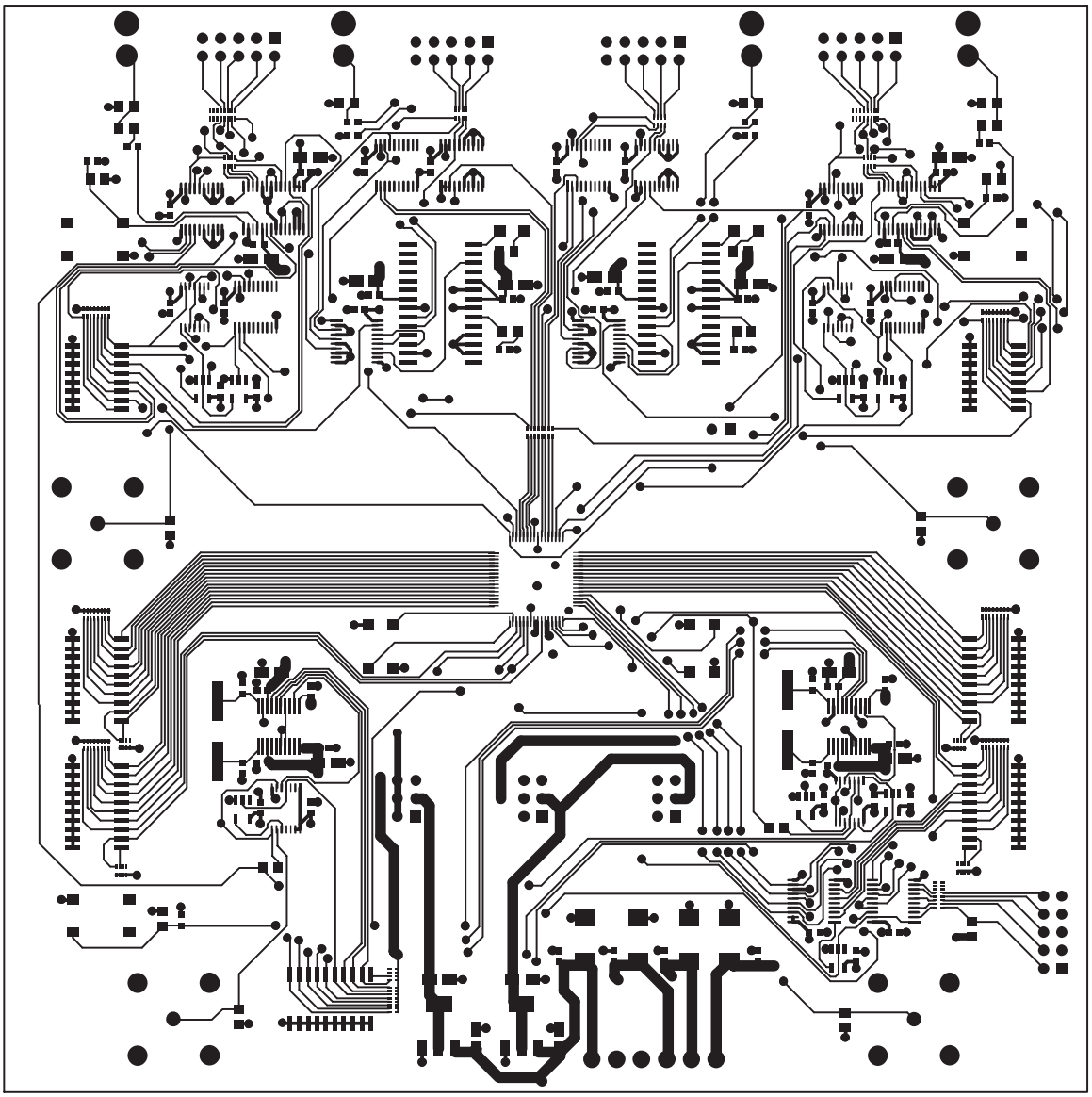


Figure 4−6. Ground Plane Layer

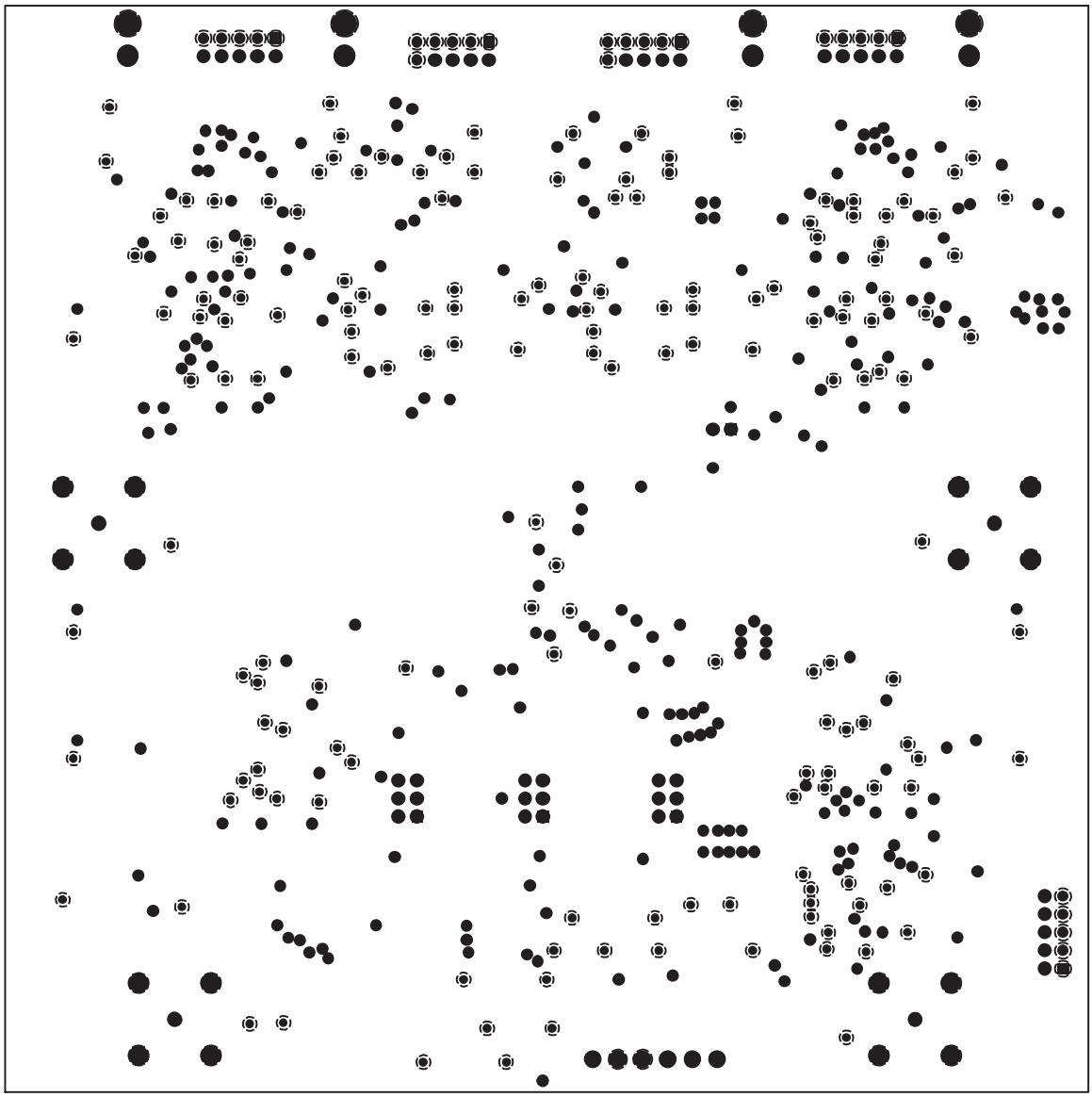


Figure 4−7. Power Layer

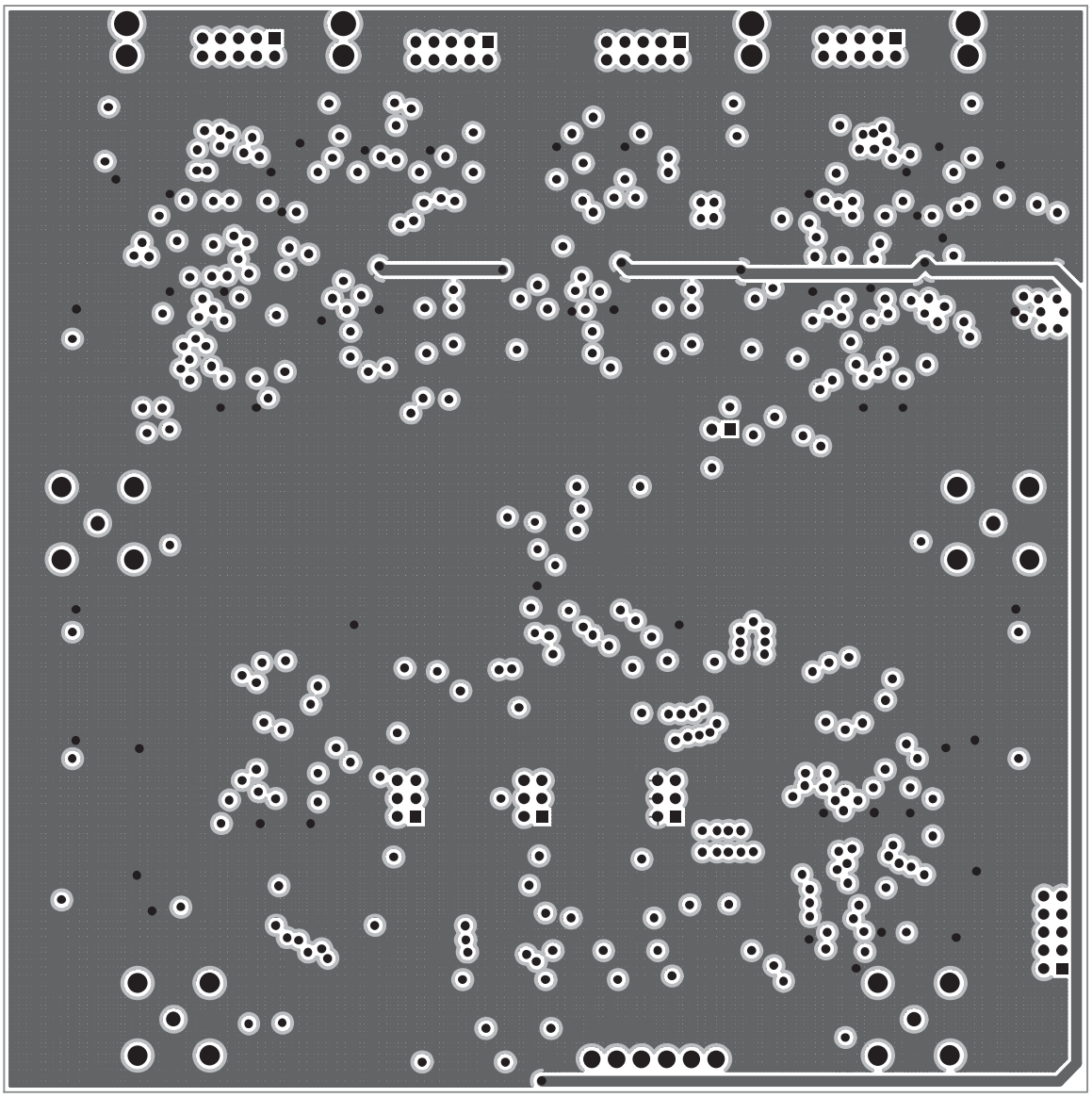
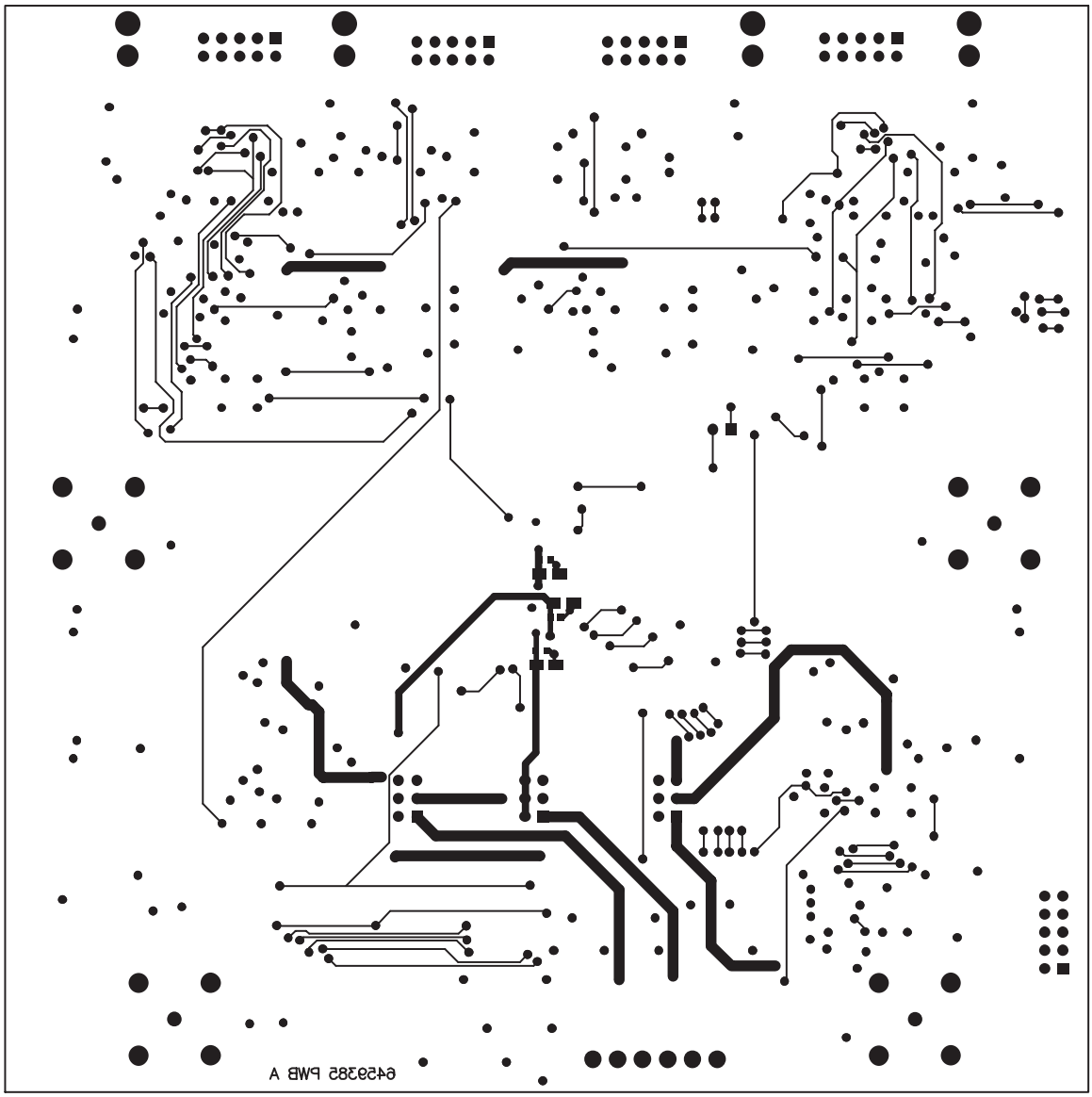


Figure 4−8. Bottom layer (Solder Side)



4.3 Bill of Materials

The bill of materials, listing the components used in the assembly of the SRC4194EVM, is shown in Table 4−1.

Table 4−1. SRC4194EVM Bill of Materials

ITEM	VALUE	REFERENCE DESIGNATOR	QTY PER BOARD	MFG	MANUFACTURER PART NUMBER	DESCRIPTION
1	27pF	C74−C77	4	Kemet	C0603C270J5GACTU	Chip Capacitor, NPO/C0G Ceramic, 27pF, ±5%, 50WV, Size = 0603
2	0.01µF	C1−C7	7	Kemet	C0603C103J5RACTU	Chip Capacitor, X7R Ceramic, 0.01µF, ±5%, 50WV, Size = 0603
3	0.068µF	C72, C73	2	Kemet	C0603C683J4RACTU	Chip Capacitor, X7R Ceramic, 0.068µF ±5%, 16WV, Size = 0603
4	0.1µF	C23−C71	49	Kemet	C0603C104K4RACTU	Chip Capacitor, X7R Ceramic, 0.1µF ±10%, 16WV, Size = 0603
5	10µF	C8−C22, C78−C81	19	Kemet	T491A106K010AS	Chip Capacitor, Tantalum, 10µF ±10%, 10WV, Size = A
6	100µF	C82−C85	4	Kemet	T491D107K010AS	Chip Capacitor, Tantalum, 100µF ±10%, 10WV, Size = D
7		J1, J2, J5, J7, J10	5	Samtec	TSW−105−07−G−D	Terminal Strip, 10-pin (5x2)
8		J3, J6, J8, J11	4	CUI Stack	RCJ−041	RCA Jack, PC Mount, Black
9		J4, J9, J12, J13	4	Kings Electronics	KC−79−274−M06	BNC Connector, Female, PC Mount
10		J14	1	Weidmuller	9967720000	Terminal Block, 3.5mm PCB, 6 poles
11		J15−J17	3	Samtec	TSW−103−07−G−D	Terminal Strip, 6-pin (3x2)
12		J18	1	Samtec	TSW−102−07−G−S	Terminal Strip, 2-pin (2x1)
13		D1−D6	6	Lumex	SML−LX1206GC−TR	Green LED, SMT, Size = 1206
14	75Ω	R8−R15	8	Panasonic or equivalent	ERJ−6ENF75R0V	Resistor, 75Ω, ±1%, 1/10W, Thick Film Chip, Size = 0805
15	120Ω	R4, R5	2	Panasonic or equivalent	ERJ−6ENF1200V	Resistor, 120Ω, ±1%, 1/10W, Thick Film Chip, Size = 0805

Table 4−1. SRC4194EVM Bill of Materials (continued)

ITEM	VALUE	REFERENCE DESIGNATOR	QTY PER BOARD	MFG	MANUFACTURER PART NUMBER	DESCRIPTION
16	150Ω	R6, R7	2	Panasonic or equivalent	ERJ−6ENF1500V	Resistor, 150Ω, ±1%, 1/10W, Thick Film Chip, Size = 0805
17	475Ω	R16−R19	4	Panasonic or equivalent	ERJ−6ENF4750V	Resistor, 475Ω, ±1%, 1/10W, Thick Film Chip, Size = 0805
18	10kΩ	R1−R3	3	Panasonic or equivalent	ERJ−6ENF1002V	Resistor, 10kΩ, ±1%, 1/10W, Thick Film Chip, Size = 0805
19	100Ω	RN1, RN14, RN15, RN18	4	CTS	741X163101JCT−ND	Thick Film Chip Resistor Array, 100Ω, 16-terminal, 8 resistors
20	100Ω	RN16, RN17, RN19, RN20	4	CTS	741X083101JCT−ND	Thick Film Chip Resistor Array, 100Ω, 8-terminal, 4 resistors
21	10kΩ	RN2, RN4, RN6, RN8, RN10, RN11, RN12	7	CTS	741X163103JCT−ND	Thick Film Chip Resistor Array, 10kΩ, 16-terminal, 8 resistors
22	10kΩ	RN3, RN5, RN7, RN9, RN13	5	CTS	741X083103JCT−ND	Thick Film Chip Resistor Array, 10kΩ, 8-terminal, 4 resistors
23		SW1, SW2, SW4, SW5	5	ITT C&K Switch	TDA10H0SK1	DIP Switch, 10-Position, Half Pitch Surface-Mount, Tape-Sealed
24		SW6, SW8	2	ITT C&K Switch	TDA08H0SK1	DIP Switch, 8-Position, Half Pitch Surface-Mount, Tape-Sealed
25		SW3, SW7, SW9	3	Omron	B3S−1000	Momentary Tact Switch, SMT w/o Ground Terminal
26		U1	1	Texas Instruments	SRC4194IPAG	4-Channel Asynchronous, Sample Rate Converter
27		U2, U3, U6, U12, U16, U22	6	Texas Instruments	SN74ALVC244PW	Octal Buffer/Driver with Tri-State Outputs
28		U4, U10, U20, U27, U30, U31	6	Texas Instruments	SN74LVC1G04DBV	Single Inverter
29		U5, U11, U15, U21	4	Texas Instruments	SN74ALVC245PW	Octal Bus Transceiver with Tri−State Outputs

Table 4−1. SRC4194EVM Bill of Materials (continued)

ITEM	VALUE	REFERENCE DESIGNATOR	QTY PER BOARD	MFG	MANUFACTURER PART NUMBER	DESCRIPTION
30		U7, U17	2	Texas Instruments	DIT4192IPW	192kHz Digital Audio Transmitter
31		U8, U18	2	Texas Instruments	SN74LVC1G08DBV	Single AND Gate
32		U9, U19, U26, U29	4	Texas Instruments	SN74ALVC125PW	Quad Buffer with Tri−State Outputs
33		U13, U23	2	Texas Instruments	SN74LVC244APW	Octal Buffer/Driver with Tri−State Outputs
34		U14, U24	2	Cirrus Logic	CS8414−CS	96kHz Digital Audio Interface Receiver
35		U25, U28	2	Texas Instruments	PLL1705DBQ	Dual PLL Multiclock Generator
36		U32	1	Texas Instruments	REG1117−3.3	+3.3V Linear Voltage Regulator
37		U33	1	Texas Instruments	REG1117A−1.8	+1.8V Linear Voltage Regulator
38		X1, X2	2	Citizen	HCM49−27.000MABJT	Quartz Crystal, SMT, 27.000MHz ±50ppm
39			4	3M Bumpon	SJ−5003	Rubber Feet, Adhesive Backed
40			4	Samtec	SNT−100−BK−G−H	Shorting Blocks