User's Guide

ADS131B26Q1EVM-PDK Evaluation Module

ABSTRACT

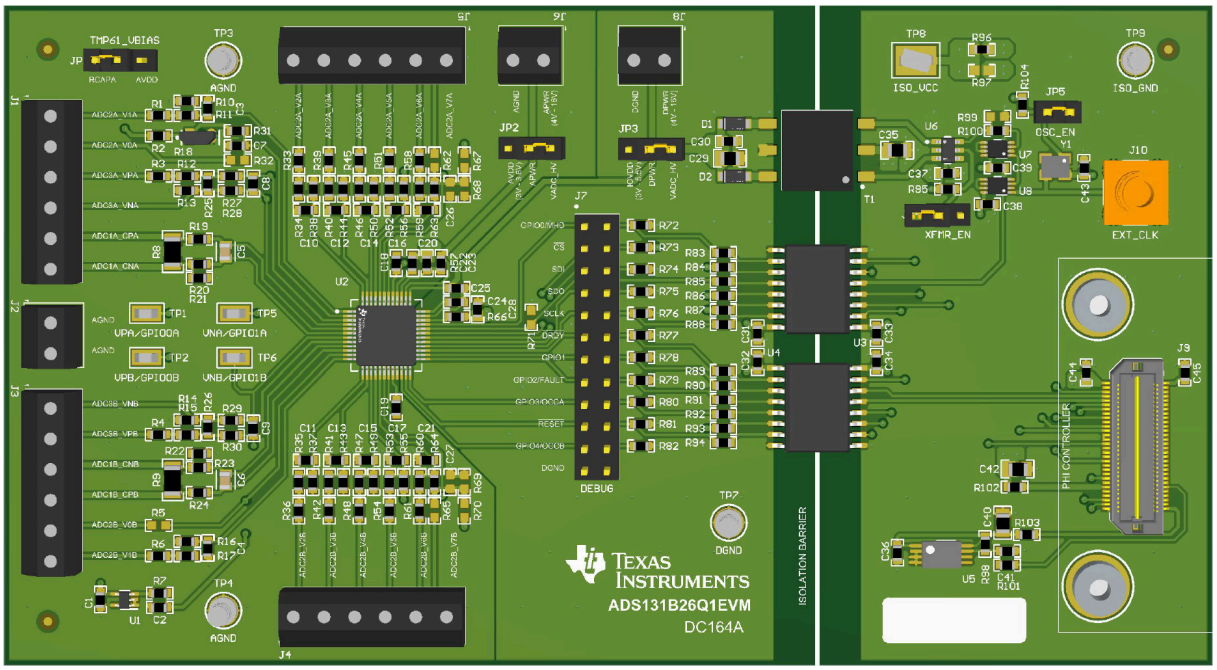

Figure 1-1. ADS131B26Q1EVM-PDK Evaluation Module

This user's guide describes the design and operation of the ADS131B26Q1EVM-PDK. This evaluation module (EVM) is an evaluation board for the ADS131B26-Q1, a complete analog front-end (AFE) for automotive electrical vehicle (EV) battery management systems (BMS) that integrates two pairs of simultaneous-sampling, high-precision, 24-bit analog-to-digital converter (ADC) channels to redundantly measure battery current and battery pack voltage with high resolution and accuracy. The EVM allows evaluation of all aspects of the ADS131B26-Q1. This user's guide covers the operation of the ADS131B26Q1EVM-PDK. Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the ADS131B26Q1EVM-PDK. The terms *PHI controller*, *PHI*, and *host* are synonymous with the precision host interface (PHI) controller board that interfaces the EVM to the PC. Complete circuit descriptions, schematic diagrams, and bill of materials are included in this document.

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1 EVM Overview

The evaluation kit includes the ADS131B26Q1EVM-PDK board and the precision host interface (PHI) controller board. The PHI board enables the accompanying computer software to communicate with the ADC over the universal serial bus (USB) for data capture and analysis.

The PHI board primarily serves three functions:

- Provides a communication interface between the EVM and the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS131B26Q1EVM-PDK
- Supplies power to all active circuitry on the ADS131B26Q1EVM-PDK board

The following related documents are available for download through the Texas Instruments web site at www.ti.com.

Table 1-1. Related Documentation

Device	Literature Number
ADS131B26-Q1	SBASA22
SN6505B-Q1	SLLSF95
ISO7762-Q1	SLLSEU7
ISO7761-Q1	SLLSEU7
TMP61-Q1	SNIS210
LMT84-Q1	SNIS178

1.1 ADS131B26Q1EVM-PDK Features

The ADS131B26-Q1 evaluation module kit includes the following features:

- Contains all support circuitry needed for the ADS131B26-Q1
- USB powered: No external power supply is required
- Analog-to-digital converter (ADC) voltage supply options:
  - DC/DC converter output provides APWR and DPWR supplies, which the ADC uses to generate AVDD and DVDD with the respective integrated low-dropout regulators (LDOs)
  - APWR and DPWR can be provided externally while still using the respective integrated LDOs when the external supply is between 4 V and 16 V
  - APWR and DPWR can be shorted to the respective LDO outputs if the external supply is between 3 V and 3.6 V
- Clock options: Internal ADC clock, onboard 8.192-MHz crystal oscillator, or external clock with a sub-miniature version A (SMA) connector
- Input signals provided by terminal blocks connect to various application circuits for voltage, current, and temperature measurements
- Digital inputs and outputs are connected to a dual-row DEBUG header for connections to a logic analyzer or external controller
- EVM GUI includes a complete register map page for ease of device configuration and a built-in analysis tool suite complete with scope, FFT, and histogram displays
- Two 16-bit multiplexed ADC channels allow for measuring multiple single-ended and pseudo-differential inputs in a specified sequence in conjunction with the four 24-bit simultaneous-sampling ADC channels

1.2 ADS131B26Q1EVM-PDK Quick-Start Guide

The following instructions are a step-by-step guide to connecting the ADS131B26Q1EVM-PDK to the computer and evaluating the performance of the ADS131B26-Q1:

1. Review the default jumper settings in Section 5.1 and GUI software installation in Section 5.2.
2. Connect the ADS131B26Q1EVM-PDK to the PHI controller. Install the two screws as indicated in Figure 1-1.
3. Connect the PHI controller to your PC using the provided USB micro cable. Three LEDs illuminate on the PHI controller to indicate connectivity to the PC.
   a. LED D5 lights up solid, indicating that the PHI is powered up.
   b. LEDs D1 and D2 start blinking at different rates to indicate that the PHI is booted up and communicating with the PC. Figure 1-1 shows the resulting LED indicators.

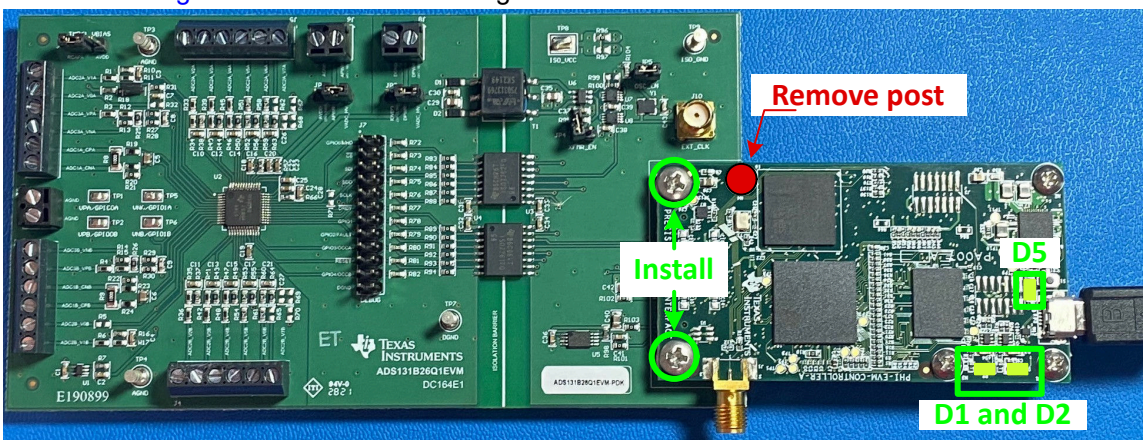


Figure 1-1. ADS131B26Q1EVM-PDK PHI Connection and LED Indicators

4. Launch the ADS131B26Q1EVM-PDK GUI software and power is supplied to the EVM. The default installation path is *C:\Program Files (x86)\Texas Instruments\ADS131B26-Q1 EVM*.
5. When the GUI finishes loading and is connected to the EVM hardware, the screen appears as illustrated in Figure 6-1. The GUI consists of multiple *Pages*, which include:
   - Register Map Config
   - Time Domain Display
   - Spectral Analysis
   - Histogram Analysis
   - Channel Configurations
   - Sequencer Configurations

   Below the *Pages* section are the basic SPI op-code commands, the *Data Capture Configuration* controls, and the current *Clocks and Data Rate* information. Section 6.1 details the EVM GUI pages and data capture controls.

2 Analog Interface

The ADS131B26Q1EVM-PDK is designed for easy and complete evaluation of the ADS131B26-Q1 using external voltage, current, and temperature sensor inputs. This section details the analog front-end circuitry, including jumper configurations, terminal block connectors, and test points for different input test signals.

2.1 Terminal Blocks and Test Points

Analog inputs to the EVM can be connected to either terminal block associated with each ADC channel. The screw terminal blocks (J1 through J5) can interface directly with the leads of an external source. Table 2-1 lists the supported input options. Table 2-2 lists key test points.

An input must not be applied such that the voltage on the input pins of the ADS131B26-Q1 exceeds the absolute maximum ratings. For more details, see the ADS131B26-Q1 data sheet.

Table 2-1. Analog Input Terminal Blocks (J1 - J5)

Terminal Block	Pin	Function	Input Range	ADS131B26-Q1 Input Pins
J1	1	Unipolar voltage input	0 V to 10 V (Gain = 1)	V1A
	2	Unipolar voltage input	0 V to 1.25 V (Gain = 1)	V0A
	3	Differential voltage, positive input or general-purpose digital input/output	–10 V to 10 V (Gain = 4)	VPA/GPIO0A
	4	Differential voltage, negative input or general-purpose digital input/output	Shorted to AGND (default)	VNA/GPIO1A
	5	Differential current, positive input	0 mA to 12.5 mA (Gain = 1)	CPA
	6	Differential current, negative input	Shorted to AGND (default)	CNA
J2	1	AGND	-	AGND, AGNDA, and AGNDB
	2	AGND	-	AGND, AGNDA, and AGNDB
J3	1	Differential voltage, negative input or general-purpose digital input/output	Shorted to AGND (default)	VNB/GPIO1B
	2	Differential voltage, positive input or general-purpose digital input/output	–10 V to 10 V (Gain = 4)	VPB/GPIO0B
	3	Differential current, negative input	Shorted to AGND (default)	CNB
	4	Differential current, positive input	0 mA to 12.5 mA (Gain = 1)	CPB
	5	Unipolar voltage input	0 V to 1.25 V (Gain = 1)	V0B
	6	Unipolar voltage input	0 V to 10 V (Gain = 1)	V1B
J4	1	Unipolar voltage input	0 V to 10 V (Gain = 1)	V2B
	2	Unipolar voltage input	–10 V to 10 V (Gain = 4)	V3B
	3	Unipolar voltage input	–10 V to 10 V (Gain = 4)	V4B
	4	Unipolar voltage input	–8.5 V to 10 V (Gain = 2)	V5B
	5	Unipolar voltage input	–8.5 V to 10 V (Gain = 2)	V6B
	6	Unipolar voltage input		V7B
J5	1	Unipolar voltage input		V7A
	2	Unipolar voltage input	–8.5 V to 10 V (Gain = 2)	V6A
	3	Unipolar voltage input	–8.5 V to 10 V (Gain = 2)	V5A
	4	Unipolar voltage input	–10 V to 10 V (Gain = 4)	V4A
	5	Unipolar voltage input	–10 V to 10 V (Gain = 4)	V3A
	6	Unipolar voltage input	0 V to 10 V (Gain = 1)	V2A

Table 2-2. Key Voltage Test Points

Test Point	Function	Input Range	ADS131B26-Q1 Input Pins
TP1	Probe VNA or GPIO0A	–10 V to 10 V (Gain = 4)	VPA/GPIO0A
TP2	Probe VPB or GPIO0B	–10 V to 10 V (Gain = 4)	VPB/GPIO0B
TP3	Ground clip for scope / multimeter	-	AGND, AGNDA, and AGNDB
TP4	Ground clip for scope / multimeter	-	AGND, AGNDA, and AGNDB
TP5	Probe VNA or GPIO1A	Shorted to AGND (default)	VNA/GPIO1A
TP6	Probe VNB or GPIO1B	Shorted to AGND (default)	VNB/GPIO1B

2.2 ADC1A and ADC1B

The ADS131B26-Q1 features two high-precision, 24-bit ADC channels that are intended for battery current-shunt measurements (ADC1A and ADC1B). For demonstration purposes, the EVM includes a 100-Ω, 1206-footprint resistor on ADC1A and ADC1B to function as a current-shunt resistor (R8 and R9, respectively). A more realistic application uses a much smaller shunt resistor value (that is, 50 µΩ) that is not practical to include on the EVM hardware. A small current up to 12.5 mA at gain = 1 can be applied to the positive channel input (CPA and CPB), and the low-side of the shunt resistor is connected to AGND by default. Figure 2-1 shows the current input schematic for ADC1A.

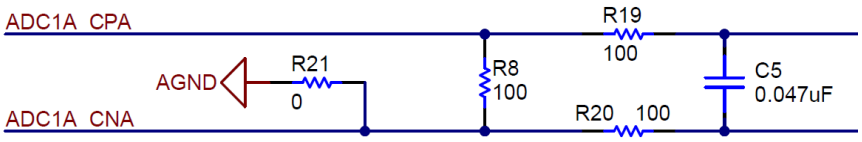


Figure 2-1. ADC1A Current Input Circuit (Schematic)

2.3 ADC2A and ADC2B

The ADS131B26-Q1 features two multiplexed, 16-bit ADC channels that are intended to measure shunt temperature using external temperature sensors and other voltages in the system. For demonstration purposes, the EVM includes multiple resistor divider ratios to support unipolar and bipolar single-ended and pseudo-differential input measurements.

The V7A and V7B signals can serve as the common-mode voltage when measuring V5A and V6A or V5B and V6B, respectively. Alternatively, an external common-mode voltage can be generated from the analog supply voltage (ADC_AVDD) by installing the *optional external VCM* circuit shown in Figure 2-2. Figure 2-2 shows the input connections and resistor divider circuits for ADC2A.

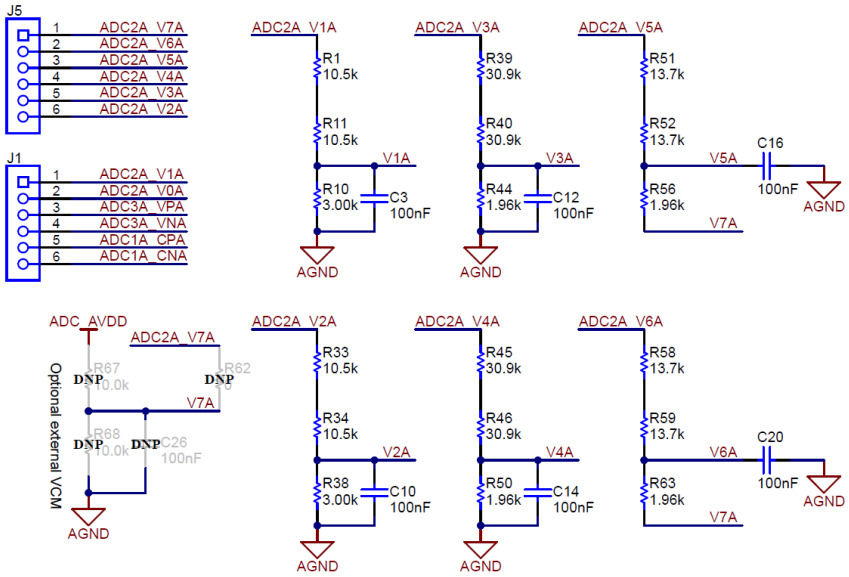


Figure 2-2. ADC2A Sequencer Input Circuits (Schematic)

2.4 ADC3A and ADC3B

The ADS131B26-Q1 features two high-precision, 24-bit ADC channels that are intended for battery stack voltage measurements (ADC3A and ADC3B). For demonstration purposes, the EVM includes a resistor divider circuit with an approximate ratio of 1 / 32.5. At gain = 4, which allows an input voltage from –10 V to 10 V on the positive voltage measurement inputs (VPA and VPB). The negative voltage measurement inputs (VNA and VNB) are connected to AGND by default. Figure 2-3 shows the voltage input schematic for ADC3A.

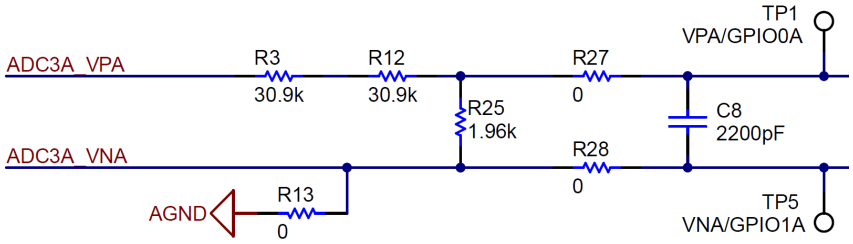


Figure 2-3. ADC3A Voltage Input Circuit (Schematic)

3 Digital Interface

As noted in Section 1, the EVM interfaces with the PHI controller and communicates with the PC over USB. There are two devices on the EVM with which the PHI controller communicates: the ADS131B26-Q1 (by SPI) and the EEPROM (by I^2C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS131B26Q1EVM-PDK GUI software. When the hardware is initialized, the EEPROM is no longer used.

3.1 Connection to the PHI Controller

The ADS131B26Q1EVM-PDK communicates with the PHI controller through a shrouded, 60-pin connector (J9). There are two round standoffs next to J9 with Phillips-head screws. To connect the PHI controller to the EVM, remove the screws, attach the PHI controller to the EVM, and replace the screws into the standoffs. The screws secure the EVM to the PHI and makes sure the connection between the two boards is complete.

Table 3-1 lists the different PHI connection and their functions.

Table 3-1. PHI Connector Pin Functions

PHI Connector Pin Name	PHI Connector Pin	Function
EVM_REG_5.5V	J9[1]	Boosted 5.5-V supply from the USB (not used)
EVM_RAW_5V	J9[2]	Raw USB 5-V supply; optional supply for the DC/DC input
ISO_GND	J9[3]	Ground connection for the isolated host controller side of the EVM
ISO_GPIO0/MHD	J9[6]	General-purpose digital input/output 0 or missing host detect output
ISO_GPIO1	J9[8]	General-purpose digital input/output 1
ISO_GPIO2/FAULT	J9[10]	General-purpose digital input/output 2 or fault output
ISO_GPIO3/OCCA	J9[12]	General-purpose digital input/output 3 or overcurrent comparator A output
ISO_GPIO4/OCCB	J9[14]	General-purpose digital input/output 4 or overcurrent comparator B output
ISO_SDI	J9[18]	SPI: Serial data input to the ADC
ISO_CSn	J9[22]	SPI: Chip-select input from the PHI controller; active low
ISO_SCLK	J9[24]	SPI: Serial data clock input
ISO_CAPCLK	J9[26, 28]	PHI clock signal to synchronize SPI transactions with the propagation delay from the EVM
ISO_DRDYn	J9[30]	SPI: Data-ready output from the ADC; active low
ISO_SDO	J9[38]	SPI: Serial data output from the ADC
ISO_RESETn	J9[46]	Reset input; active low
WP	J9[49]	Write protection for the EEPROM
ISO_3V3	J9[50]	Power-supply source for the isolated host controller side of the EVM and default supply input to the DC/DC circuit
EVM_ID_SDA	J9[56]	I^2C serial data for the EEPROM
EVM_ID_SCL	J9[58]	I^2C serial clock for the EEPROM
ID_PWR	J9[59]	Power-supply source for the EEPROM
ISO_GND	J9[60]	Ground connection for the isolated host controller side of the EVM

3.2 Digital Header

In addition to the PHI connector, header J7 on the EVM is connected to the digital inputs and outputs between the ADS131B26-Q1 and the PHI connector. Each row is shorted across both pins to allow access to an external logic analyzer or oscilloscope and an external controller simultaneously. Table 3-2 lists the digital header pins.

Table 3-2. DEBUG Header Pins (J7)

Signal Name	Digital Header Pins
GPIO0/MHD	J7[1-2]
CSn	J7[3-4]
SDI	J7[5-6]
SDO	J7[7-8]
SCLK	J7[9-10]
DRDYn	J7[11-12]
GPIO1	J7[13-14]
GPIO2/FAULT	J7[15-16]
GPIO3/OCCA	J7[17-18]
RESETn	J7[19-20]
GPIO4/OCCB	J7[21-22]
DGND	J7[23-24]

3.3 Clock Options

The ADS131B26-Q1 uses an internal oscillator by default after power-up. The internal oscillator frequency (f_{CLK}) has a nominal frequency of 8.192 MHz and serves as the primary timing reference for both analog and digital circuitry inside the device. The ADC modulator frequency (f_{MOD}) is equal to one-half the clock frequency ($f_{MOD} = f_{CLK} / 2$) and controls the timing of the input sample-and-hold switches inside each delta-sigma ADC modulator.

In addition to the internal oscillator, the EVM allows the user to provide an external clock to the ADS131B26-Q1 CLK pin. The user must also uninstall R71 and set DEVICE_CFG (4Ch) bit 12 = 1b when enabling the external clock source. The external clock signal can come from either:

1. The onboard crystal oscillator (Y1), which has a nominal frequency of 8.192 MHz.
2. An external clock source connected to the SMA connector (J10).

One advantage to using either external ADC clock option on the EVM is the ability to synchronize the DC/DC converter switching frequency with a null in the ADC digital sinc3 filter. For more information, see Section 4.1. Figure 3-1 shows a schematic of the external clock options.

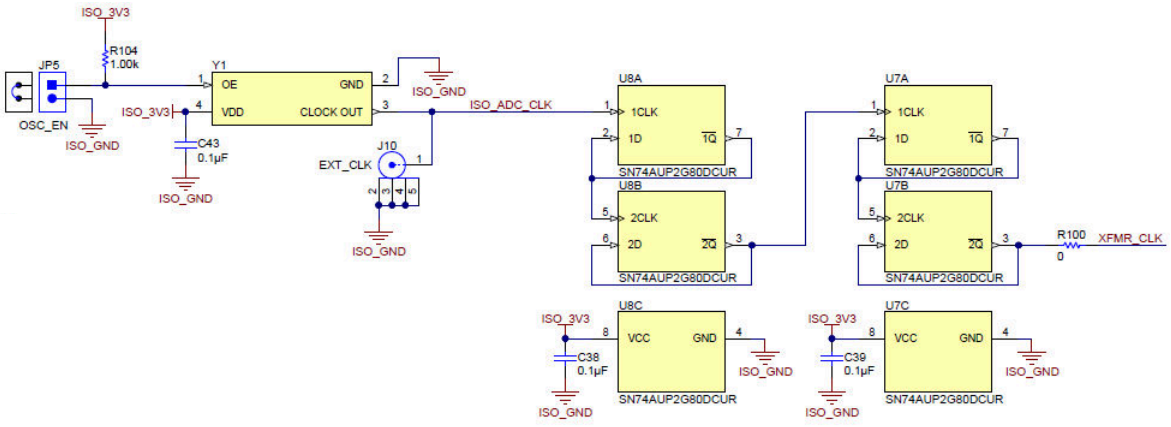


Figure 3-1. External ADC Clock Options (Schematic)

4 Power Supplies

This section details the EVM power supplies, ADC analog and digital supply options, and the PCB layout and decoupling guidelines.

4.1 DC/DC Converter Circuit

As mentioned previously in Section 1, power to the EVM can be supplied entirely by the PHI controller through connector J9. For information about the PHI pins and power connections, see Table 3-1.

A 3.3-V LDO output on the PHI (*ISO_3V3*) is used to power the controller side of the isolation barrier, including the digital isolators, onboard 8.192-MHz oscillator, and D flip-flop clock divider circuit. ISO_3V3 is also the default option to power the transformer driver (SN6505B-Q1, U6) and generate the supplies used on the ADC side of the isolation barrier. U6 can also be powered by the raw USB supply (*EVM_RAW_5V*) by uninstalling R96 and installing R97.

By default, the SN6505B-Q1 uses an internal 420-kHz clock to set the transformer switching frequency. This clock operates asynchronously to the ADS131B26-Q1 internal clock (CLK = 8.192 MHz). However, the EVM also supports an external ADC clock, which can be provided either by enabling the onboard oscillator (Y1) or by connecting a clock from an external source to the onboard SMA connector (J10). When an external clock is used for the ADC, this signal is divided by a factor of 16 using the dual D-type flip-flops (U7 and U8) and shared with the SN6505B-Q1 CLK input. The SN6505B-Q1 internally divides this clock input by another factor of 2, resulting in a transformer switching frequency that is synchronous with the ADC clock. Any remaining switching noise at the transformer output detected by the ADS131B26-Q1 aligns with a null in the ADC sinc3 digital filter response and be significantly attenuated. Figure 4-1 shows the DC/DC converter and transformer driver circuits.

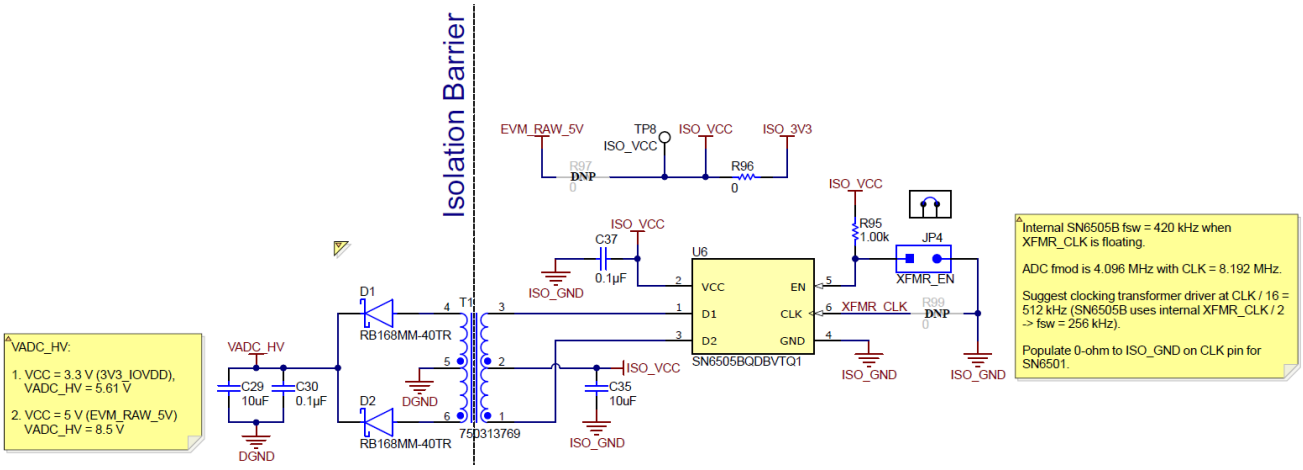


Figure 4-1. DC/DC Converter and Transformer Driver Circuit (Schematic)

4.2 ADC Power Supplies

The transformer output is connected to two rectification diodes (D1 and D2) to provide the main high-side supply voltage (*VADC_HV*). JP2 and JP3 connect *VADC_HV* to the ADC APWR and DPWR supply pins, respectively. The ADS131B26-Q1 uses two internal LDOs to generate the primary analog and digital supplies (*AVDD* and *IOVDD*). Series 0.1-ohm resistors (R57 and R66) are provided for LDO supply current measurements and are not required by the ADC for normal operation. When JP2 and JP3 are installed in the [2-3] position, *VADC_HV* is nominally approximately 5.1 V. To evaluate the ADS131B26-Q1 with an external APWR and DPWR supply, uninstall the jumpers on JP2 and JP3 and connect the external supply to the corresponding terminal block inputs (J6 and J8). Alternatively, the ADC internal LDOs can be completely bypassed by moving both JP2 and JP3 jumpers to the [1-2] position. In this configuration, APWR must be between 3 V and 3.6 V, and DPWR must be between 3 V and 5.5 V. Figure 4-2 shows the analog and digital ADC supply options.

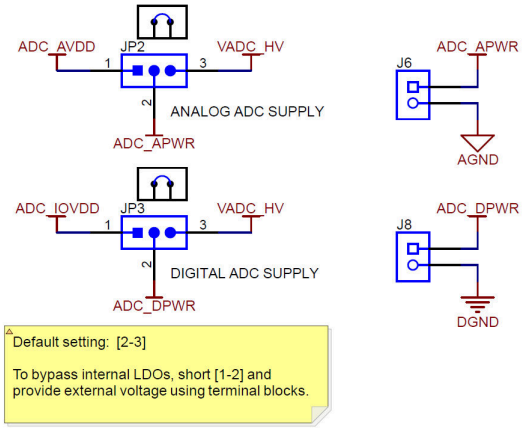


Figure 4-2. ADC Analog and Digital Supply Options (Schematic)

4.3 Power Supply and Voltage Reference Decoupling

The power supply and ADC voltage reference pins for the ADS131B26-Q1 are bypassed with ceramic capacitors placed close to the supply pins. Additionally, the EVM layout uses thick traces or large copper fill areas, where possible, between bypass capacitors and loads to minimize inductance along the load current path.

The EVM schematic lists the analog and digital grounds (*AGND* and *DGND*) as separate net names for the purpose of circuit illustration. However, these two nets are connected on the EVM by a net-tie on the bottom signal layer. Proper component placement and solid ground pours are important to make sure that the lowest noise and highest accuracy is used in any precision ADC application. See Section 7.2 for more suggested layout practices.

5 ADS131B26Q1EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed to properly operate the ADS131B26Q1EVM-PDK.

5.1 Default Jumper Settings

After unpacking, the EVM is configured with the default jumper settings. Figure 5-1 shows the locations for the default jumpers and Table 5-1 shows the functions of the default shunts.

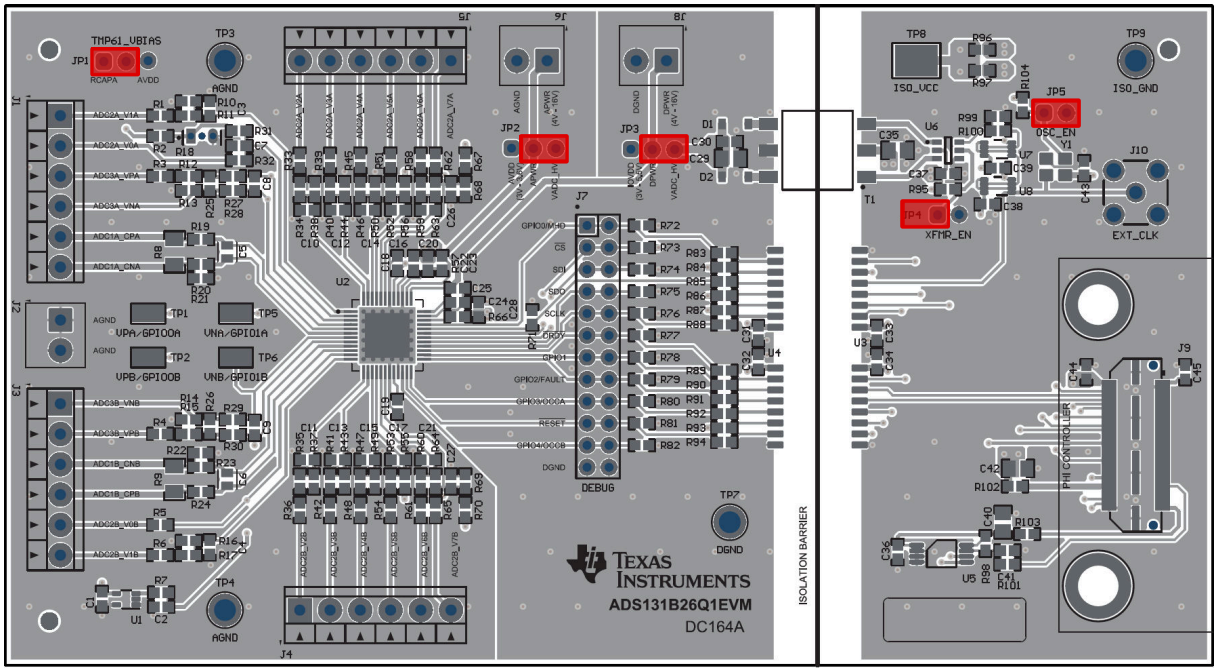


Figure 5-1. ADS131B26Q1-PDK Jumper Default Settings

Table 5-1. Default Jumper Settings

Designator	Position	Function
JP1	[1-2]	RCAPA is selected as bias voltage for the TMP61
JP2	[2-3]	Selects the transformer output as the APWR supply
JP3	[2-3]	Selects the transformer output as the DPWR supply
JP4	Not installed	The transformer driver is enabled
JP5	Installed	The onboard crystal oscillator is disabled

Table 5-2 lists the nominal voltages that result from the default configuration.

Table 5-2. Nominal Voltages: Default Configuration

Supply Name	Voltage
ISO_VCC	3.3 V
ISO_3V3	3.3 V
VADC_HV	5.1 V
APWR	5.1 V
DPWR	5.1 V
AVDD	3.3 V
DVDD	3.3 V
RCAPA	1.25 V
RCAPB	1.25 V

Note

Voltages are measured with respect to the local ground on the same side of the isolation barrier.

5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the *Tools and Software* folder of the ADS131B26Q1EVM-PDK and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Depending on the antivirus settings, an error message can appear and the executable file can be deleted.

Accept the license agreements and follow the on-screen instructions shown in Figure 5-2 to complete the installation.

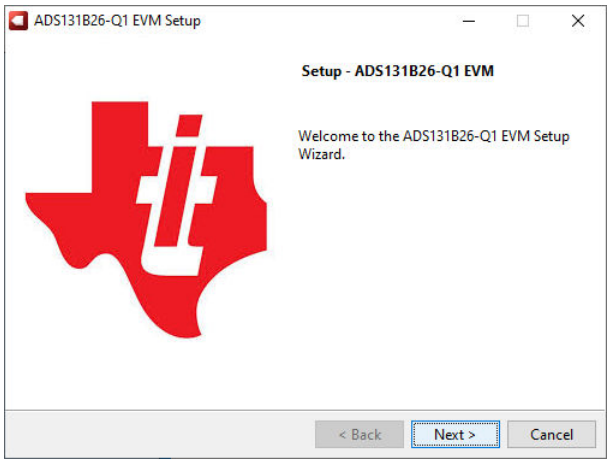


Figure 5-2. ADS131B26-Q1 Software Installation Prompt

As part of the ADS131B26-Q1 EVM GUI installation, a prompt with a device driver installation (as shown in Figure 5-3) appears on the screen. Click *Next* to proceed.

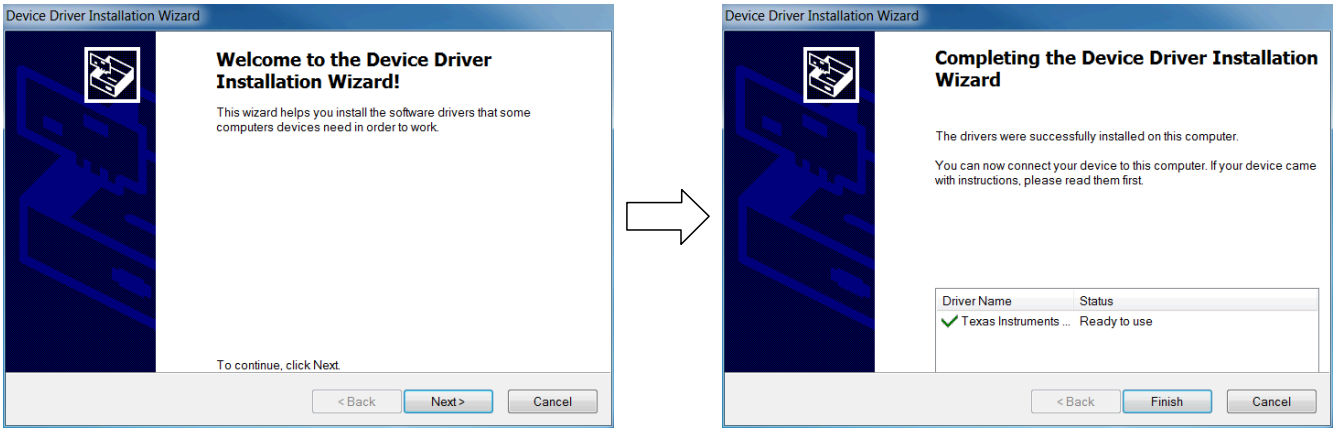


Figure 5-3. Device Driver Installation Wizard Prompts

Note

A notice can appear on the screen stating that Windows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

The ADS131B26Q1EVM-PDK requires the LabVIEW® run-time engine and can prompt for the installation of this software, as shown in Figure 5-4, if not already installed.

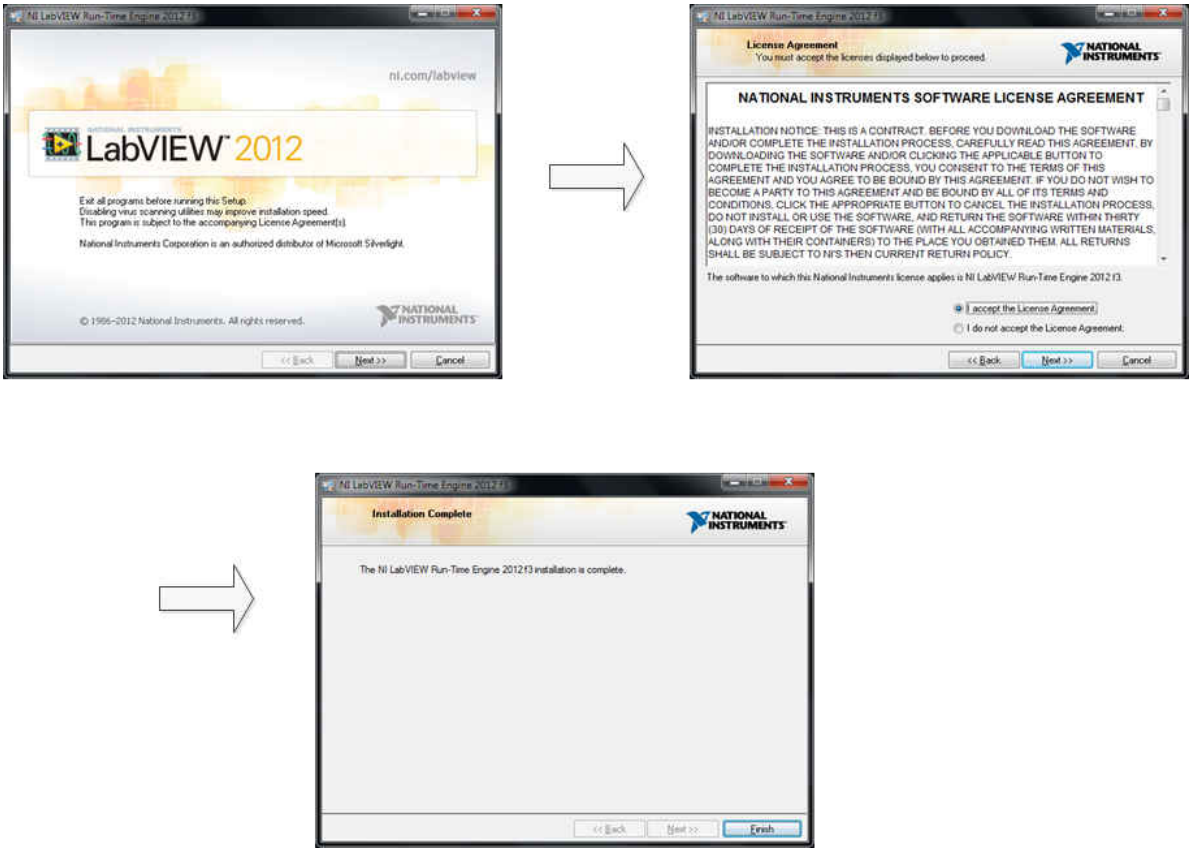


Figure 5-4. LabVIEW Run-Time Engine Installation

Verify that *C:\Program Files (x86)\Texas Instruments\ADS131B26Q1EVM-PDK* is available after these installations.

6 ADS131B26Q1EVM-PDK Software Reference

6.1 Global Settings for ADC Control

Figure 6-1 displays the default view of the ADS131B26-Q1 EVM GUI after start-up and successful connection to the EVM hardware. The EVM connection status can be verified by observing the green light indicator next to *HW Connected* at the bottom of the screen.

The *Pages* section at the top-left corner of the window lists the multiple register map controls and data analysis tools supported in this GUI. Section 6.2.1 through Section 6.2.3 detail the pages that configure the ADS131B26-Q1 register settings. Section 6.3.1 through Section 6.3.4 detail the pages that display and analyze the raw conversion data from the high-resolution, 24-bit ADC channels and the 16-bit sequencer ADC channels.

Below the *Pages* section is an abbreviated list of device commands, which execute the RESET, LOCK, and UNLOCK SPI op-codes. The RESET command restores the device register configuration to the power-on default settings. The LOCK command locks the interface to prevent unwanted commands from changing the state of the device. The UNLOCK command unlocks the interface to allow device configuration changes.

In the *Data Capture Configuration* section are basic settings and controls to initiate a data capture from the main ADC channels. *OSR13A* and *OSR13B* allow data rates to be configured for ADC1A, ADC1B, ADC3A, and ADC3B. *DRDYn Driving Source* selects which ADC channel generates the data-ready interrupt used for data collection. The *Samples* drop-down menu allows the user to choose from a pre-populated list of sample sizes or to enter a custom sample quantity. The number of samples are collected contiguously in a single data set when the **Capture** button is clicked from any of the analysis tool pages.

The *CLK Frequency (Hz)* and *Data Rate (SPS)* fields display the current clock frequency and ADC data rate based on the current OSR settings. If a target SCLK frequency (Hz) is specified, the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings.

The GUI is switched between hardware mode and simulation mode by checking and un-checking the *Connect to Hardware* box in the top-right area of the screen at any time.

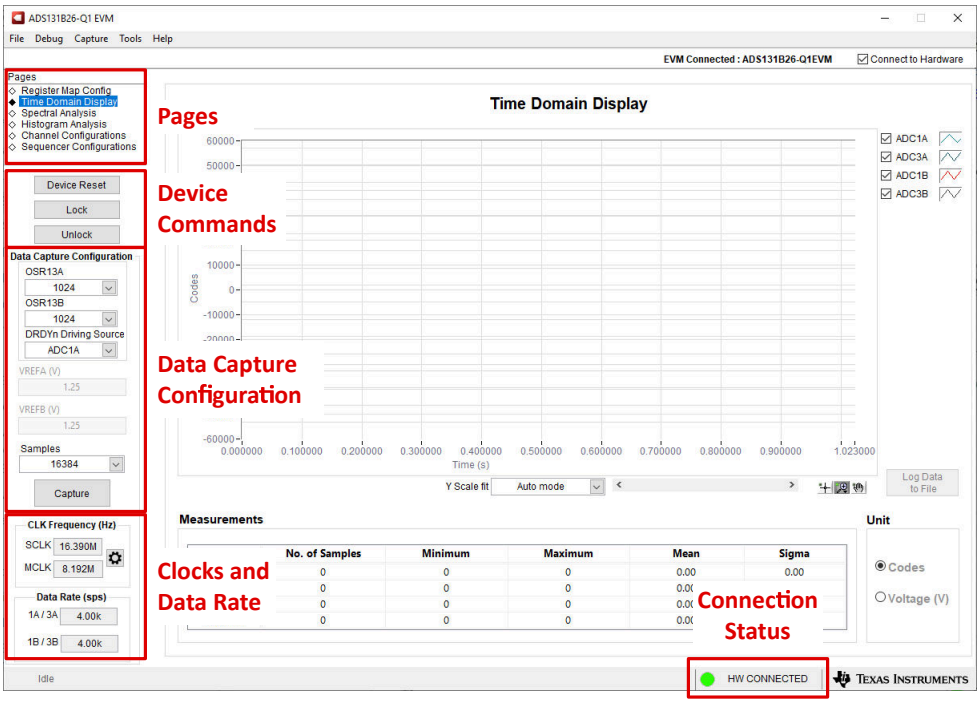


Figure 6-1. EVM GUI Global Input Parameters

6.2 Register Map Configuration

This section describes how to use the *Register Map Configuration* tools in the ADS131B26-Q1 EVM GUI. The GUI provides control over the device register settings via three pages:

1. *Register Map Config*: This page is the main register map configuration space in the GUI, which provides access to all device registers.
2. *Channel Configurations*: This page displays all register settings from multiple addresses that configure ADC1A, ADC1B, ADC3A, and ADC3B. The same register settings can also be configured in the main *Register Map Config* page.
3. *Sequencer Configurations*: This page displays all register settings from multiple addresses that configure ADC2A and ADC2B. The same register settings can also be configured in the main *Register Map Config* page.

6.2.1 Register Map Basics

The register map configuration tool (Figure 6-2) allows the user to view and modify the registers of the ADS131B26-Q1. This tool can be selected by clicking on *Register Map Config* under the *Pages* section of the left window pane. On power-up, the values on this page correspond to the ADC default register settings described in the ADS131B26-Q1 data sheet.

The *Register Map Configuration* tool has three distinct views that summarize the current register map configuration. At the top of the window is a tabular view where registers are listed in order of ascending hexadecimal address to display the *Register Name*, *Address*, *Default* value, *Mode* (R = Read-only, R/W = Read/Write), and register *Size*. To the right, the current register value is also displayed in both hexadecimal and binary formats. The register value can be modified either by entering the desired hexadecimal value in the *Value* column, or by clicking on the individual bits (read-only bits are listed in gray and cannot be edited).

Below the table is the *Field View* and *Register Description*. The *Field View* on the bottom-left lists the designated bit fields that are grouped together to configure a particular setting. Depending on the bit field, the current setting can be modified either by selecting the corresponding drop-down menu or entering the desired hexadecimal value. The *Register Description* view on the bottom-right describes the function and settings of the bit fields in the selected register, as described in the ADS131B26-Q1 data sheet.

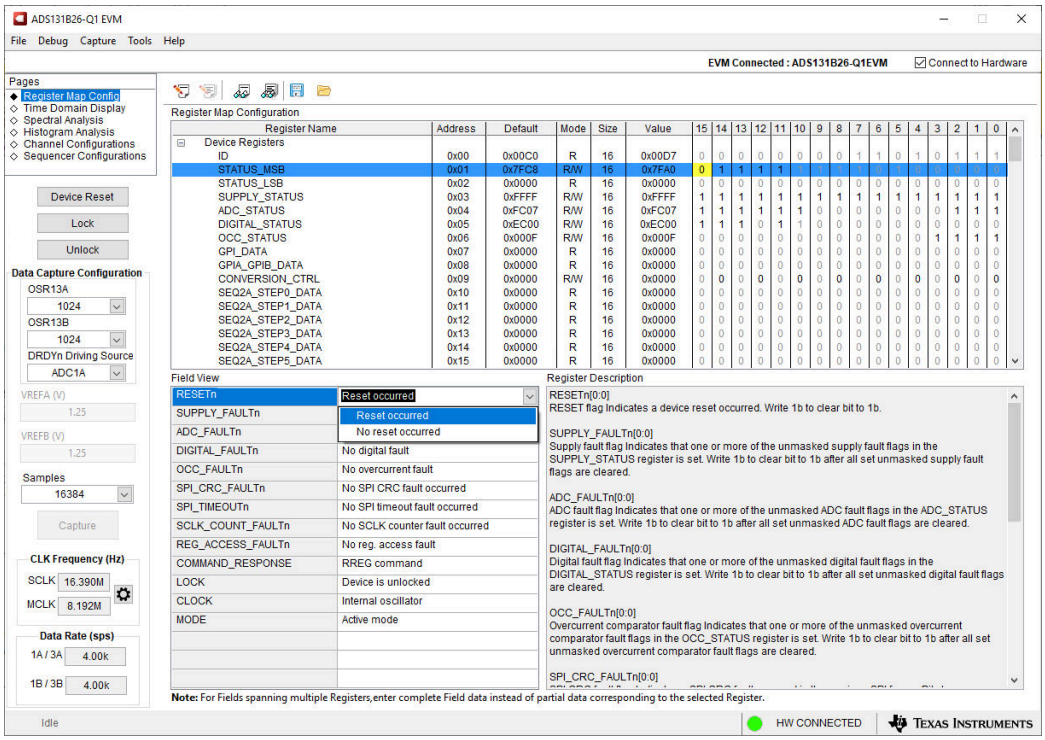


Figure 6-2. Register Map Configuration

6.2.2 ADC1A, ADC3A and ADC1B, ADC3B Configuration

Figure 6-3 displays the *Channel Configurations* register map page. These register controls allow the user to configure the register settings for ADC1A, ADC1B, ADC3A, and ADC3B in a more user-friendly interface.

The page is partitioned into ADC1A and ADC3A settings on the left and ADC1B and ADC3B settings on the right. At the top of each section are **Global Settings for ADC1A and ADC3A** and **Global Settings for ADC1B and ADC3B**, which contain the register settings from addresses 82h and C2h, respectively.

Below the global channel settings are individual ADC controls to figure the following settings:

- ADC enable
- Channel gain
- Channel Mux
- Current Source or Sink Mux
- Current Source or Sink Value
- Offset Calibration
- Gain Calibration

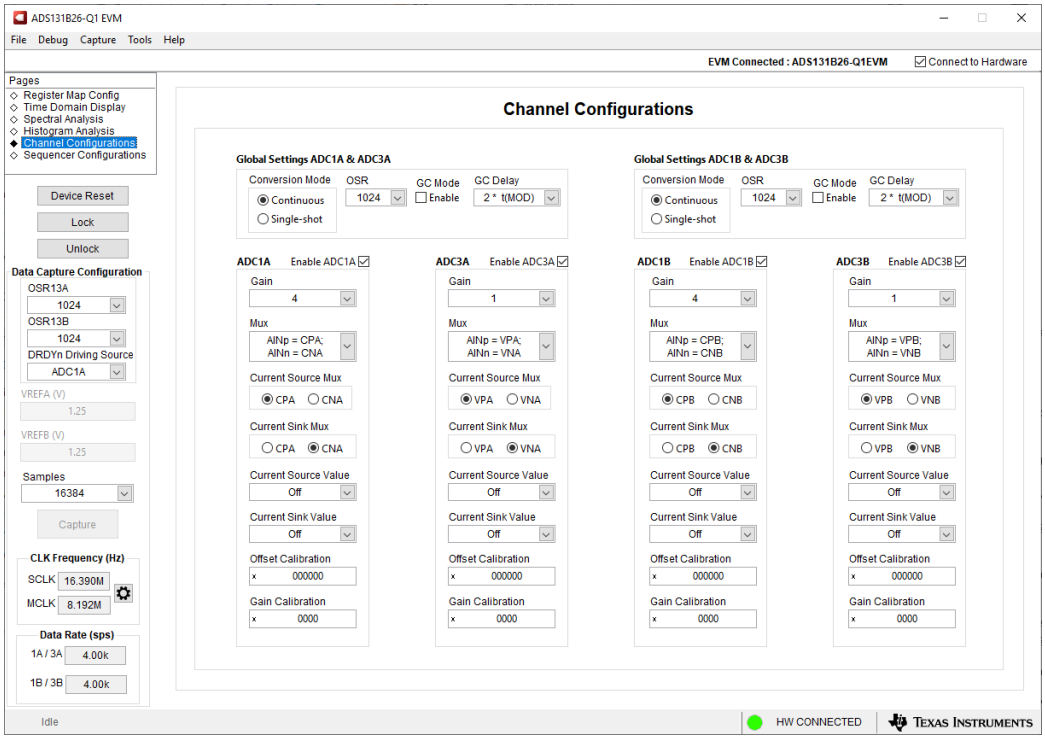


Figure 6-3. Channel Configurations Register Page

6.2.3 ADC2A and ADC2B Configuration

Figure 6-4 displays the *Sequencer Configurations* register map page. These register controls allow the register settings to be configured for ADC2A and ADC2B through a more user-friendly interface.

The page is partitioned into ADC2A settings on the left and ADC2B settings on the right. At the top of each section are *Global Settings for ADC2A* and *Global Settings for ADC2B*, which contain the register settings from addresses 8Bh and CBh, respectively.

Below the global channel settings are *ADC2A Steps Configurations* and *ADC2B Steps Configurations* to configure each of the individual sequencer steps. Steps 0 through 7 are displayed on the page by default, and steps 8 through 15 can be displayed by selecting the corresponding tab on the bottom of each section. Each step allows the following settings to be configured:

- Sequence step enable
- Gain
- Negative input
- Positive input

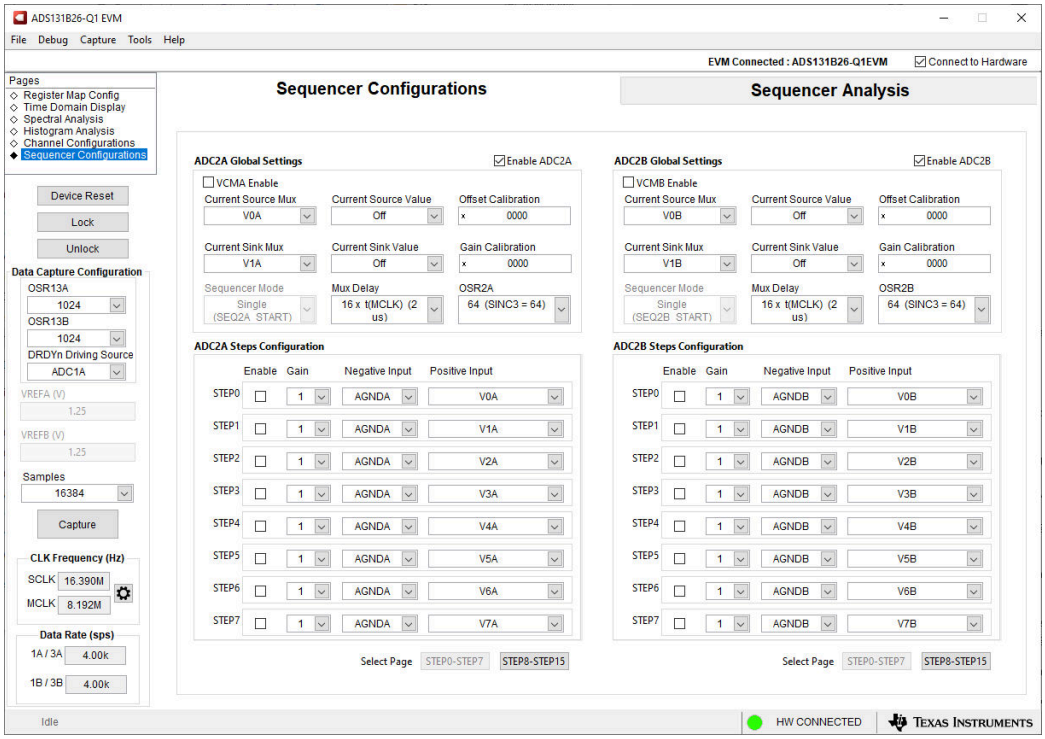


Figure 6-4. Sequencer Configurations Register Page

6.3 Analysis Tools

This section describes the analysis tools included with the ADS131B26Q1EVM-PDK GUI. These tools include Time Domain Display, Spectral Analysis, Histogram Analysis, and Sequencer Analysis. Section 6.3.1 through Section 6.3.3 describe the data collection and analysis features of the ADS131B26-Q1 EVM GUI.

6.3.1 Time Domain Display

The *Time Domain Display* tool allows visualization of the ADC conversion data for ADC1A, ADC1B, ADC3A, and ADC3B. This tool is useful for both studying the circuit behavior and debugging any gross problems with the ADC or input source.

The *Data Capture Configuration* panel on the left side of the window allows the user to independently specify the oversampling ratio (OSR) used by ADC1A, ADC3A and ADC1B, ADC3B by configuring OSR13A and OSR13B, respectively. In addition, ADC1A or ADC1B can be selected as the driving channel source to generate the DRDYn interrupt. If the data rates differ, and the faster channel is selected as the DRDYn driving source, the GUI collects data until the faster channel reaches the specified number of samples. In this case, the slower channel ends up with fewer samples than specified. If the slower channel is selected as the DRDYn driving source, the GUI collects the specified number of samples for all channels, but some conversion data are missed from the faster channels, reducing the effective data rate.

Initiate a data capture by specifying the number of samples and clicking the **Capture** button at the bottom of the *Data Capture Configuration* panel. The raw ADC conversion data is then displayed on the graph with a statistical summary of each channel in the *Measurements* table below the plot. The **Units** radio buttons configure the plot y-axis and the summary table results as either *Codes* or *Voltage (V)*. When *Voltage (V)* is selected, the values are input-referred based on the channel gain setting. Figure 6-5 shows an example of the *Time Domain Display* window and relevant controls. Switching pages to any of the other *Analysis* tools described in the subsequent sections exports the same data for viewing without having to recollect the data.

Figure 6-5. Time Domain Display Tool

6.3.2 Spectral Analysis Tool

The *Spectral Analysis* tool is intended to evaluate the dynamic performance of ADC1A, ADC3A, ADC1B, and ADC3B. This tool analyzes the AC characteristics of the ADC and input signal source.

The *Data Capture Configuration* panel on the left side of the window allows the user to independently specify the oversampling ratio (OSR) used by ADC1A, ADC3A and ADC1B, ADC3B by configuring OSR13A and OSR13B, respectively. Even though the resulting data rates can differ, the resulting fast-fourier transform (FFT) always plots from DC to one-half the data rate for each channel. Therefore, one channel FFT plot can easily occupy less of the x-axis than the other.

The *Measurements* summary table above the FFT plot is updated based on the *Display Channel* drop-down menu selection. The calculated specifications include SNR, THD, SFDR, SINAD, and ENOB. The GUI also identifies the frequency and signal power of the fundamental component of the input signal, and the frequency and signal power of the largest spur component.

Under the *Configuration* section, select the number of harmonics used for distortion calculations (default = 9 harmonics) and specify the windowing function required to mitigate the effects of non-coherent sampling. The *7-Term Blackman-Harris* window is the default option and has sufficient dynamic range to resolve the frequency components of a 24-bit ADC. The *None* option corresponds to not using a window (or using a rectangular window) and is not recommended. Both the calculated specifications and the FFT plot can be displayed in dBc or dBFS units by toggling the radio buttons beneath the *Display Channel* drop-down menu.

Figure 6-6 shows the *Spectral Analysis Tool* window. Initiate a data capture by specifying the number of samples and clicking the **Capture** button at the bottom of the *Data Capture Configuration* panel. In the example below, ADC3A is configured for 64 kSPS (OSR13A = 64) and is measuring a 2-kHz single-ended sine wave, producing a –6.26 dBFS input signal. The resulting FFT is plotted from DC to 32 kHz. For fully-differential inputs, restrict the input signal amplitude to –0.5 dBFS maximum (approximately 95% of full-scale) to avoid saturating the ADC channels and introducing unwanted distortion terms into the signal. ADC3B is configured to measure an internal short to AGNDB at 32 kSPS (OSR13B = 128). As a result, the noise floor of ADC13B is only plotted from DC to 16 kHz.

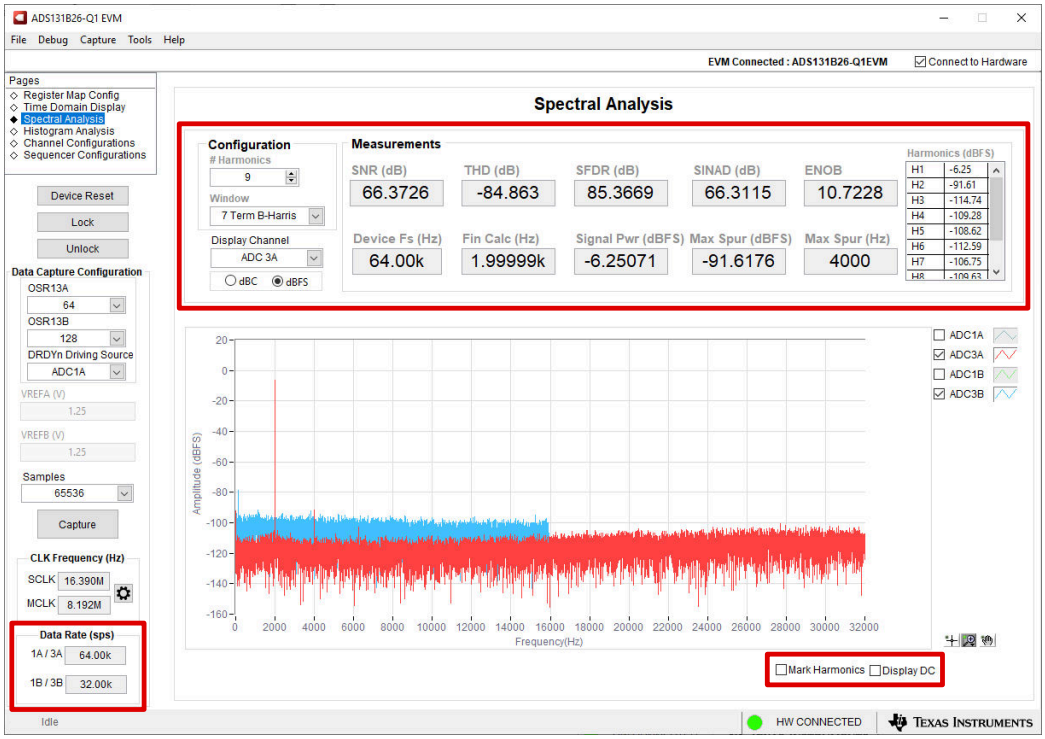


Figure 6-6. Spectral Analysis Tool

6.3.3 Histogram Analysis

The *Histogram Analysis* tool plots the histogram of the raw ADC conversion data for ADC1A, ADC1B, ADC3A, and ADC3B. This tool is useful for studying the statistical summary of the data set, mainly by computing the mean and standard deviation of the data from each channel. Noise degrades ADC resolution and the histogram tool can estimate an effective resolution, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram bin width is calculated using Scott's Rule by default. This method minimizes the mean-squared error in the bin approximation, assuming the data follows a Gaussian distribution. Alternatively, select *Custom* under the *Binning Rule* drop-down menu and enter the desired *Codes per Bin* setting in the field to the right.

Below the histogram plot is a *Measurements* summary table, which lists the *Minimum*, *Maximum*, *Sigma*, *Peak-to-Peak*, and *Number of Bins* for each channel. The histogram x-axis and the table statistics can be displayed in *Codes* or *Voltage (V)* by toggling the radio buttons under the *Unit* section to the right of the table.

Initiate data capture by specifying the number of samples and clicking the **Capture** button at the bottom of the *Data Capture Configuration* panel. Figure 6-7 shows an example data capture with all channels configured for an internal input short. ADC1A and ADC1B are configured for Gain = 4, and ADC3A and ADC3B are configured for Gain = 1.

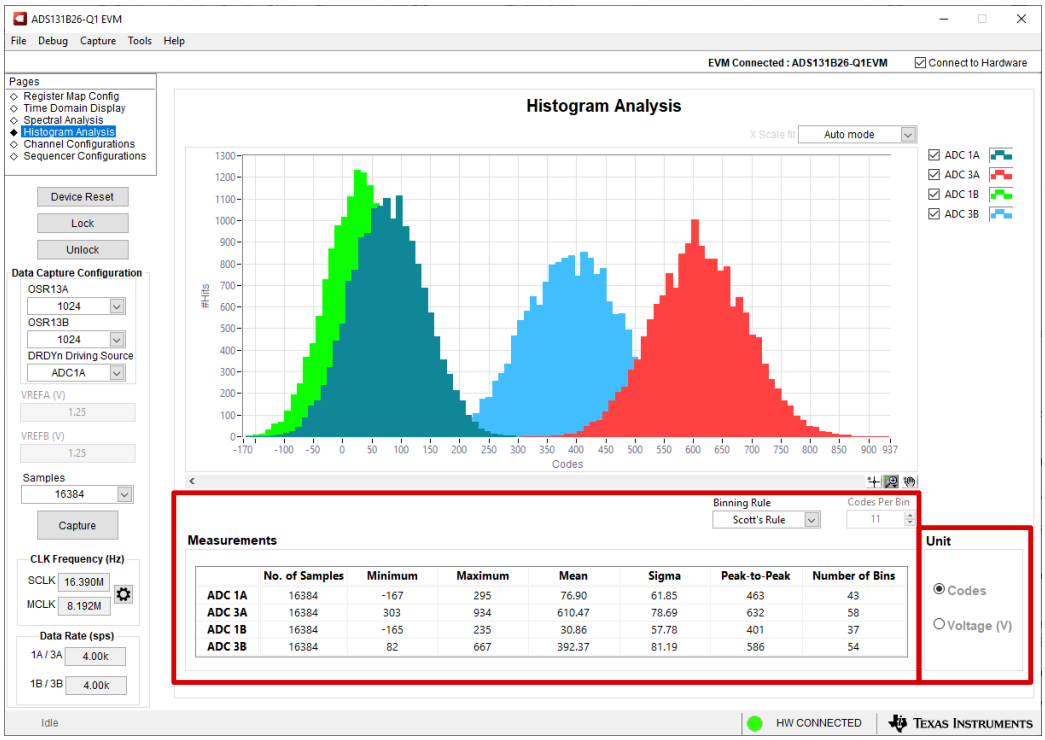


Figure 6-7. Histogram Analysis Tool

6.3.4 Sequencer Analysis

The *Sequencer Analysis* tool displays the raw ADC conversion data for ADC2A and ADC2B. This tool can be accessed by selecting the *Sequencer Configurations* page from the top-left side of the GUI window. This page defaults to the *Sequencer Configurations* tab explained in Section 6.2.3. When the sequencer steps are enabled and configured, select the right tab at the top of the window to access the *Sequencer Analysis* display.

From the *Sequencer Analysis* page, initiate a data capture by specifying the desired number of sequencer iterations in the *Samples* drop-down menu and clicking the **Capture** button on the left side of the window. This button collects the specified number of samples from each sequencer step that is enabled. The GUI uses Sequencer Mode 01b, which initiates a new sequence of measurements after each DRDYn falling edge. For demonstration purposes, the GUI configures ADC1A and ADC1B to use the highest OSR setting, which produces the minimum data rate and allows the maximum time for each sequence to complete.

The sequencer results are plotted by the *Iteration* number on the x-axis of the graph. Each enabled sequence step is automatically enabled for display, but the user can deselect any plot by unchecking the box next to the sequence step in the legend on the right side. Below the plot is a *Results* summary table, which lists the results from each step and each sequence iteration. The results in the plot and summary table can be displayed in either *Codes* or *Voltage (V)* by using the radio buttons on the bottom-right. Figure 6-8 shows an example sequencer data capture.

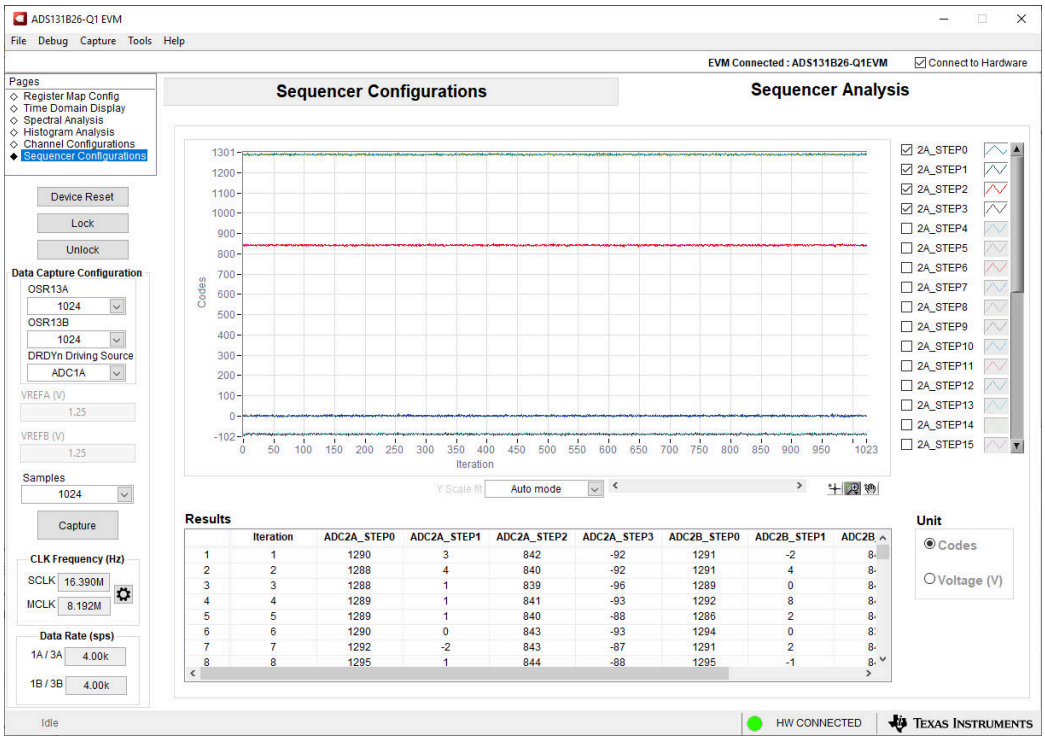


Figure 6-8. Sequencer Analysis Tool

7 ADS131B26Q1EVM-PDK Bill of Materials, PCB Layout, and Schematics

7.1 Bill of Materials (BOM)

Table 7-1 lists the ADS131B26Q1EVM-PDK bill of materials.

Table 7-1. ADS131B26Q1EVM-PDK Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C1	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 10%, X7R, 0603	603	C0603X103K5RACTU	Kemet		
C2, C3, C4, C7, C10, C11, C12, C13, C14, C15, C16, C17, C20, C21	14	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	603	C0603C104J3RACTU	Kemet		
C5, C6	2	47 nF	0.047 µF ±1% 16 V Ceramic Capacitor C0G, NP0 0805 (2012 Metric)	805	C0805C473F4GAC7800	Kemet		
C8, C9	2	2200 pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	603	GRM1885C1H222JA01D	MuRata		
C18, C19, C22, C23, C25, C28, C44, C45	8	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	603	C0603C105K3RACTU	Kemet		
C24	1	0.22uF	CAP, CERM, 0.22 uF, 25 V, +/- 5%, X7R, 0603	603	C0603C224J3RAC7867	Kemet		
C29, C35, C40, C42	4	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X5R, 0805	805	GRM21BR61E106KA73L	MuRata		
C30, C31, C32, C33, C34, C37, C38, C39, C43	9	0.1uF	CAP, CERM, 0.1 µF, 25 V,+/- 10%, X5R, 0603	603	CL10A104KA8NNNC	Samsung Electro-Mechanics		
C36, C41	2	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	603	06033C104JAT2A	AVX		
D1, D2	2		DIODE SCHOTTKY 40 V 1 A PMDU	SOD-123FL-2	RB168MM-40TR	Rohm		
H1, H2	2		ROUND STANDOFF M3 STEEL 5 MM	ROUND STANDOFF M3 STEEL 5 MM	9774050360R	Wurth Elektronik		
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
H7, H8	2		Machine Screw Pan PHILLIPS M3		RM3X4MM 2701	APM HEXSEAL		
J1, J3, J4, J5	4		Terminal Block, 3.5mm Pitch, 6x1, TH	20.5x8.2x6.5mm	ED555/6DS	On-Shore Technology		
J2, J6, J8	3		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5 mm	ED555/2DS	On-Shore Technology		

Table 7-1. ADS131B26Q1EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J7	1		Header, 100mil, 12x2, Gold, TH	12x2 Header	TSW-112-07-G-D	Samtec		
J9	1		Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Header (Shrouded), 19.7mil, 30x2, SMT	QTH-030-01-L-D-A	Samtec		
J10	1		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
JP1, JP2, JP3	3		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
JP4, JP5	2		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
R1, R6, R11, R17, R33, R34, R35, R36	8	10.5k	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K5FKEA	Vishay-Dale		
R2	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RCG060310K0FKEA	Vishay Draloric		
R3, R4, R12, R15, R39, R40, R41, R42, R45, R46, R47, R48	12	30.9k	RES, 30.9 k, 1%, 0.1 W, 0603	603	RC0603FR-0730K9L	Yageo		
R7	1	1.50k	RES, 1.50 k, 1%, 0.1 W, 0603	603	RC0603FR-071K5L	Yageo		
R8, R9	2	100	RES, 100, 0.1%, 1 W, AEC-Q200 Grade 0, 1206	1206	HRG3216P-1000-B-T1	Susumu Co Ltd		
R10, R16, R37, R38	4	3.00k	RES, 3.00 k, 1%, 0.1 W, 0603	603	RC0603FR-073KL	Yageo		
R13, R14, R21, R22, R27, R28, R29, R30, R31	9	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	RMCF0603ZT0R00	Stackpole Electronics Inc		
R18	1	10k	PTC Thermistor 10 kOhms TO-226-2, TO-92-2 (TO-226AC) Short Body	TO92	TMP6131QLPGMQ1	Texas Instruments		
R19, R20, R23, R24	4	100	RES, 100, 1%, 0.1 W, 0603	603	RC0603FR-07100RL	Yageo		
R25, R26, R43, R44, R49, R50, R55, R56, R63, R64	10	1.96k	RES, 1.96 k, 1%, 0.1 W, 0603	603	RC0603FR-071K96L	Yageo		
R51, R52, R53, R54, R58, R59, R60, R61	8	13.7k	RES, 13.7 k, 1%, 0.1 W, 0603	603	RC0603FR-0713K7L	Yageo		

Table 7-1. ADS131B26Q1EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R57, R66	2	0.1	RES, 0.1, 5%, 0.1 W, 0603	603	CRL0603-JW-R100ELF	Bourns		
R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82	11	100k	RES, 100 k, 1%, 0.1 W, 0603	603	RC0603FR-07100KL	Yageo		
R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94	12	33	RES, 33.0, 1%, 0.1 W, 0603	603	RC0603FR-0733RL	Yageo		
R95, R104	2	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	603	RC0603FR-071KL	Yageo		
R96, R100, R101, R102, R103	5	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	ERJ-3GEY0R00V	Panasonic		
R98	1	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	603	CRCW060310K0JNEA	Vishay-Dale		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	5	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
T1	1	340uH	Transformer, 340uH, SMT	Transformer, 8x7.62x9.14 mm	750313769	Wurth Elektronik		
TP1, TP2, TP5, TP6	4		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone		
TP3, TP4, TP7, TP9	4		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone		
TP8	1		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		Automotive Grade, 1.5V-Capable,10 uA Analog Output Temperature Sensor, DCK0005A (SOT-SC70-5)	DCK0005A	LMT84QDCKRQ1	Texas Instruments	LMT84QDCKTQ1	Texas Instruments
U2	1		Automotive Current, Voltage and Temperature Measurement Analog Front-End for Battery Management Systems	HTQFP48	ADS131B26QPHPRQ1	Texas Instruments		
U3	1		Automotive, High Speed, Robust EMC Six-Channel Digital Isolators, DW0016B (SOIC-16)	DW0016B	ISO7762FQDWQ1	Texas Instruments	ISO7762FQDWRQ1	Texas Instruments

Table 7-1. ADS131B26Q1EVM-PDK Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U4	1		High Speed, Robust EMC, Reinforced Six-Channel Digital Isolator, DW0016B (SOIC-16)	DW0016B	ISO7761FQDWQ1	Texas Instruments	ISO7761DW	Texas Instruments
U5	1		I2C BUS EEPROM (2-Wire), TSSOP-B8	TSSOP-8	BR24G32FVT-3AGE2	Rohm		
U6	1		Transformer Driver PMIC SOT-23-6	SOT-23-6	SN6505BQDBVTQ1	Texas Instruments		
U7, U8	2		Low-Power Dual Positive-Edge-Triggered D-Type Flip-Flop, DCU0008A (VSSOP-8)	DCU0008A	SN74AUP2G80DCUR	Texas Instruments		
Y1	1		Oscillator, 8.192 MHz, 15 pF, AEC-Q200 Grade 1, SMD	3.2x2.5mm	SIT8924BA-22-33E-8.192000G	SiTime		

7.2 PCB Layout

Figure 7-1 through Figure 7-6 show the ADS131B26Q1EVM-PDK PCB layout.

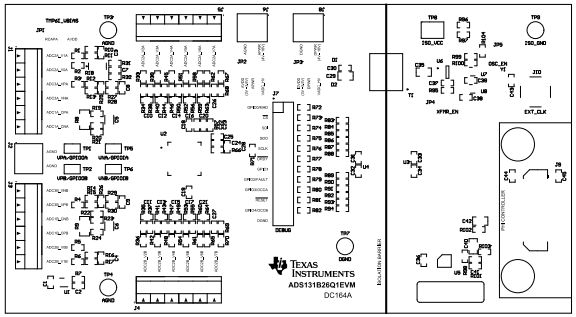


Figure 7-1. Top Silkscreen

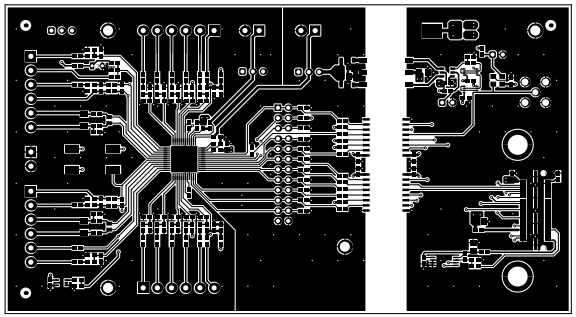


Figure 7-2. Top Layer

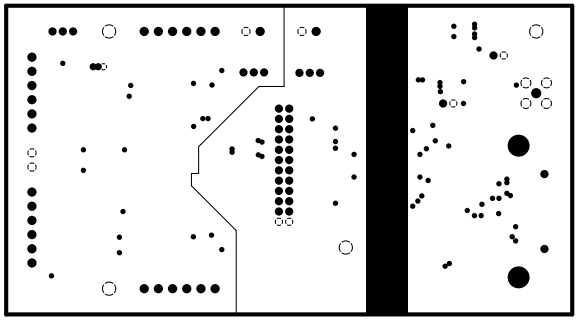


Figure 7-3. Ground Layer

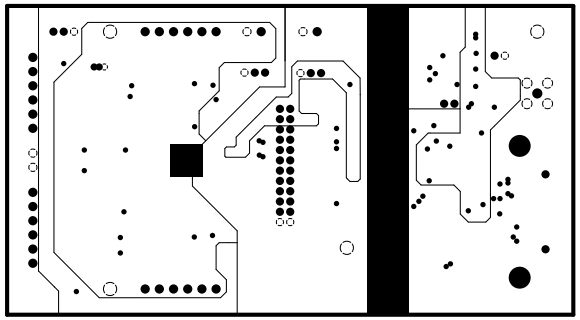


Figure 7-4. Power Layer

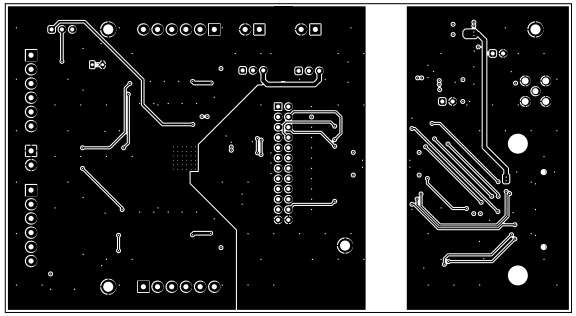


Figure 7-5. Bottom Layer

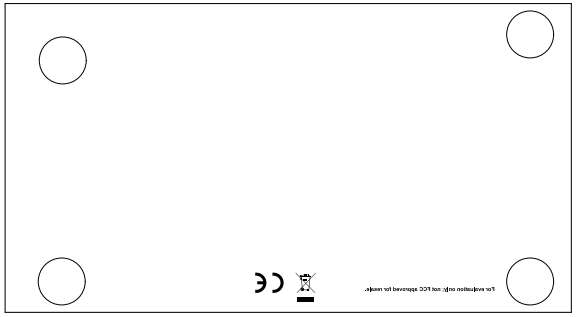


Figure 7-6. Bottom Silkscreen

7.3 Schematics

Figure 7-7 and Figure 7-8 contain the schematics for the ADS131B26Q1EVM-PDK.

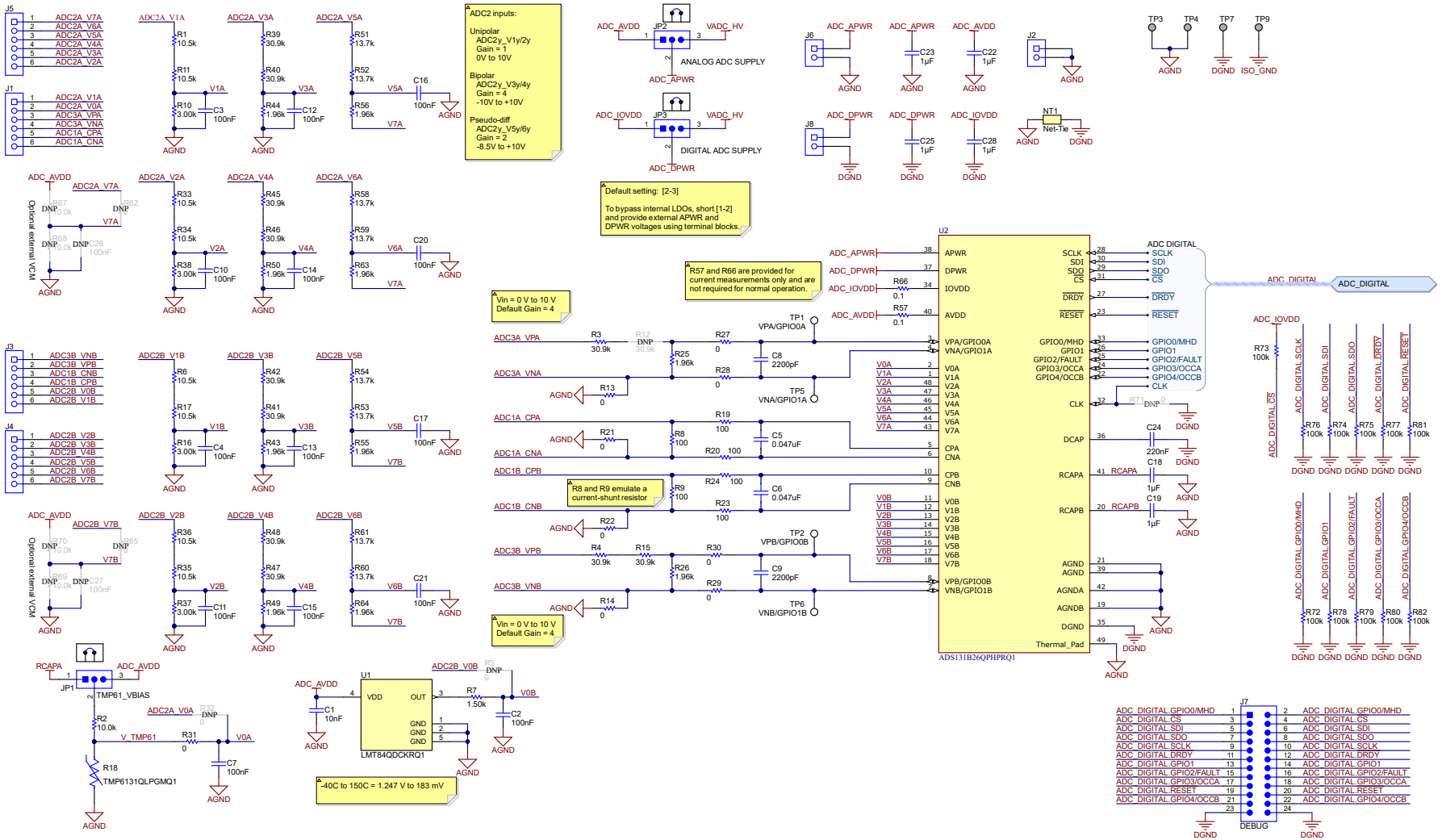


Figure 7-7. Analog Inputs, ADC Power, and Interface Connections

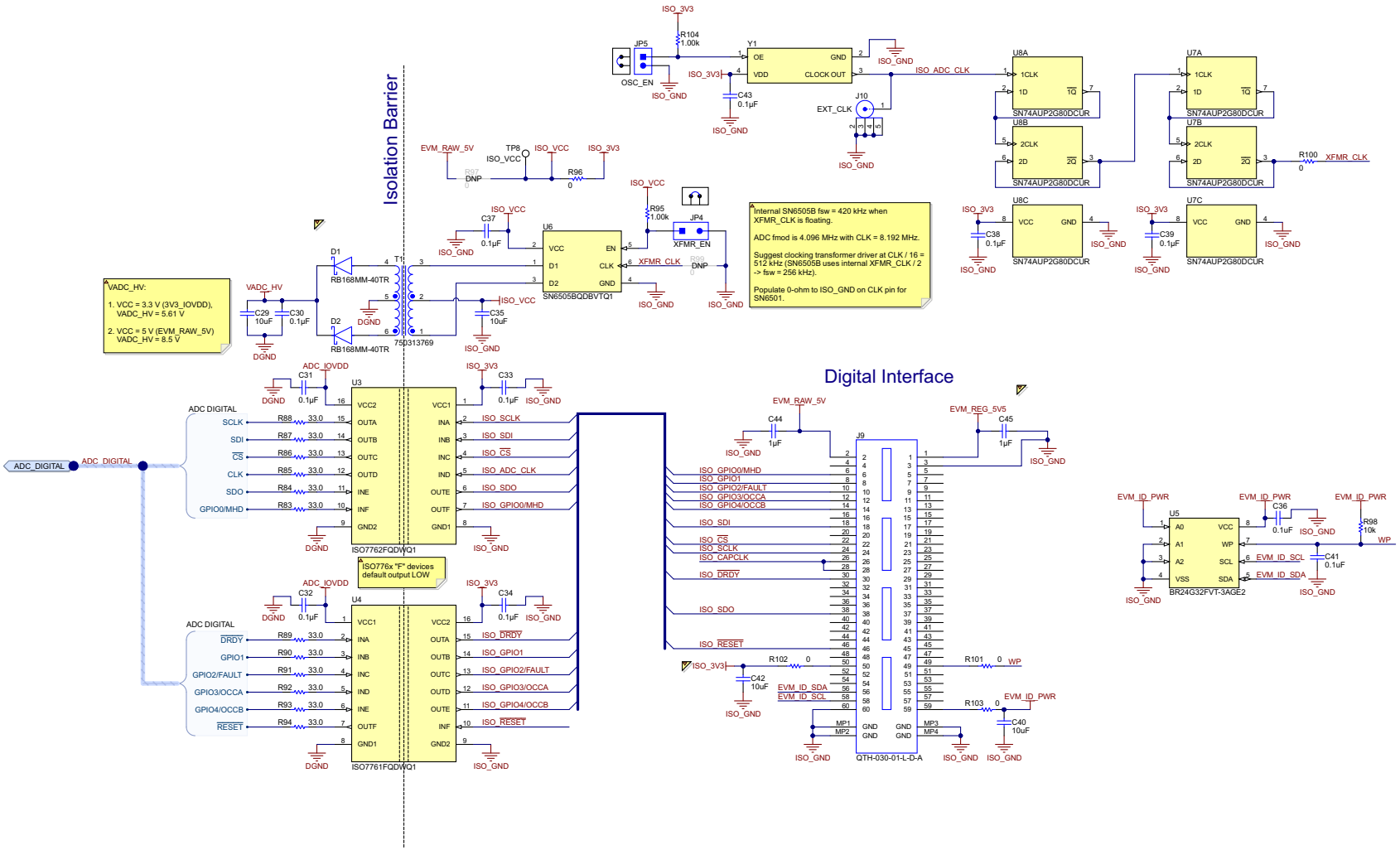
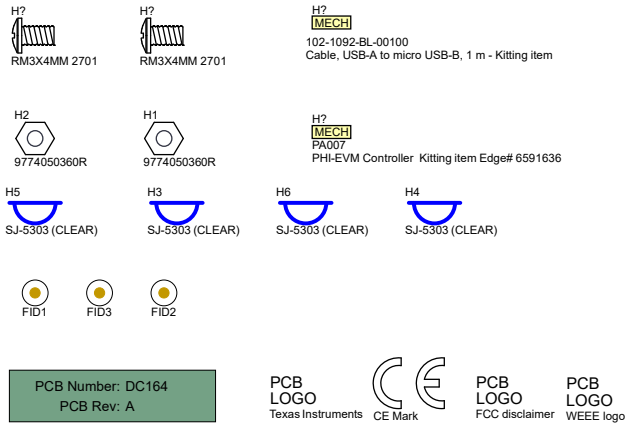


Figure 7-8. Digital Isolators, DC/DC Power Supply, External Clock, and PHI Controller



LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

Variant/Label Table	
Variant	Label Text
001	ADS131B26Q1EVM-PDK

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Figure 7-9. Hardware, Logos, Miscellaneous

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2022) to Revision A (May 2023)	Page
• Added text to specify which configurations are needed for an external clock source to the ADC CLK pin	10
• Added text to clarify when to use R57 and R66	12
• Changed Figure 7-7 and added Figure 7-9 to *Schematics* section	29

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NOTE:

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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