EVM User's Guide: ADC3683EVMCVAL ADC36xxEVMCVAL Evaluation Module

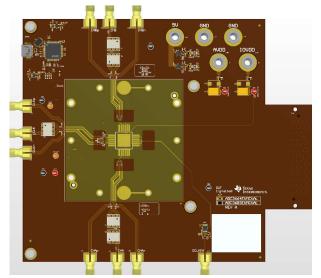


Description

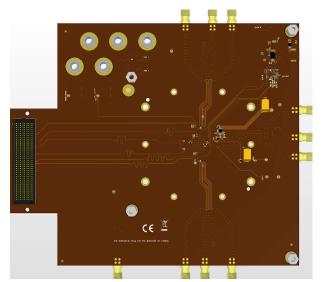
The ADC36xxEVMCVAL is an evaluation board used to evaluate the ADC36XXQML-SP analog-todigital converter (ADC) from Texas Instruments. The ADC36XXQML-SP uses a serial LVDS interface to output the digital data. The serialized LVDS interface supports output rates up to 1Gbps. The ADC36XXQML-SP can be operated in *oversampling* + *decimating* mode using the internal decimation filter to improve the dynamic range and relax external antialiasing filter.

Features

- Transformer coupled or single-ended clock inputs
- Transformer coupled or single-ended analog inputs
- FMC connector
- Single 5 V power supply jack for easy power-up
- REF35160QDBVR Precision Voltage Reference for the ADC 1.6 V external reference
- REFBUF test point provides a hardware option to change the voltage reference



ADC36xxEVMCVAL (Top View)



ADC36xxEVMCVAL (Bottom View)



1 Evaluation Module Overview

1.1 Introduction

This user's guide describes the characteristics, operation, and use of the ADC36xxEVMCVAL and discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADC36xxEVMCVAL. In the following sections of this document, the ADC36xxEVMCVAL evaluation board is referred to as the EVM and the ADC36XXQML-SP devices are referred to as the ADC devices, respectively. This document applies only to the ADC3683EVMCVAL and ADC3664EVMCVAL.

By default, the EVM is configured to receive external inputs for the sampling clock and analog input via ACcoupled, transformer (balun) inputs. These transformers perform single-ended to differential conversion, and provide a low noise/distortion passive input.

To exercise the full performance capabilities of this high performance successive approximation (SAR) ADC, TI recommends to evaluate the ADC in the default configuration, and then evaluate in other configurations, as needed.

1.2 Kit Contents

- ADC36xxEVMCVAL
- Mini-USB cable

1.3 Specification

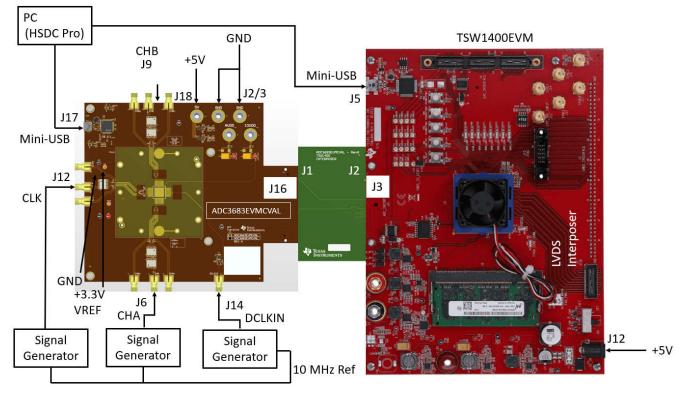
The ADC36xxEVMCVAL receives power from the 5 V jack at J18, which is then converted to +1.8 VDC for AVDD and +1.8 VDC for DVDD. This conversion happens by way of two ultra-low noise, ultra-high PSRR, low-dropout regulators, TPS7A9401DSC. USB-to-SPI communication is established using the FTDI (FT4232HL-REEL). The ADC clocks are supplied externally. The default configuration is to input the device clock (CLK) single-ended into J12 and the data clock (DCLK) single-ended into J14 (high quality external clocks are used to achieve best AC performance). The analog inputs by default are supplied through J6 for channel A and J9 for channel B where the signal is AC coupled through the baluns (ADT4-1WT). The analog input full-scale is 3.2 V_{pp}. The analog input is driven at -1 dBFs (approximately 2.8 V_{pp}) in all examples in this user's guide.

The ADC36XXQML-SP family has a +1.6 V voltage reference (VREF) that can be supplied internally or externally. By default, the EVM is configured to supply an external voltage reference using REF35160QDBVR Precision Voltage Reference which is supplied using the VREF test point and 3.3 V supply. At any time, the reference can be changed to internal via SPI write.

The ADC36XXQML-SP family uses an unbuffered analog input, so a glitch filter is required to attenuate the ADC sampling glitch from when the sampling capacitors switch (sample/hold). The glitch filter acts as a low pass filter with a corner frequency (F_c) at 30 MHz (accepts DC to 30 MHz).

The ADC36xxEVMCVAL LVDS output data is routed to an FMC connector, and then connected to an LVDS Interposer card. This interposer card then maps to the HSMC connector of the TSW1400EVM to capture the ADC36xxEVMCVAL SLVDS clock and data signals.







1.4 Device Information

Table 1-1. Devices on ADC36xxEVMCVAL

Part Name	Description	Function
TPS7A9401DSC	Ultra-low noise, ultra-high psrr, low-dropout regulator	Drop down the 5 V input to 1.8 V AVDD and 1.8 V DVDD
TLV702	Low-I _Q , low-dropout regulator	Drop down the 5 V from mini-USB cable to 3.3 V and 1.8 V for FTDI circuits
ADT4-1WT+	RF transformer	Converts single ended clock and input signals to differential signals
SN65LVDS100DGKR	Differential translator/repeater	Converts single ended DCLKIN signal to differential signal
REF35160QDBVR	Ultra low-power, high-precision voltage reference	Supplies external voltage reference of 1.6 V to the ADC for external reference mode
SN74AVC4T774RSV	Dual supply bus transceiver with configurable voltage-level shifting	Level shifters in FTDI circuits
FT4232HL	Quad high speed USB to multipurpose UART/ MPSSE IC	FTDI chip
93LC46B	Serial EEPROM	FTDI circuit
UX60SC-MB-5S8	Mini-USB connector	Surface mount Mini-USB connector



2 Software

2.1 Software Description

The required software to test this EVM includes HSDC Pro and ADC35XX EVM GUI. HSDC Pro is TI's data capture GUI that is compatible with the TSW1400EVM. ADC35XX EVM GUI is the GUI that allows easy configuration of the device.

2.2 Software Installation

HSDC Pro software can be found using the following link: HSDC Pro.

Once downloaded, launch the executable and accept the default installation process.

2.3 GUI Installation

ADC35XX EVM GUI download can be found using the following link, under the *Related Design Sources* tab: ADC35XX EVM GUI.

Once downloaded, extract and run the executable file and accept the default installation options.



3 Hardware

3.1 Additional Images

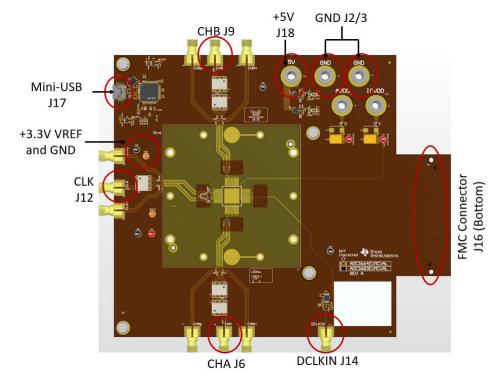


Figure 3-1. ADC36xxEVMCVAL Features Identification (Top)

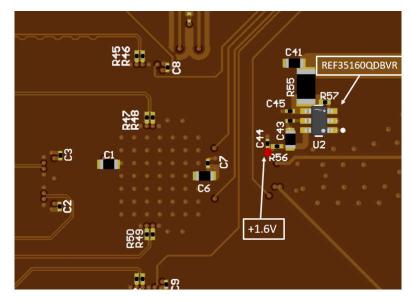
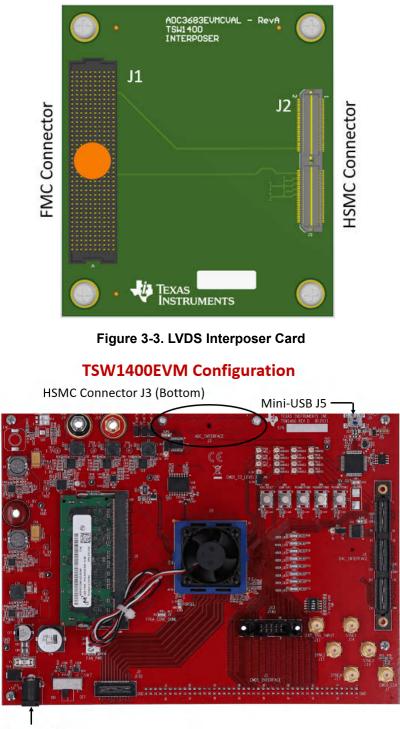


Figure 3-2. ADC36xxEVMCVAL Features Identification (Bottom)



ADC3683_TSW1400_Interposer_RevA



J12: 5V, 4A



3.2 Power Requirements

The default power configuration for the EVM requires a power supply capable of supplying 5 V (1 A) via banana jacks for the device power (AVDD and IOVDD) and 3.3 V (1A) via test clips for VREF. Also needed is 5 V (4A) via J12 power jack on the TSW1400EVM.



3.3 Interfaces

There are two key interfaces involved with the setup of this EVM. The first is directly on the EVM located at J16 on the bottom of the board. J16 is an FMC connector and interfaces with J1 on the ADC3683_TSW1400_Interposer_RevA (Interposer Card). The other side of the interposer card, J2 (directly across from J1), interfaces with J3 of the TSW1400EVM via an HSMC connector (bottom side of the board).

3.4 Test Points

The EVM has nine test points located on the board. There are four GND test points, one VREF test point, one REFBUF test point, one AVDD_SENSE test point, and one DVDD_SENSE test point.

The VREF test point is used to supply 3.3 V to the on board REF35160QDBVR Precision Voltage Reference. This chip is what supplies the ADC a 1.6 V external reference.

The REFBUF test point is not used in the default configuration. The REFBUF pin voltage can control the reference to the part if desired as opposed to doing this via SPI.

The AVDD_SENSE and IOVDD_SENSE test points are not used in the default configuration. These test points can be used when supplying AVDD and IOVDD independently (needs a board modification to accomplish this) to verify precise supply voltage.

3.5 Setup

Before setup, make sure the necessary software is downloaded and installed, as described in Section 2. Go ahead and open HSDC Pro and ADC35XX EVM GUI.

As an additional note, there are not any jumpers or headers that need to be checked or addressed.

First, connect the FMC data interface of the ADC36xxEVMCVAL (J16) to J1 of the LVDS interposer card (ADC3683_TSW1400_Interposer_RevA). Then, connect the HSMC interface of the LVDS interposer card to J3 of the TSW1400EVM.

Connect one mini-USB cable to the TSW1400EVM (J5) and another mini-USB cable to the ADC36xxEVMCVAL (J17).

Connect 5 V (4 A capable supply) to J12 of the TSW1400EVM. Turn the TSW1400EVM on using SW7.

Connect 5 V (1 A capable supply) banana jack to J18 of the ADC36xxEVMCVAL and the corresponding ground banana jack to J2 or J3 of the EVM. Turn the power supply on.

Connect 3.3 V (1 A capable supply) via a clip to VREF test point on the ADC36xxEVMCVAL and the corresponding ground clip to the most convenient GND test point on the EVM. Turn the power supply on.

Using a multi-meter, set the measure to volts (DC) and verify the following test points have the following voltage levels on the ADC36xxEVMCVAL.

Test Point	Voltage (V)
IOVDD	+1.8 VDC +/- 0.1 V
AVDD	+1.8 VDC +/- 0.1 V
VREF	+3.3 VDC +/- 0.1 V

Also using the multi-meter and the same settings above, verify the voltage at the node between R56 and C44 (bottom side of the board) is +1.6 VDC +/- 0.1 V. This is the voltage to be supplied as the external reference to the part. See the images below for reference to this location.



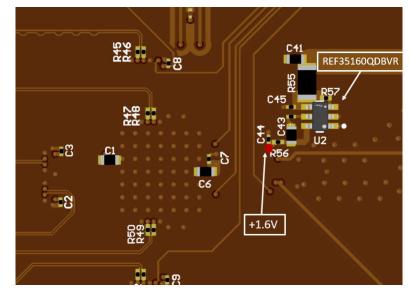
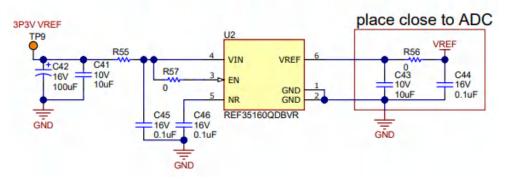


Figure 3-5. VREF (+1.6 V) Node

Reference Voltage





Connect an SMA cable between the output of a signal generator and the input of a 5 MHz band-pass filter. Set the frequency of the signal generator to 5 MHz with an amplitude of +10 dBm. Then connect an SMA cable between the output of the 5 MHz band-pass filter and the analog input of the ADC36xxEVMCVAL (J6) for Channel A. For Channel B testing, connect to J9. This is the analog input.

Connect an SMA cable between the output of a signal generator and the input of a 65 MHz band-pass filter. Set the frequency of the signal generator to 65 MHz with an amplitude of +10 dBm. Then connect an SMA cable between the output of the 65 MHz filter and the CLK input of the ADC36xxEVMCVAL (J12). The is the device sampling clock.

Connect an SMA cable to the output of a signal generator and the input of DCLKIN (J14) of the ADC36xxEVMCVAL. Set the frequency of the signal generator to 292.5 MHz with an amplitude of 0 dBm.

One important point is that the signal generators referenced above must share the same reference frequency (frequency locked). This is usually accomplished by connecting the 10 MHz input and output ports on the back panel of the signal generators using BNC cables.



4 Implementation Results

4.1 Evaluation Setup

Now that the hardware is setup and the necessary software has been installed, the user can now begin to capture data. The ADC powers up into the default mode with only a few actions needed to have data ready to capture. Once the EVM is opened, check to see if the USB is connected using the indicator next to the *Reconnect USB* button. If the USB is not connected, then make sure the clock signal is on and click *Reconnect USB*. Once the USB connects, the *Device Variant* box auto-populates to *ADC3683*. Make sure the Resolution is 18 bits, the Mode is set to 2 Wire, and DDC is set to Bypass in the *Output Info* box. Though not necessary for configuration, input 65 for Fs and click Enter on the keyboard, followed by clicking the *Calculate* button in the GUI to verify the correct DCLKIN frequency. The *CDC Clock Enable* slider needs to be red and off, as an external clock is being supplied. Simply click the slider to turn off if the *CDC Clock Enable* slider is still enabled. Perform a software reset by clicking *Reset* and then click the *Configure* button to configure the part.

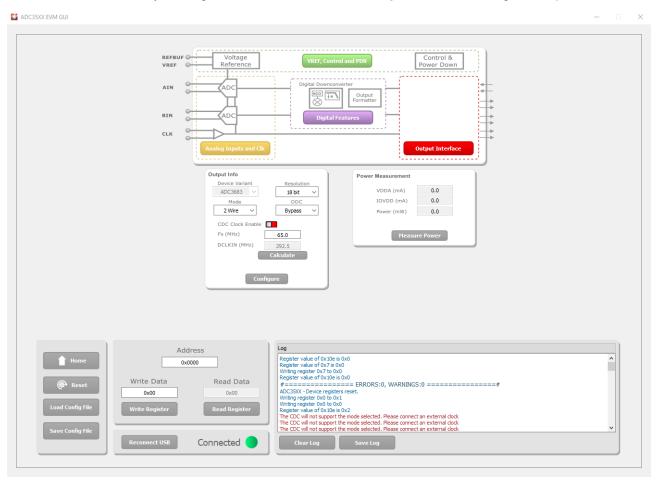
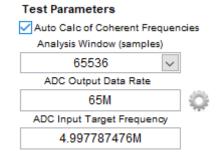
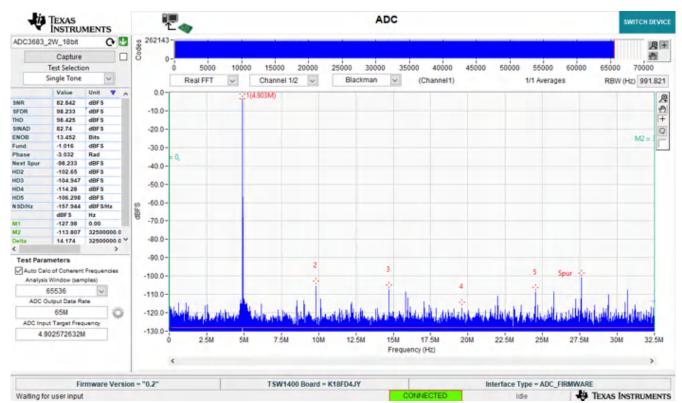


Figure 4-1. ADC35XXEVM GUI Configuration

After launching HSDC Pro, a window prompts a board connection. The serial number of the TSW1400EVM appears. Click *OK* to connect to the TSW1400EVM. Another window pops up prompting the user to select a device. Select *ADC* from the *Select a device* drop-down menu. Click *OK* in the pop-up box that reads *No firmware*. *Please select a device to load firmware into the board*. Use the *Select ADC* drop-down menu at the top left corner to select *ADC3683_2W_18bit*. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW1400EVM. Enter *65M* into the *ADC Output Data Rate* field at the bottom left corner. Calculate the coherent 5 MHz frequency by entering *5M* into the *ADC Input Target Frequency* box and then clicking in the *Auto Calculation of Coherent Frequencies* box. Enter this new coherent frequency value into the signal generator of the input signal. Click *Capture* to capture data from the ADC.







4.2 Performance Data and Results

Figure 4-3. ADC36xxEVMCVAL Default Configuration Capture

The capture above is a typical result from the default configuration. Remember that typical values can vary slightly depending on the setup and the quality of SMA cables, signal generators and filters that are used in the setup.



5 Hardware Design Files

5.1 Schematics

For schematic files, please refer to the *Design files* tab on the product page for ADC36xxEVMCVAL.

5.2 PCB Layouts

For PCB layout files, please refer to the *Design files* tab on the product page for ADC36xxEVMCVAL.

5.3 Bill of Materials (BOM)

For the BOM, please refer to the *Design files* tab on the product page for ADC36xxEVMCVAL.

6 Additional Information

6.1 Trademarks

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NOTE:

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3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

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- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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