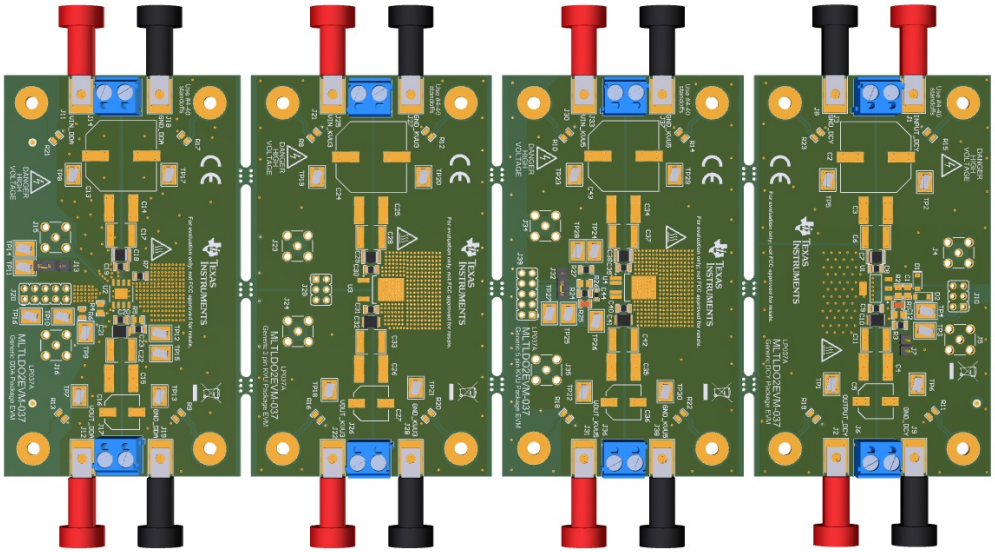
MLTLDO2EVM-037 Evaluation Module



This user's guide describes the operational use of the MLTLDO2EVM-037 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of linear regulators. The EVM is specifically designed for linear regulators which are packaged in the DDA, DCY, 3-pin KVU and 5-pin KVU packages. Included in this user's guide are setup and operating instructions, thermal and layout guidelines, a printed circuit board (PCB) layout, a schematic diagram, and a bill of materials (BOM).

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Trademarks

All trademarks are the property of their respective owners.

1 General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitable qualified, you should immediately stop from further use of the HV EVM.

1. Work Area Safety
   a. Keep work area clean and orderly.
   b. Qualified observer(s) must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and nonconductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety
   As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
   a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   c. After EVM readiness is complete, energize the EVM as intended.

WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

3. Personal Safety
   a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

2 Introduction

TI's MLTLDO2EVM-037 helps design engineers evaluate the operation and performance of linear regulators for possible use in their own circuit application. The MLTLDO2EVM-037 EVM offers four linear regulator designs, each one electrically isolated from the other through tab routing in the PCB fabrication step. The boards can be quickly separated through the breakaway tabs if desired. Combined, the boards can mount many linear regulators which come in the DDA, DCY, 3-pin KVU and 5-pin KVU packages. The boards that carry the DDA, DCY and 3-pin KVU packages have been designed to withstand up to 100 Vdc of voltage across its input and output terminals. The board carrying the 5-pin KVU package has been designed to withstand up to 50 Vdc of voltage across its input and output terminals. All four boards have been designed to withstand 5 Adc of current draw. This allows the EVM to be used for numerous linear regulator designs in TI's portfolio, as well as future designs that may operate into high voltage or high current. Each board is designed to populate multiple input and output capacitors, allowing the user to customize the EVM for their specific needs. User-selectable grounding is available on each board, allowing the user to evaluate the linear regulator in a floating application. Thermal vias have been placed near each linear regulator to aid in thermal spreading of the heat generated by the device. The EVM comes with four bumpons to lift the EVM off of the test surface, and mounting holes are provided for standoffs or mounting to an external chassis. Additional features provided for each design are covered in this User's Guide.

2.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the MLTLDO2EVM-037. Observe all safety precautions.

WARNING

Danger: HIGH VOLTAGE! This evaluation board is intended for professional use only. This board has exposed high voltages. Do not operate this board without proper high-voltage and high-current safety practices. Read this user guide carefully before testing with the MLTLDO2EVM-037. Use floating measurement equipment such as high-voltage differential scope probes.

WARNING

Hot surface. Contact may cause burns. Do not touch.

CAUTION

The circuit module can be damaged by overtemperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

CAUTION

Some power supplies can be damaged by application of external voltages. If you are using more than one power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

Do not leave EVM powered when unattended.

CAUTION

The circuit module is not a finished product or electrical appliance. The module does not contain current or voltage thresholds for circuit protection. It must be used by qualified personnel with additional equipment for evaluation only.

2.2 MLTLDO2EVM-037 Design Details

2.2.1 Connector Ratings

Each board within the MLTLDO2EVM-037 comes with two sets of input and output connectors. The banana connectors are rated for 60 Vdc maximum applied voltage, however banana cables are typically rated for low voltage only. The user should review the voltage rating of the banana cables prior to applying power to the EVM. If the banana cables are not rated for the voltage being applied to the EVM, the terminal blocks must be used instead. For the purposes of this user guide, it is assumed that the banana cables are rated up to 50 Vdc. For operation above 50 Vdc, the terminal blocks must be used. Either set of connectors may be used for the current draw of the EVM when the load current is less than or equal to 5 Adc.

2.2.2 EVM Operation Up To 50 Vdc (KVU|5 Package) or 100 Vdc (DCY, DDA, and KVU|3 Packages)

The IPC-2221 standard was used during the design of the MLTLDO2EVM-037 to set the conductor spacing between low-voltage nets and high-voltage nets. Specifically, column A6 of Table 6-1 was used during the design of the EVM. The boards carrying the DCY, DDA, and 3-pin KVU packages were designed with 100 Vdc spacing in accordance with the IPC-2221 standard, Table 6-1, column A6. The board carrying the 5-pin KVU package was also designed with 100 Vdc spacing in accordance with the IPC-2221 standard, Table 6-1, column A6; however the 5-pin KVU package pin spacing is too narrow to meet 100 Vdc clearance. This board is therefore rated up to 50 Vdc in accordance with the IPC-2221 standard.

2.2.3 The Importance of a Clean PCB

Prior to connecting power to any circuit board, it is always important to ensure the PCB is free from contaminants. These contaminants can come in the form of flux residue, oils deposited from handling the PCB, dirt, or other sources of foreign object debris (FOD). Contaminants affect the electrical characteristics of the PCB by lowering the isolation impedance between traces. Furthermore, they can introduce additional leakage paths into the system. If the PCB is to be used at high voltage, it is critical that the board is clean from contaminants, as arcing through the contaminants may occur. The MLTLDO2EVM-037 is shipped from the factory clean from contaminants. If you believe the board may have contaminants, please consult your organization's procedures on testing for contaminants or refer to IPC-TM-650. Common methods of cleaning a PCB include a DI bath or use of a specially made PCB cleaning product readily available through distributors. To clean the PCB, consult the processes in your organization for the right cleaning process for your hardware. Alternatively, refer to IPC-CH-65B which offers guidelines on cleaning printed-circuit boards and assemblies.

2.2.4 EVM System Grounding

Each board within the MLTLDO2EVM-037 is electrically isolated from the other three boards in the EVM. External mounting holes are provided to mount the EVM to the system chassis. An 0805-sized surface pad is placed near each mounting hole. If populated, the components will tie the mounting hole to the internal board ground plane. The user may short these pads if the chassis should be tied directly to ground. If the EVM will be floating, it is recommended that the user capacitively couple the EVM to the chassis using an 0805-sized capacitor.

2.3 EVM Mounting Hole Locations

Each of the four boards within the MLTLDO2EVM-037 has mounting holes for standoffs or placement into a chassis. The mounting hole locations on an individual board are separated in width by 1.71 inches and length by 3.315 inches. The MLTLDO2EVM-037 mounting hole locations are separated in width by 8.925 inches and length by 3.315 inches.

2.4 Using the MLTLDO2EVM-037 PCB Beyond Its Design Ratings

2.4.1 EVM Operation Beyond 5 Adc

The MLTLDO2EVM-037 PCB was designed to withstand current loading up to 5 Adc from VIN to VOUT, and back through the ground plane, of each board. If larger load currents are used, the user should review the connector data sheets to confirm they can withstand the load current. By design the current density will be the largest at the package pins of each linear regulator. As such, the linear regulator package pins will experience elevated heat and current density when the load current is above 5 Adc.

2.4.2 EVM Operation Beyond 50 Vdc (KVU|5 Package) or 100 Vdc (DCY, DDA, and KVU|3 Packages)

If the end use of the MLTLDO2EVM-037 PCB will require larger voltages than it was designed for, it may still be possible to use it if the proper precautions are taken. A common method to extending the voltage rating of a PCB is to apply conformal coating. Conformal coatings are readily available through most distributors.

2.5 Inputs/Outputs Connectors and Jumper Descriptions

2.5.1 J1 – INPUT_DCY_BANANA

Input voltage for the DCY package. Use this connection for voltages at 50 Vdc or less.

2.5.2 J2 – OUTPUT_DCY_BANANA

Regulated output power supply voltage for the DCY package. Use this connection for voltages at 50 Vdc or less.

2.5.3 J3 – INPUT_DCY_TERMINAL

Input voltage terminal block for the DCY package.

2.5.4 J4 – DCY_IN_S

Input voltage sense for the DCY package.

2.5.5 J5 –DCY_OUT_S

Output voltage sense for the DCY package.

2.5.6 J6 – OUTPUT_DCY_TERMINAL

Output voltage terminal block for the DCY package.

2.5.7 J7 – DCY_FB

DCY package feedback pin header.

2.5.8 J8 – GND_DCY_BANANA_IN

Input supply ground for the DCY package. Use this connection for voltages at 50 Vdc or less.

2.5.9 J9 – GND_DCY_BANANA_OUT

Regulated output supply ground for the DCY package. Use this connection for voltages at 50 Vdc or less.

2.5.10 J10 – DCY PACKAGE TEST HOOKUP

Intended for test purposes only.

2.5.11 J11 – INPUT_DDA_BANANA

Input voltage for the DDA package. Use this connection for voltages at 50 Vdc or less.

2.5.12 J12 – OUTPUT_DDA_BANANA

Regulated output power supply voltage for the DDA package. Use this connection for voltages at 50 Vdc or less.

2.5.13 J13 – DDA_EN

DDA package EN pin header. Connect the jumper from pin 1 to pin 2 of the header to enable the DDA package linear regulator.

2.5.14 J14 – INPUT_DDA_TERMINAL

Input voltage terminal block for the DDA package.

2.5.15 J15 – DDA_IN_S

Input voltage sense for the DDA package.

2.5.16 J16 –DDA_OUT_S

Output voltage sense for the DDA package.

2.5.17 J17 – OUTPUT_DDA_TERMINAL

Output voltage terminal block for the DDA package.

2.5.18 J18 – GND_DDA_BANANA_IN

Input supply ground for the DDA package. Use this connection for voltages at 50 Vdc or less.

2.5.19 J19 – GND_DDA_BANANA_OUT

Regulated output supply ground for the DDA package. Use this connection for voltages at 50 Vdc or less.

2.5.20 J20 – DDA PACKAGE TEST HOOKUP

Intended for test purposes only.

2.5.21 J21 – INPUT_KVU3_BANANA

Input voltage for the KVU 3-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.22 J22 – OUTPUT_KVU3_BANANA

Regulated output power supply voltage for the KVU 3-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.23 J23 – KVU3_IN_S

Input voltage sense for the KVU 3-pin package.

2.5.24 J24 –KVU3_OUT_S

Output voltage sense for the KVU 3-pin package.

2.5.25 J25 – INPUT_KVU3_TERMINAL

Input voltage terminal block for the KVU 3-pin package.

2.5.26 J26 – OUTPUT_KVU3_TERMINAL

Output voltage terminal block for the KVU 3-pin package.

2.5.27 J27 – GND_KVU3_BANANA_IN

Input supply ground for the KVU 3-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.28 J28 – GND_KVU3_BANANA_OUT

Regulated output supply ground for the KVU 3-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.29 J29 – KVU3 PACKAGE TEST HOOKUP

Intended for test purposes only.

2.5.30 J30 – INPUT_KVU5_BANANA

Input voltage for the KVU 5-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.31 J31 – OUTPUT_KVU5_BANANA

Regulated output power supply voltage for the KVU 5-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.32 J32 – KVU5_EN

KVU 5-pin package EN pin header. Connect the jumper from pin 1 to pin 2 of the header to enable the KVU 5-pin package linear regulator.

2.5.33 J33 – INPUT_KVU5_TERMINAL

Input voltage terminal block for the KVU 5-pin package.

2.5.34 J34 – KVU5_IN_S

Input voltage sense for the KVU 5-pin package.

2.5.35 J35 –KVU5_OUT_S

Output voltage sense for the KVU 5-pin package.

2.5.36 J36 – OUTPUT_KVU5_TERMINAL

Output voltage terminal block for the KVU 5-pin package.

2.5.37 J37 – GND_KVU5_BANANA_IN

Input supply ground for the KVU 5-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.38 J38 – GND_KVU5_BANANA_OUT

Regulated output supply ground for the KVU 5-pin package. Use this connection for voltages at 50 Vdc or less.

2.5.39 J39 – KVU5 PACKAGE TEST HOOKUP

Intended for test purposes only.

2.5.40 TP1 – DCY_OUTPUT

DCY regulated output voltage test point.

2.5.41 TP2 – DCY_INPUT

DCY input voltage test point.

2.5.42 TP3 – DCY_BODE_TOP

DCY top bode resistor test point.

2.5.43 TP4 – DCY_BODE_BOTTOM

DCY bottom bode resistor test point.

2.5.44 TP5 – DCY_INPUT_GND

DCY input ground test point.

2.5.45 TP6 – DCY_OUTPUT_GND

DCY output ground test point.

2.5.46 TP7 – DDA_OUTPUT

DDA regulated output voltage test point.

2.5.47 TP8 – DDA_INPUT

DDA input voltage test point.

2.5.48 TP9 – DDA_PG

DDA power good test point.

2.5.49 TP10 – DDA_FB

DDA feedback pin test point.

2.5.50 TP11 – DDA_EN

DDA enable test point.

2.5.51 TP12 – DDA_DELAY

DDA delay test point.

2.5.52 TP13 – DDA_INPUT_GND

DDA input ground test point.

2.5.53 TP14 – DDA_EN_GND

DDA ground test point.

2.5.54 TP15 – DDA_DELAY_GND

DDA ground test point.

2.5.55 TP16 – DDA_FB_GND

DDA ground test point.

2.5.56 TP17 – DDA_OUTPUT_GND

DDA output ground test point.

2.5.57 TP18 – KVU3_OUTPUT

A 3-pin KVU output test point.

2.5.58 TP19 – KVU3_INPUT

A 3-pin KVU input test point.

2.5.59 TP20 – KVU3_INPUT_GND

A 3-pin KVU input ground test point.

2.5.60 TP21 – KVU3_OUTPUT_GND

A3-pin KVU output ground test point.

2.5.61 TP22 – KVU5_OUTPUT

A 5-pin KVU output test point.

2.5.62 TP23 – KVU5_INPUT

A 5-pin KVU input test point.

2.5.63 TP24 – KVU5_EN

A 5-pin KVU enable test point.

2.5.64 TP25 – KVU5_BODE_BOTTOM

A 5-pin KVU bottom bode resistor test point.

2.5.65 TP26 – KVU5_BODE_TOP

A 5-pin KVU top bode resistor test point.

2.5.66 TP27 – KVU5_FB

A 5-pin KVU feedback pin test point.

2.5.67 TP28 – KVU5_FB_GND

A 5-pin KVU ground test point.

2.5.68 TP29 – KVU5_INPUT_GND

A 5-pin KVU input ground test point.

2.5.69 TP30 – KVU5_OUTPUT_GND

A 5-pin KVU output ground test point.

2.6 Soldering Guidelines

To avoid damaging the integrated circuit (IC), use a hot-air system for any solder rework to modify the EVM for the purpose of repair or other application rework. An IR infrared rework station may also be used to rework the EVM.

2.7 Equipment Connection

Connect the equipment as shown in the following steps:

1. Review the data sheet for the linear regulator being installed on the MLTLDO2EVM-037 EVM.
2. Set the input power supply up to maximum rated voltage as listed on the data sheet, then turn it off.
3. Locate the positive banana connector (if the input voltage will be less than or equal to 50 Vdc) or the screw terminal (if the input voltage will be greater than 50 Vdc) on the EVM for the linear regulator package you are testing. Connect the positive terminal of the input power supply to the correct positive input on the EVM.
4. Locate the ground banana connector (if the input voltage will be less than or equal to 50 Vdc) or the screw terminal (if the input voltage will be greater than 50 Vdc) on the EVM for the linear regulator package you are testing. Connect the ground terminal of the input power supply to the correct GND input of the EVM.
5. Locate the output banana connectors (if the output voltage will be less than or equal to 50 Vdc) or the

screw terminal (if the output voltage will be greater than 50 Vdc) on the EVM for the linear regulator package you are testing. Connect the load between the output of the linear regulator and ground using the correct outputs (banana connectors or screw terminals). Be sure not to exceed the load current limit as described in the linear regulator data sheet.

6. Disable the 5-pin KVU package by connecting J32 pin 2 (EN_KVU5) to J32 pin 3 (GND_KVU5).
7. Disable the DDA package by connecting J13 pin 2 (EN_DDA) to J13 pin 3 (GND_DDA).

3 PCB Layout

Figure 1 to Figure 5 illustrate the PCB layouts for this EVM.

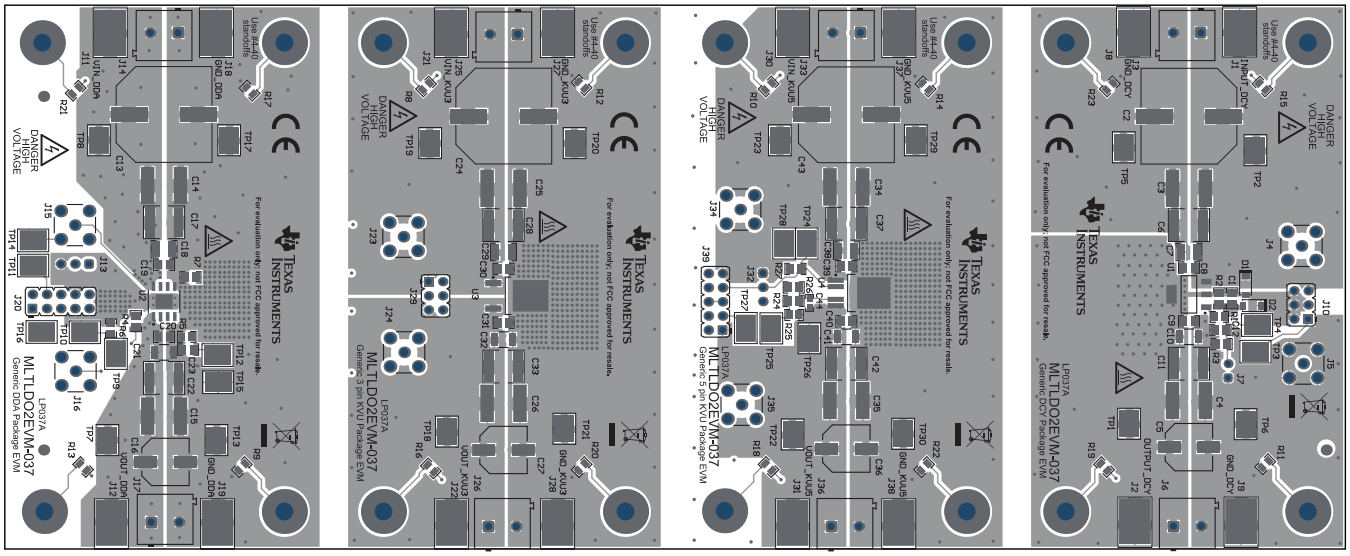

Figure 1. Assembly Layer

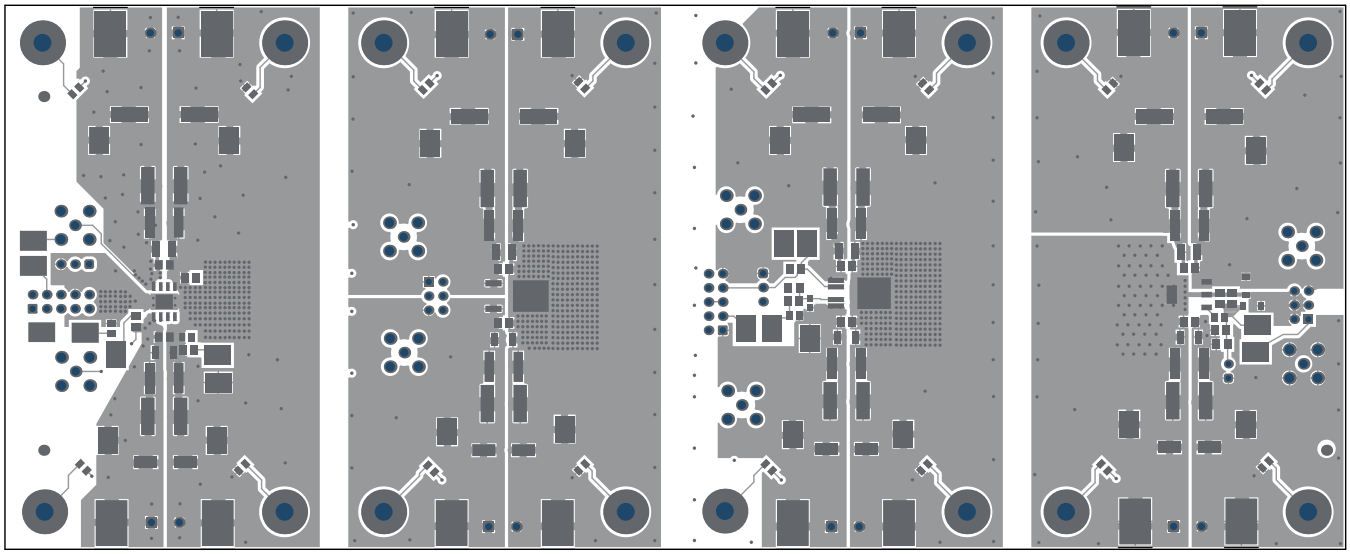

Figure 2. Top Layer Routing

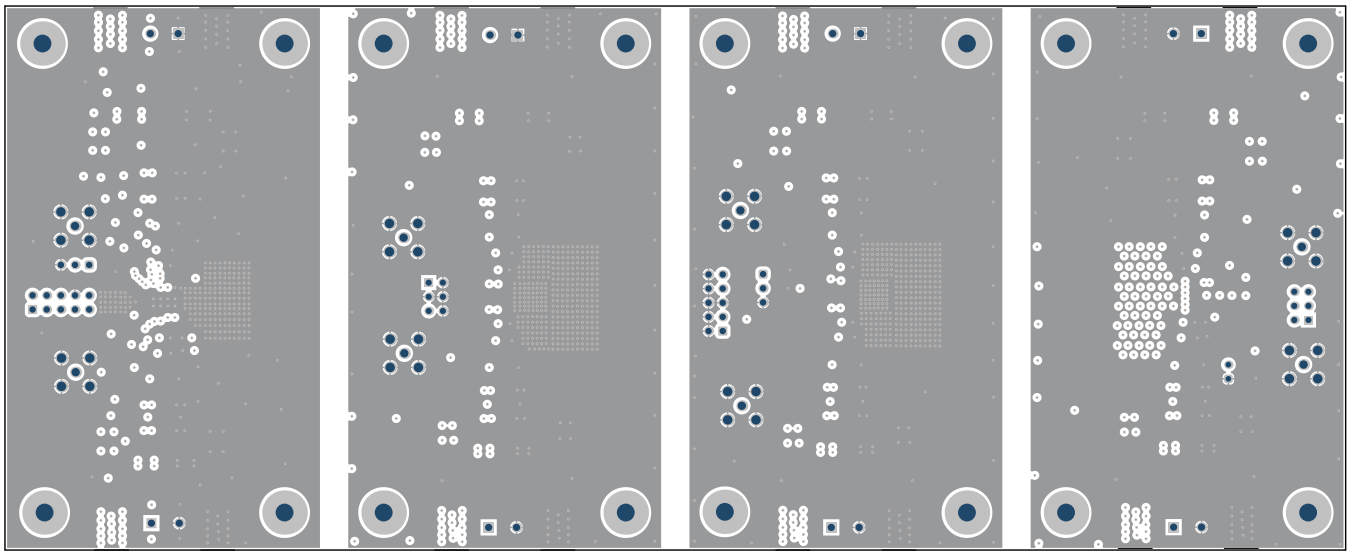

Figure 3. First Middle Layer

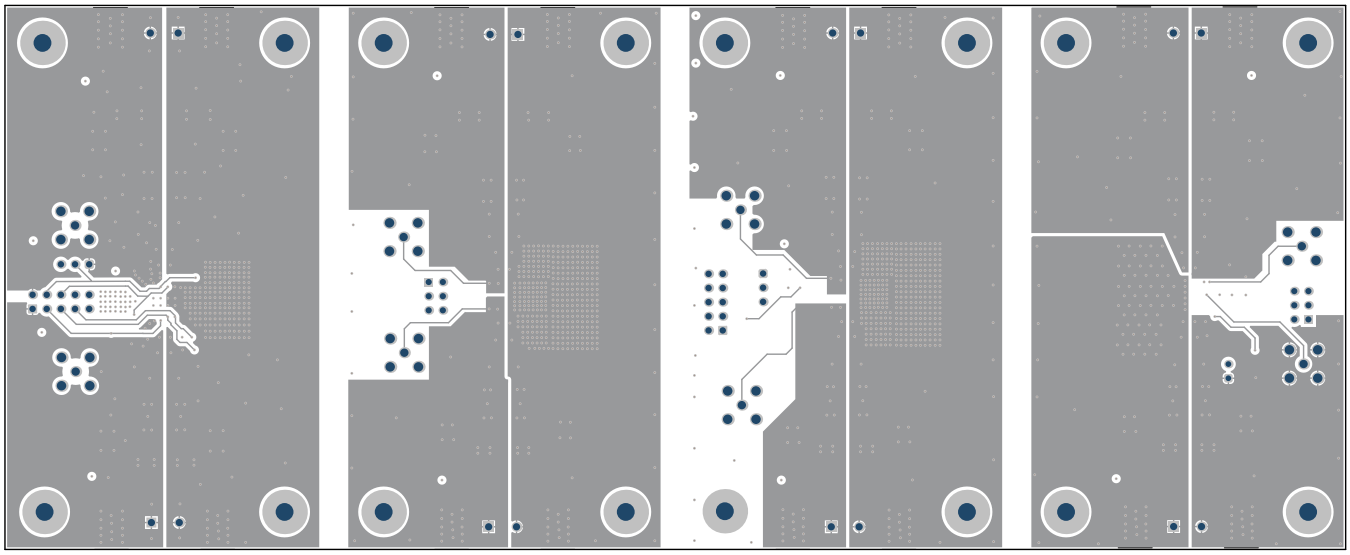

Figure 4. Second Middle Layer

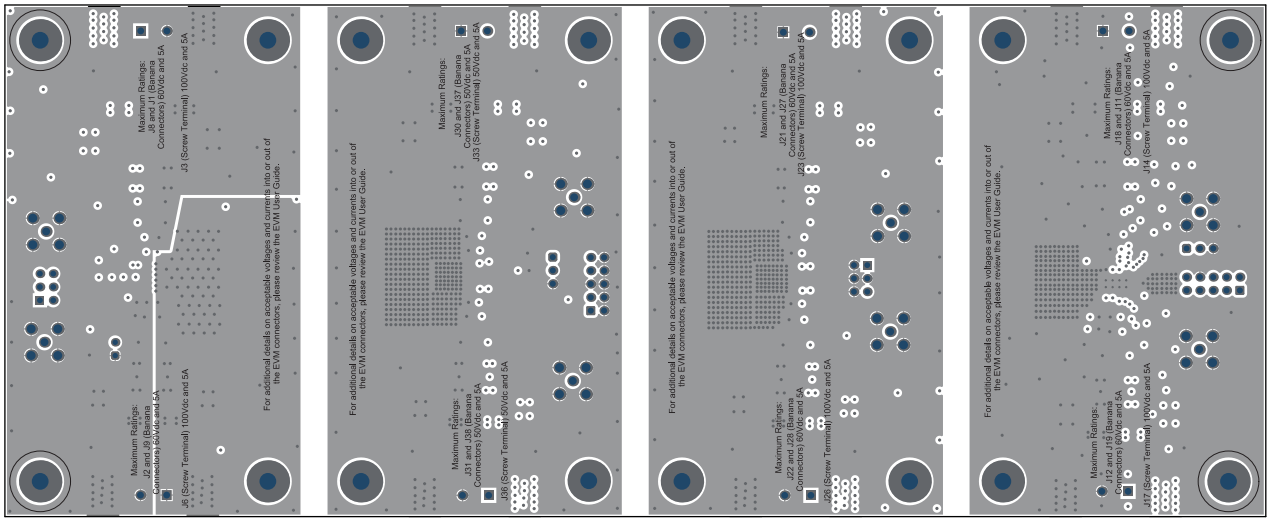

Figure 5. Bottom Layer Routing

4 Schematic

Figure 6 to Figure 9 provide the schematics for this EVM.

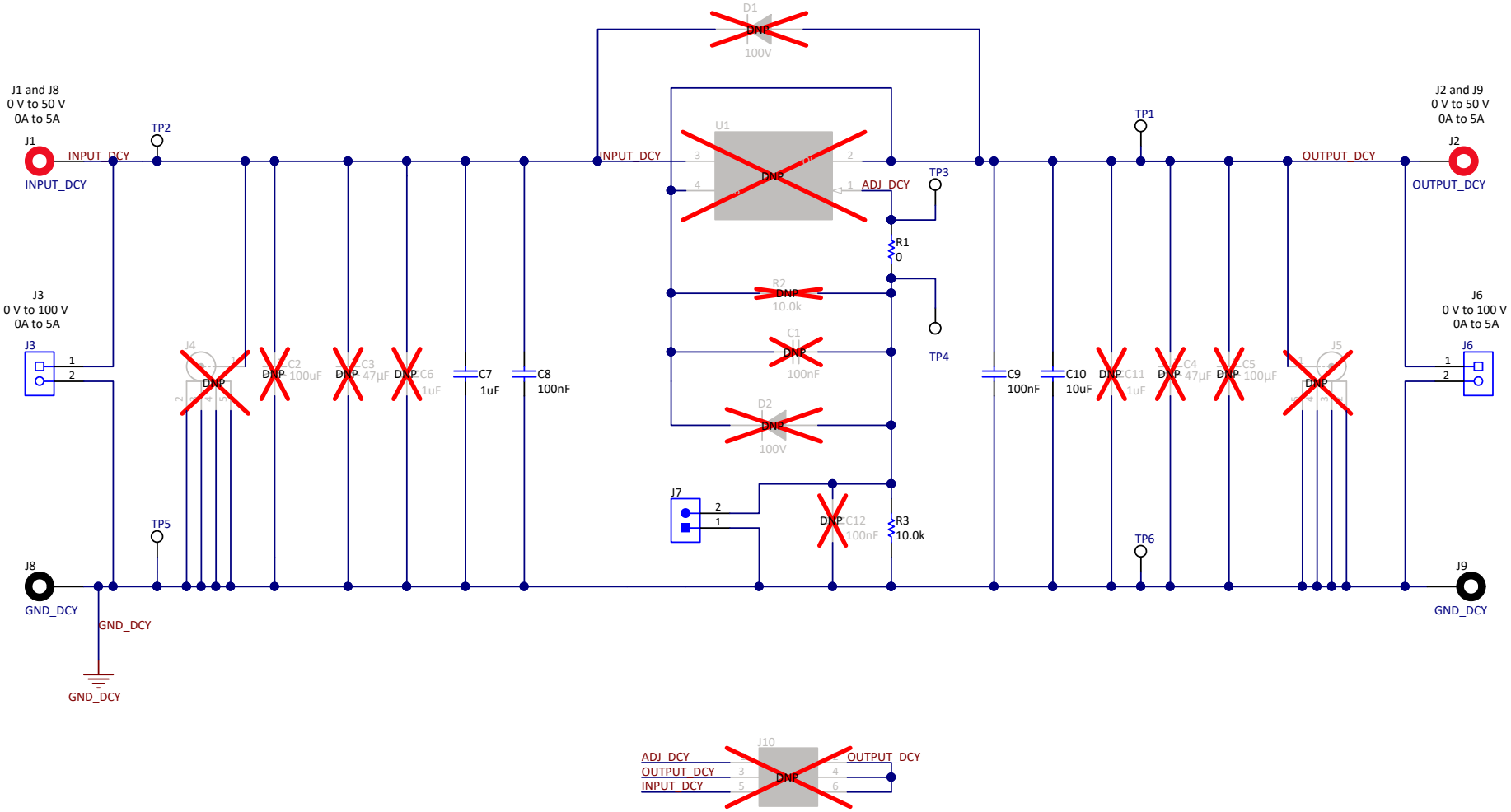

Figure 6. Generic DCY Package Schematic

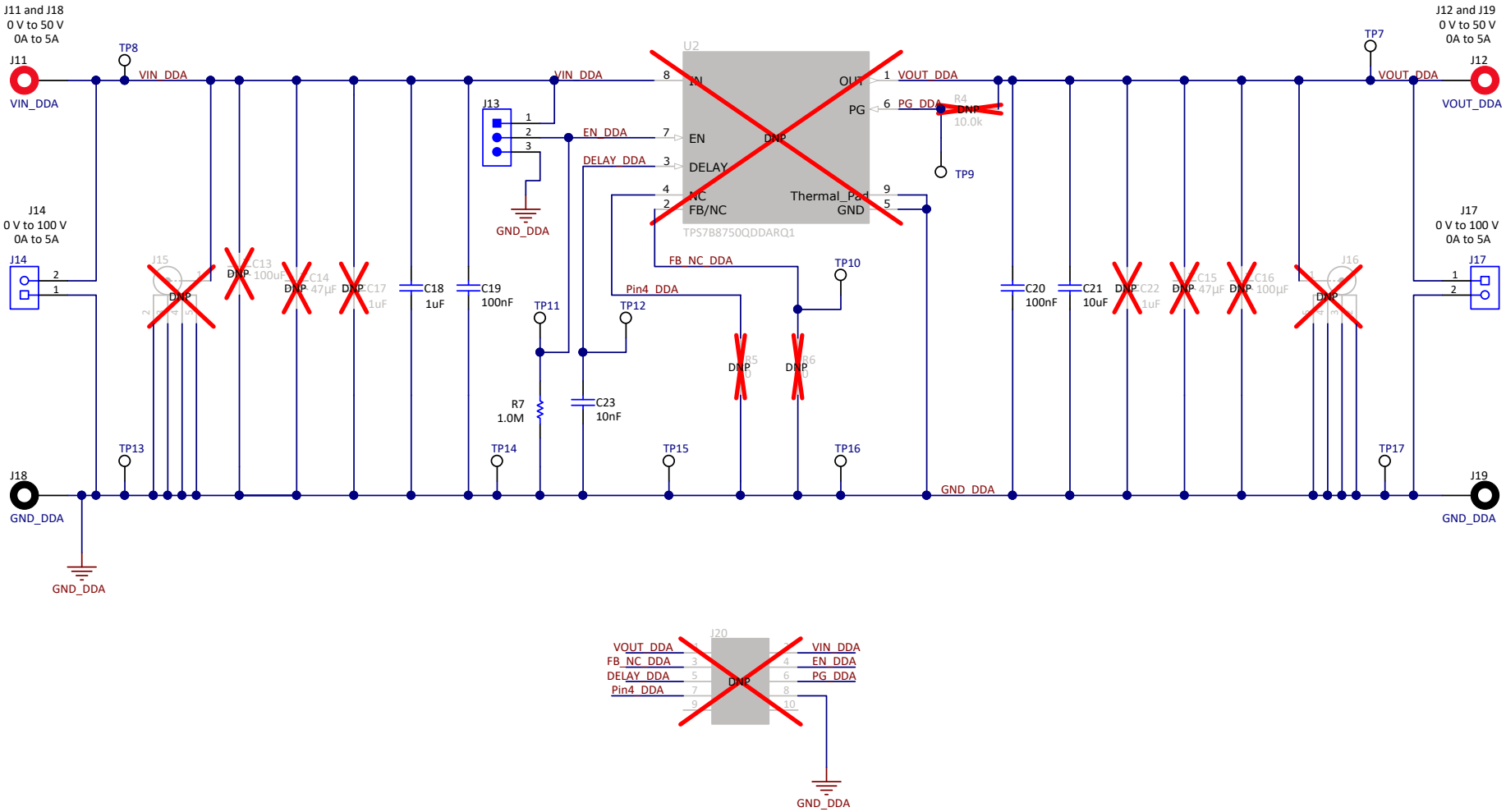

Figure 7. Generic DDA Package Schematic

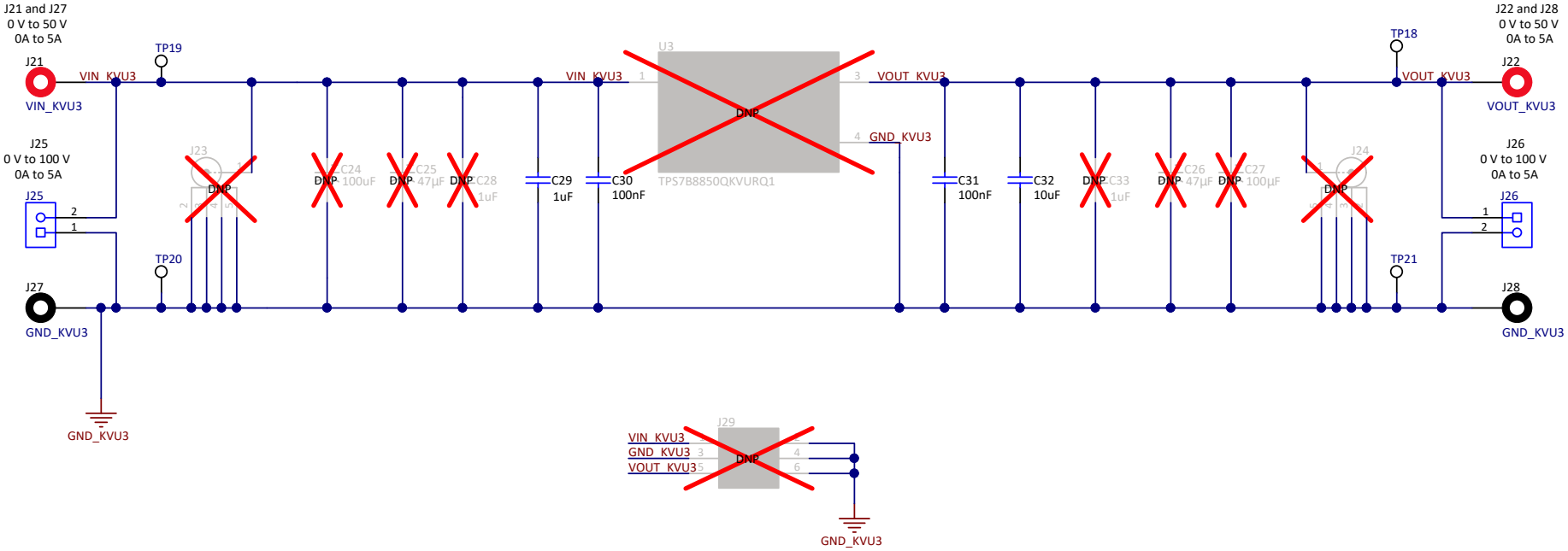

Figure 8. Generic 3-pin KVU Package Schematic

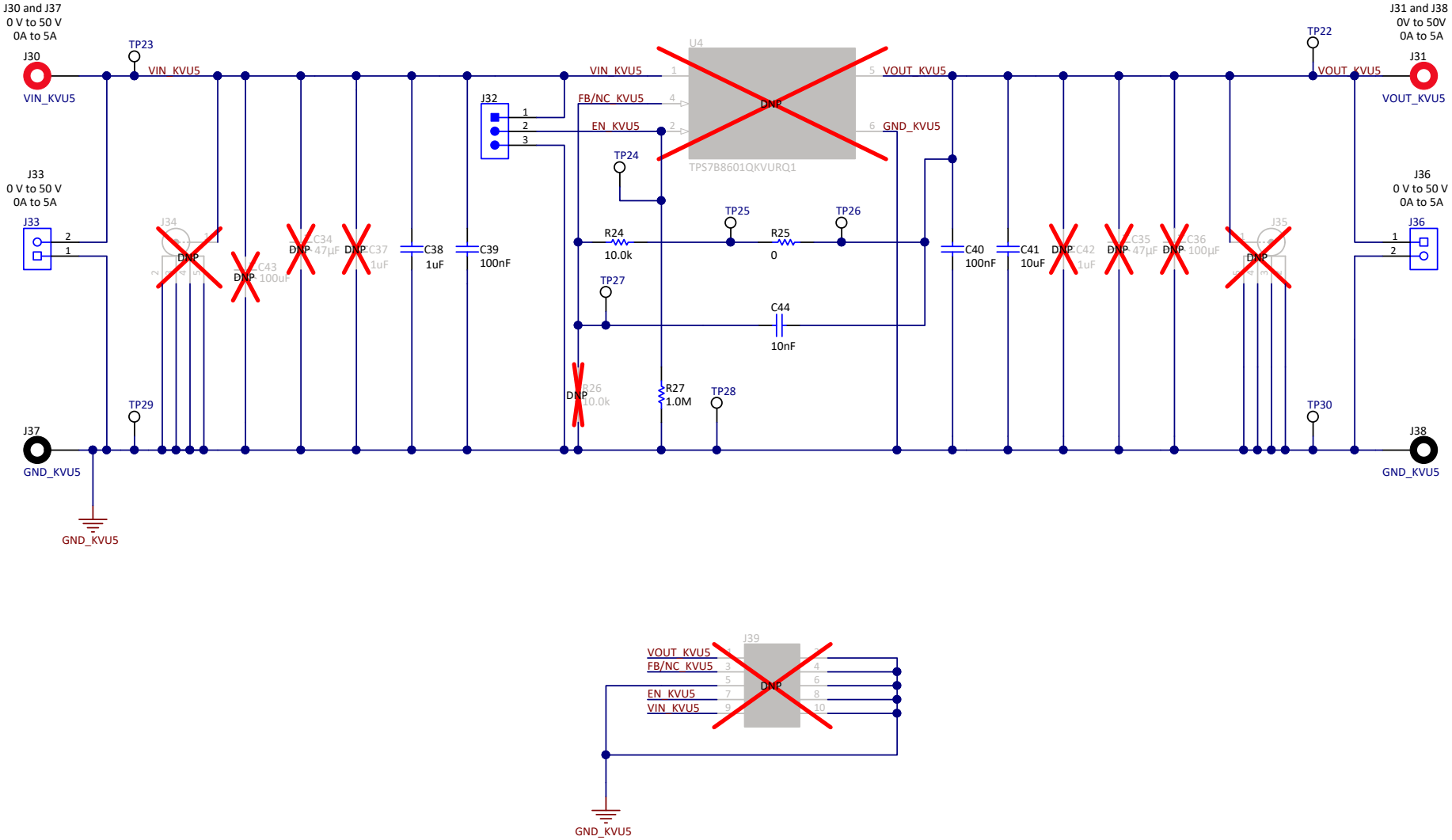

Figure 9. Generic 5-pin KVU Package Schematic

5 Bill of Materials

Table 1 shows the BOM for this EVM.

Table 1. MLTLDO2EVM-037 BOM(1)(2)(3)(4)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LP037	Any		
C7, C18, C29, C38	4	1 µF	CAP, CERM, 1 µF, 100 V, ±10%, X7R, 1210	1210	C3225X7R2A105K200AA	TDK		
C8, C9, C19, C20, C30, C31, C39, C40	8	0.1 µF	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0805	0805	CGA4J2X7R2A104K125AA	TDK		
C10, C21, C32, C41	4	10 µF	CAP, CERM, 10 µF, 50 V, ±20%, X7R, 1210	1210	C3225X7R1H106M250AC	TDK		
C23	1	0.01 µF	CAP, CERM, 0.01 µF, 100 V, ±10%, X7R, 0805	0805	08051C103KAT2A	AVX		
C44	1	0.01 µF	CAP, CERM, 0.01 µF, 100 V,±10%, X7R, 0603	0603	885012206114	Wurth Elektronik		
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1, J2, J11, J12, J21, J22, J30, J31	8		Standard Banana Jack, Insulated, Red	6091	6091	Keystone		
J3, J6, J14, J17, J25, J26, J33, J36	8		Terminal Block, 5 mm, 2 × 1, Tin, TH	Terminal Block, 5 mm, 2 × 1, TH	691 101 710 002	Wurth Elektronik		
J7	1		Header, 2.54 mm, 2 × 1, Tin, TH	Header, 2.54 mm, 2 × 1, TH	TSW-102-23-T-S	Samtec		
J8, J9, J18, J19, J27, J28, J37, J38	8		Standard Banana Jack, Insulated, Black	6092	6092	Keystone		
J13, J32	2		Header, 2.54 mm, 3 × 1, Gold, TH	Header, 2.54 mm, 3 × 1, TH	61300311121	Wurth Elektronik		
R1, R25	2	0	RES, 0, 1%, 0.5 W, 0805	0805	5106	Keystone		
R3, R24	2	10.0 kΩ	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080510K0FKEA	Vishay-Dale		
R7, R27	2	1.0 Meg	RES, 1.0 M, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6GEYJ105V	Panasonic		
SH-J1, SH-J2	2	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30	30		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
C1, C12	0	0.1 µF	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 0805	0805	GRM21BR72A104KAC4L	MuRata		

(1) These assemblies are ESD sensitive, observe ESD precautions.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Unless otherwise noted in the *Alternate Part Number* or *Alternate Manufacturer* columns, all parts can be substituted with equivalents.

Table 1. MLTLDO2EVM-037 BOM[(1)(2)(3)(4)] (continued)

Designator	QTY	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C2, C13, C24, C43	0	100 µF	CAP, AL, 100 µF, 100 V, ±20%, 0.17 ohm, AEC-Q200 Grade 2, SMD	SMT Radial J16	EEV-FK2A101M	Panasonic		
C3, C4, C14, C15, C25, C26, C34, C35	0	47 µF	CAP, TA, 47 µF, 50 V, ±10%, 0.24 ohm, SMD	6.2 × 6 mm	597D476X9050Z2T	Vishay-Sprague		
C5, C16, C27, C36	0	100 µF	CAP, AL, 100 µF, 35 V, ±20%, 0.2 ohm, AEC-Q200 Grade 1, SMD	D8 × L10.2 mm	EEE-TC1V101P	Panasonic		
C6, C11, C17, C22, C28, C33, C37, C42	0	1 µF	CAP, CERM, 1 µF, 250 V, ±10%, X7R, 2220	2220	GRM55DR72E105KW01L	MuRata		
D1, D2	0	100 V	Diode, Switching, 100 V, 0.15 A, SOD-123FL	SOD-123FL	1N4148WFL-G3-08	Vishay-Semiconductor		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
H1, H2, H3, H4, H13, H14, H15, H16, H21, H22, H23, H24, H29, H30, H31, H32	0		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply		
H5, H6, H7, H8, H17, H18, H19, H20, H25, H26, H27, H28, H33, H34, H35, H36	0		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone		
J4, J5, J15, J16, J23, J24, J34, J35	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
J10, J29	0		Header, 2.54 mm, 3 × 2, Gold, TH	Header, 2.54 mm, 3 × 2, TH	61300621121	Wurth Elektronik		
J20, J39	0		Header, 2.54 mm, 5 × 2, Gold, TH	Header, 2.54 mm, 5 × 2, TH	61301021121	Wurth Elektronik		
R2, R4, R26	0	10.0 kΩ	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080510K0FKEA	Vishay-Dale		
R5, R6, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23	0	0	RES, 0, 1%, 0.5 W, 0805	0805	5106	Keystone		
U1	0		Most LDOs in the DCY package	DCY0004A		Texas Instruments		
U2	0		Most LDOs in the DRV package	SOIC8		Texas Instruments		
U3	0		Most LDOs in the DQN package	KVU0003A		Texas Instruments		
U4	0		Most LDOs in the SOT-23 package	KVU0005A		Texas Instruments		

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265