User's Guide

TPS7A57EVM-056 Evaluation Module

ABSTRACT

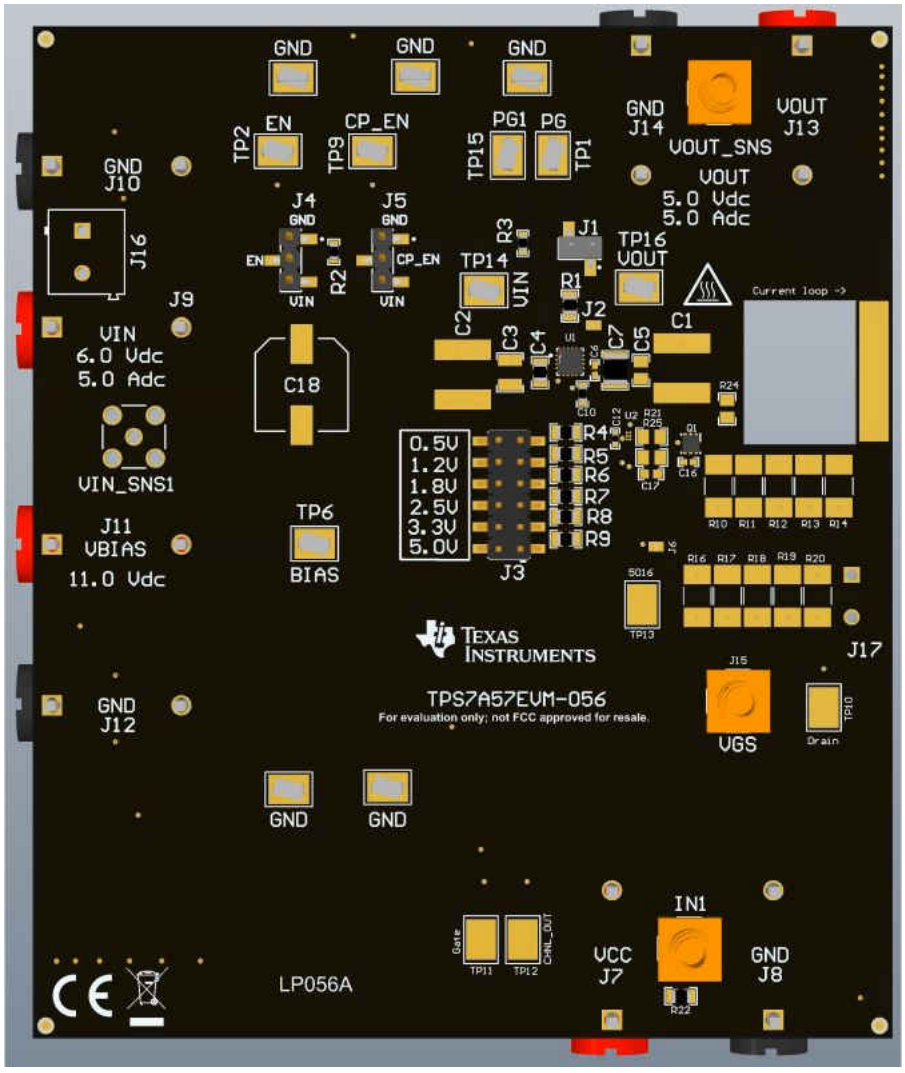

Figure 1-1. TPS7A57EVM-056 Evaluation Module

This user's guide describes the operational use of the TPS7A57EVM-056 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A57 low-dropout linear regulator (LDO). Included in this user's guide are setup and operating instructions, thermal and layout guidelines, a printed-circuit board (PCB) layout, schematic diagrams, and a bill of materials (BOM).

Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the TPS7A57EVM-056.

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1 Introduction

The Texas Instruments TPS7A57EVM-056 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A57 LDO voltage regulator. As shown in Table 1-1, the TPS7A57EVM-056 contains one TPS7A57 LDO voltage regulator in the RTE package. An optional load transient circuit is also included to assist the user with high-speed load transient testing.

Table 1-1. Device Information

EVM ORDERABLE NUMBER	V_{OUT}	PART NAME	PACKAGE
TPS7A57EVM-056	0.5 V to 5.2 V	TPS7A5701RTE	16-pin RTE

2 Setup

This section describes the jumpers and connectors on the EVM, and how to properly connect, set up, and use the TPS7A57EVM-056. Section 2.1 and Section 2.3 describe the test setup and operation for the TPS7A57 LDO. Section 2.2 and Section 2.4 describe the test setup and operation of the optional load transient circuit.

2.1 LDO Input and Output Connector Descriptions

2.1.1 VIN and GND

VIN (J9) and GND (J10) are the connection terminals for the input supply. The VIN terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.1.2 VOUT and GND

VOUT (J13) and GND (J14) are the connection terminals for the output load. The VOUT terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.1.3 J3

J3 is a 6-pin header used to select different output voltage options for the TPS7A57.

The header connects the REF pin to a resistor to set a given output voltage value. The voltage options are 0.5 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V, 5.0 V.

2.1.4 J4 (EN)

J4 (EN) is a 3-pin header used to enable or disable the TPS7A57.

The center pin of the 3-pin header is tied to the TPS7A57 EN input. When the 2-pin shunt is placed across the bottom two pins of the header, VIN is shorted to EN, and the TPS7A57 is enabled. When the 2-pin shunt is placed across the top two pins of the header, GND is shorted to EN, and the TPS7A57 is disabled. Alternatively, the 3-pin header can remain floating. If the 3-pin header is floating, the TPS7A57 remains disabled.

When driving the EN terminal with an off-board supply or signal generator, the applied voltage must be kept between 0 V and 6.0 V.

2.1.5 J5 (CP_EN)

J5 (CP_EN) is a 3-pin header used to enable or disable the internal charge pump of the TPS7A57.

The center pin of the 3-pin header is tied to the TPS7A57 CP_EN input. When the 2-pin shunt is placed across the bottom two pins of the header, VIN is shorted to CP_EN, and the internal charge pump is enabled. When the 2-pin shunt is placed across the top two pins of the header, GND is shorted to CP_EN, and the internal charge pump is disabled.

The CP_EN is shorted to GND as default. Short CP_EN to GND if an external VBIAS is applied.

For more information regarding the use of CP_EN and the internal charge pump, see the *TPS7A57* data sheet.

2.1.6 J1 (PG)

J1 (PG) is a 2-pin header used for the power-good (PG) feature of the TPS7A57 LDO.

When the 2-pin shunt is placed across the header, the PG pin is pulled up to VOUT using a 100-kΩ resistor.

For more information regarding PG functionality, see the *TPS7A57* data sheet.

2.2 Optional Load Transient Input and Output Connector Descriptions

2.2.1 VCC and GND

VCC (J7) and GND (J8) are the connection terminals for the input supply of the load transient circuit. The VCC terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.2.2 J17

J17 is an optional connection for the user to make measurements or apply DC loads to the output of the LDO.

2.2.3 TP10

TP10 is a test point that allows measurements of the load transient MOSFET drain voltage.

2.2.4 IN1

IN1 is the connection for the function generator to drive the gate driver device. IN1 is terminated by the 50-Ω resistor, R22.

2.2.5 J15

J15 is a high-frequency kelvin connection that allows accurate measurements of the load transient MOSFET gate to source voltage. Alternatively, J15 can be used to toggle the load transient MOSFET on and off by using a function generator if gate driver functionality is not desired.

2.2.6 TP11 and TP12

TP11 and TP12 allow the user to measure the gate drive resistance R21 when power is turned off to the EVM. The user can also measure the voltage before and after R21 when the gate driver is used.

2.2.7 J6 and TP13

TP13 is the enable pin to enable the gate driver device. Tie this pin to GND by creating a solder-short on J6 to enable the gate driver.

2.3 TPS7A57 LDO Operation

The TPS7A57EVM-056 evaluation module contains the TPS7A57 low-dropout regulator (LDO) with input and output capacitors installed. Additional pads are available to test the LDO with additional input and output capacitors beyond what is already installed on the EVM. The TPS7A57 LDO can be enabled or disabled by using the J4 3-pin header.

1. Placing a 2-pin shunt across the header to tie VIN to EN enables the device
2. Placing a 2-pin shunt across the header to tie GND to EN, or leaving the 3-pin header floating, disables the device
3. Placing a 2-pin shunt across the header to tie GND to CP_EN disables the internal charge pump

Alternatively, by connecting an external function generator to TP2 (EN) and a nearby GND, the user can enable or disable the TPS7A57 LDO after VIN is applied. Figure 2-1 shows the result of the TPS7A57EVM-056 during turn-on. The blue trace is the enable voltage and the pink trace is the output voltage.

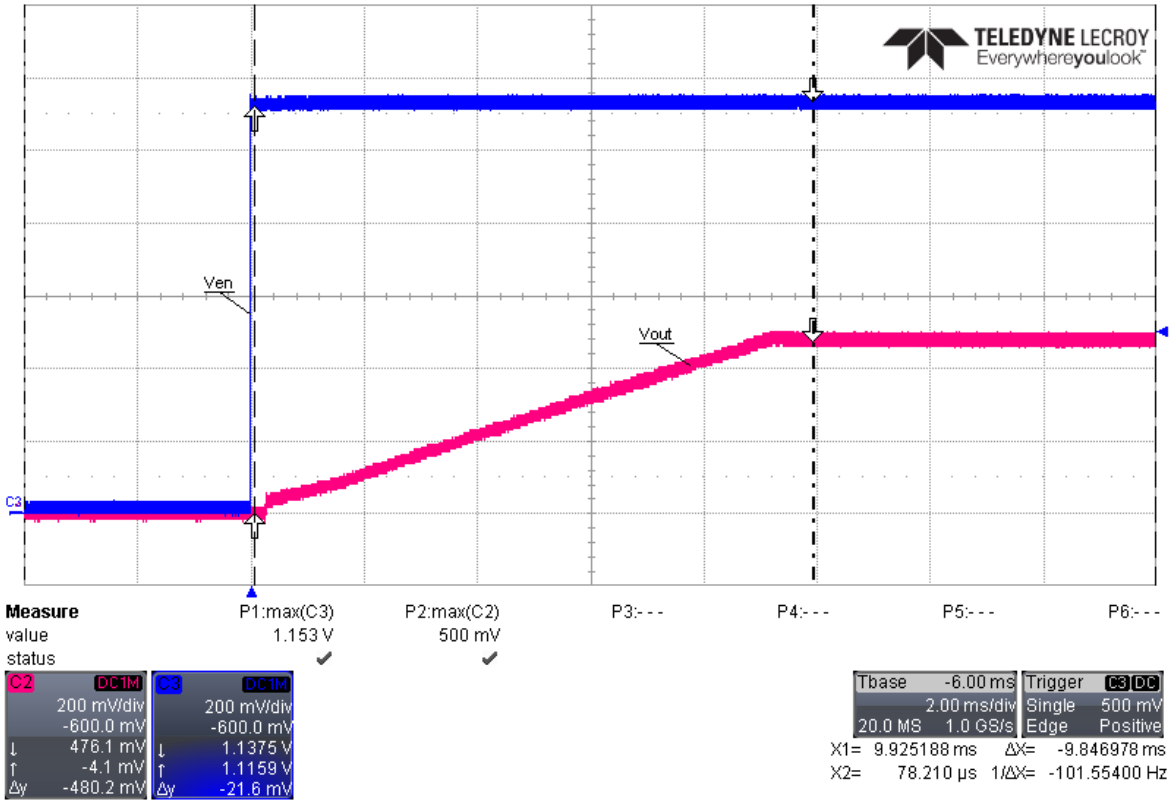

Figure 2-1. TPS7A57EVM-056 Turn On

If desired, a current probe can be inserted in the EVM as shown in Figure 2-2 to measure the output current. The slot was sized to fit most current probes, such as the LeCroy™ AP015 or CP031 current probes.

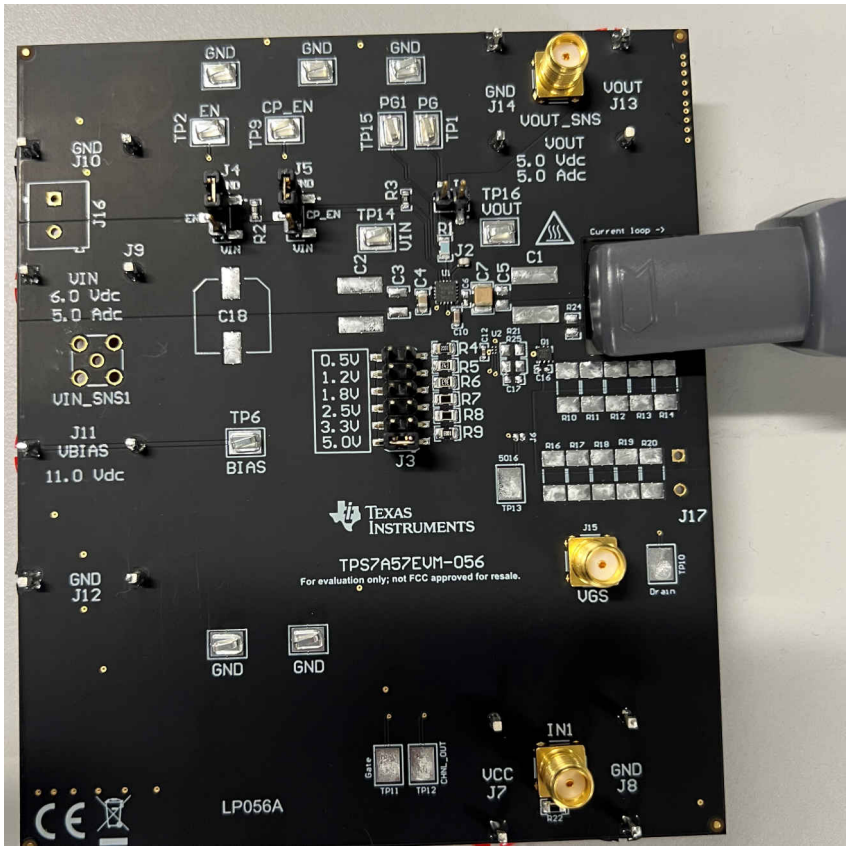

Figure 2-2. TPS7A57EVM-056 With Current Probe Attached

The user has three options for providing a DC load on the output of the TPS7A57. J17 can be used to place a DC load that flows through the current sense path and use the IOUT loop to measure the current. The second option is to use the R16, R17, R18, R19, and R20 footprints to place a DC load and use the IOUT loop to measure this current. Alternatively, the J13 (VOUT) and J14 (GND) banana connectors can be used for external measurements and loading; however, the IOUT loop does not sense current flowing through these connectors. In cases where very fast transient tests are performed, ringing may occur on VIN or VOUT as a result of the parasitic inductance within the PCB of the EVM. A strip of wire placed on the exposed copper in the current path can help reduce this ringing. Select the correct size of additional wire to fill the volume of the current probe. For most current probes, a 10 AWG wire can be used.

WARNING

The sensors of some current probes are tied to GND and cannot come into contact with energized conductors. See the user manual of your current probe for details. If your current probe has this limitation, use a thin strip of electrical or Kapton® tape to isolate the current sense path from the current probe.

Optional kelvin sense points are provided using the SMA connectors VIN_SNS1 and VOUT_SNS.

2.4 Optional Load Transient Circuit Operation

The TPS7A57EVM-056 evaluation module contains an optional high-performance load transient circuit to allow efficient testing of the TPS7A57 LDO load transient performance. To use the optional load transient circuit, install the correct components in accordance with the application. Modify the input and output capacitance connected to the TPS7A57 LDO to match the expected operating conditions. As given by Equation 1, determine the desired peak current to test and modify the parallel resistor combination of R10, 11, R12, R13, and R14.

$$I_{Peak} = \frac{V_{OUT}}{R_{10} \parallel R_{11} \parallel R_{12} \parallel R_{13} \parallel R_{14}} \quad (1)$$

The slew rate of the load step can be adjusted by C11, R15, and R21. In this section, only R21 is adjusted to set the slew rate. For a 0-mA to 5-A load step, use Table 2-1 to help select a value of R21 that results within a desired rise or fall time.

Table 2-1. Suggested Ramp Rate Resistor Values

R21	Rise Time	Fall Time
49.9 kΩ	11.5 µs	31 µs
30.9 kΩ	7.4 µs	19.7 µs
24.9 kΩ	6 µs	15.1 µs
21.5 kΩ	3.9 µs	14.8 µs
4.12 kΩ	980 ns	2.5 µs

After the EVM is modified (if needed), and if the LMG1020 gate driver is used, connect a power supply to banana connectors J7(VCC) and J8 (GND) with a 5-V DC supply and a 1-A DC current limit. As illustrated in Figure 2-3, the TPS7A57 transient response is very fast and the output voltage recovers in well under 1 ms after the initial load transient. Therefore, use a load transient pulse duration limit of 1 ms to prevent excessive heating of the pulsed resistors (R10, R11, R12, R13, and R14). Configure a function generator for the 50-Ω output, in a 0-V DC to 5-V DC square pulse. If necessary, burst mode can be configured in the function generator for repetitive, low duty cycle, load transient testing.

Figure 2-3 provides example test data with R21 = 21.5 kΩ. The blue trace is the output voltage and the green trace is the output current. R10, R11, R12, R13, and R14 provide 5-A of pulsed load. The resulting test data shows a 0-mA to 5-A load step on VOUT of the LDO, with only a 22-µF capacitor on the output of the LDO.

The load transient circuit also provides footprints to install a damping network as needed. Install R23 and C15 to create a damping network if needed.

Alternatively, load transient measurements can be achieved by solely using the pre-installed Q1 load transient MOSFET. J15 can be used to provide a signal to Q1 using a function generator. Figure 2-4 depicts results using the MOSFET without the LMG1020 gate driver at a 5-A load.

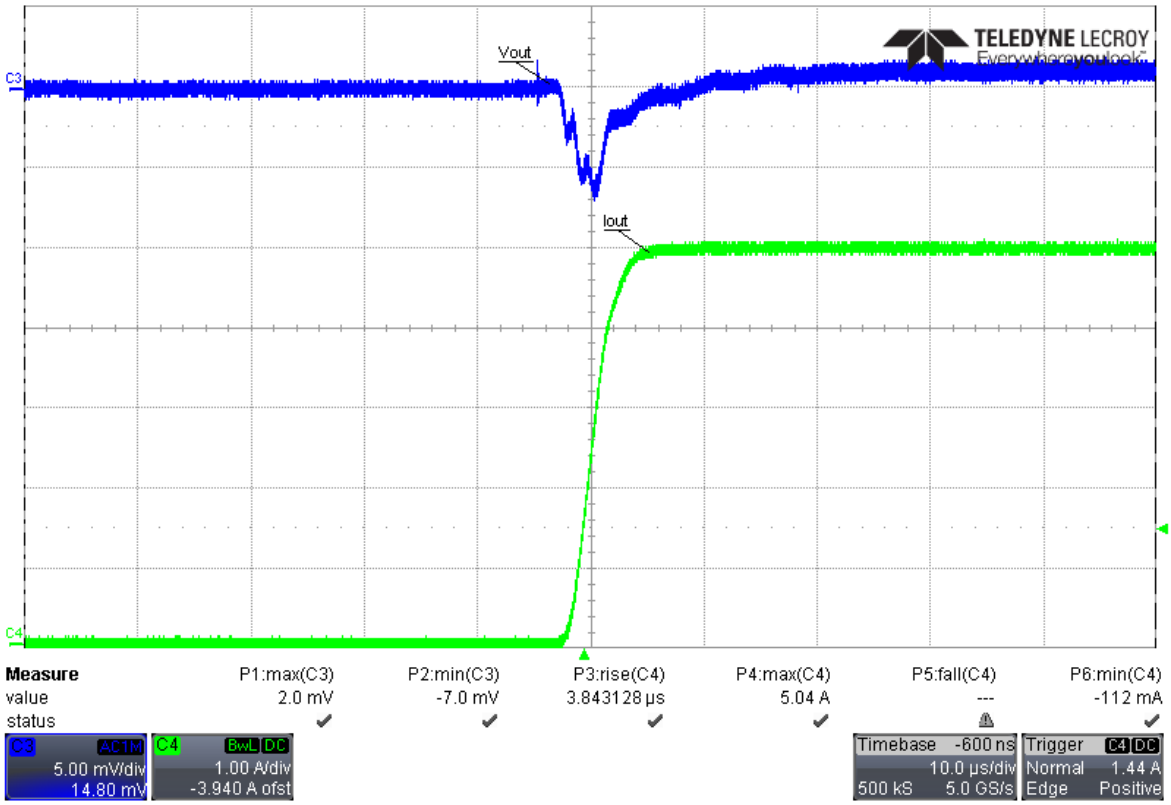

Figure 2-3. TPS7A57EVM-056 Load Transient Results

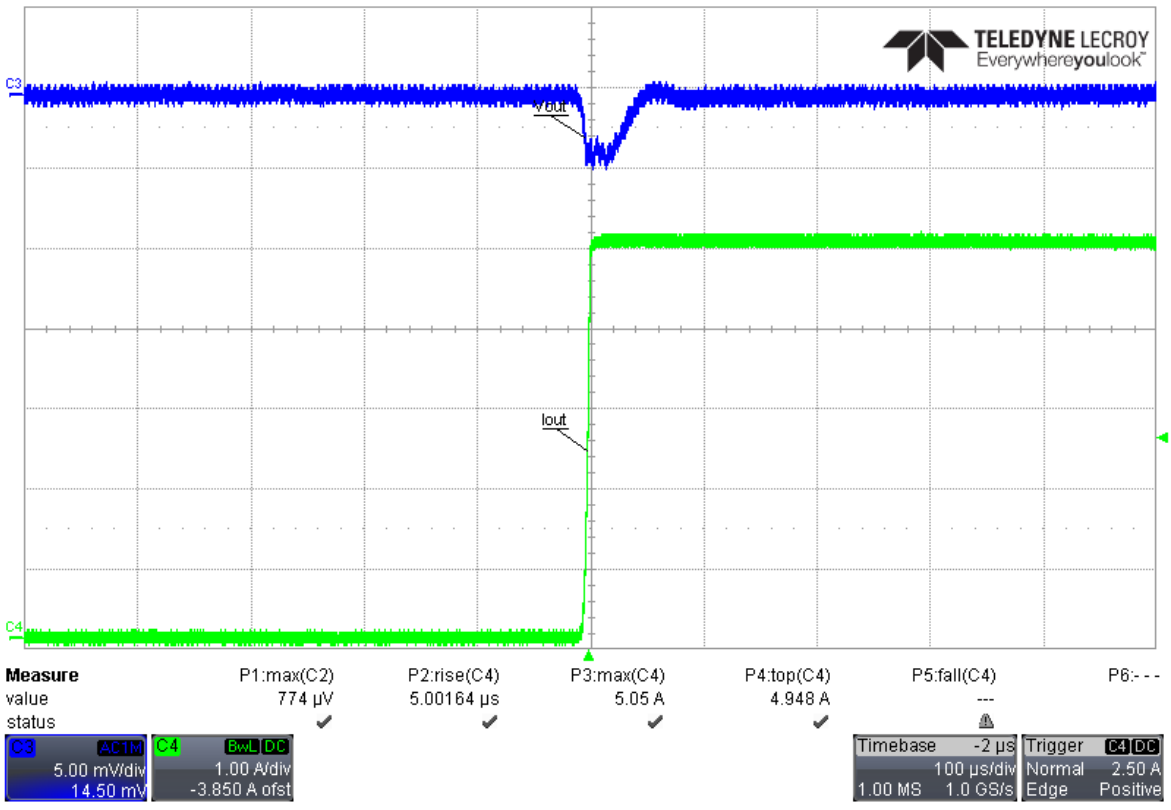

Figure 2-4. TPS7A57EVM-056 Load Transient Results With a Q1 MOSFET

3 Board Layout

Figure 3-1 through Figure 3-8 illustrate the board layout for the TPS7A57EVM-056 PCB.

The TPS7A57EVM-056 dissipates power, which may cause some components to experience an increase in temperature. The TPS7A57 LDO, LMG1020YFFR gate driver, and pulsed resistors R10, R11, R12, R13, and R14 are most at risk of raising to a high junction temperature during normal operation.

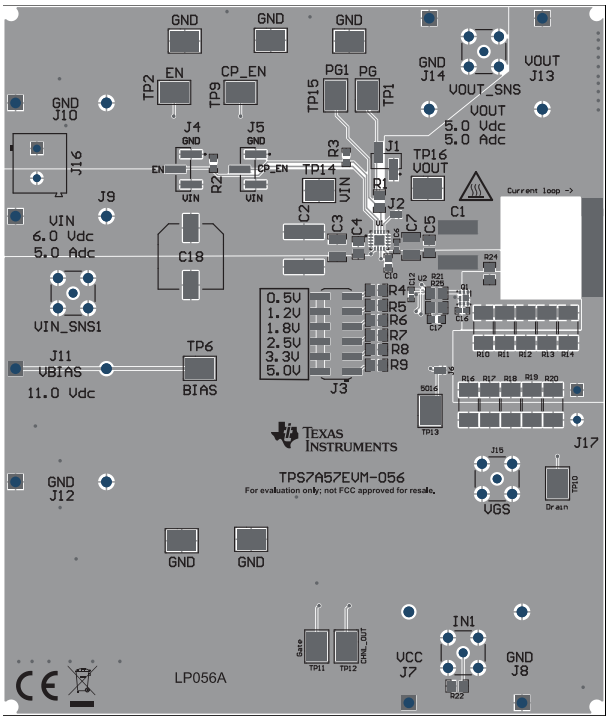

Figure 3-1. Top Assembly Layer and Silkscreen

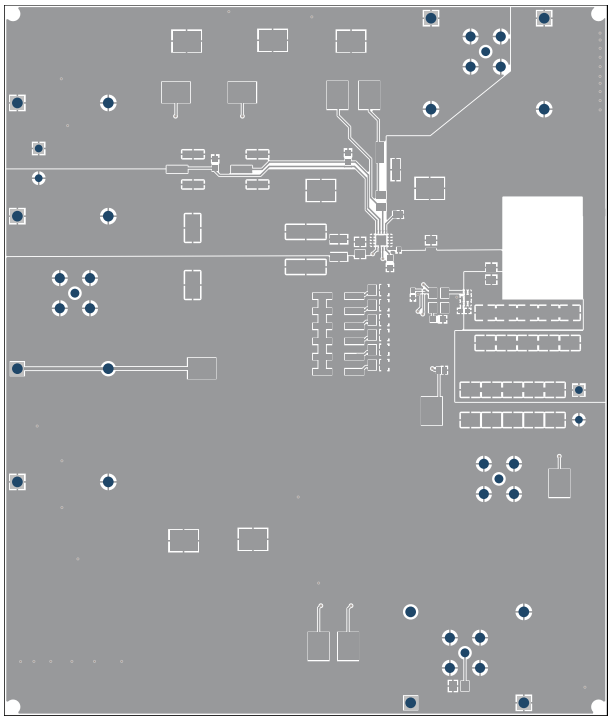

Figure 3-2. Top Layer Routing

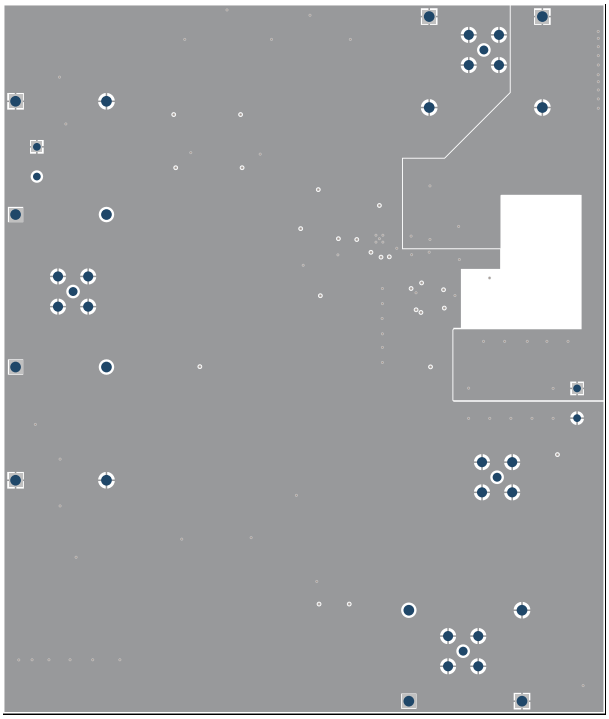

Figure 3-3. Layer 2

Figure 3-4. Layer 3

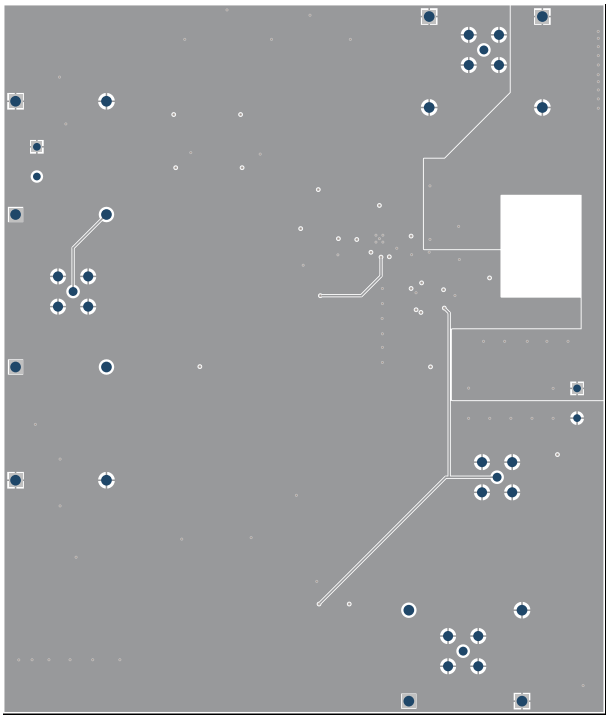

Figure 3-5. Layer 4

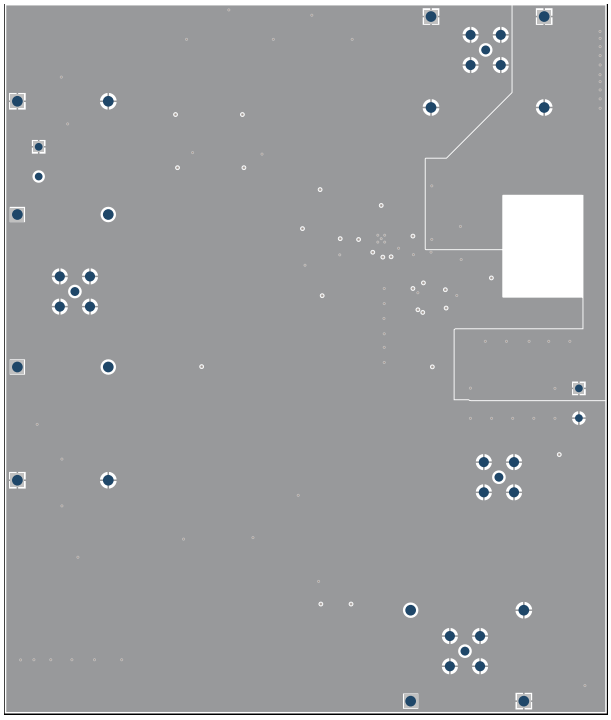

Figure 3-6. Layer 5

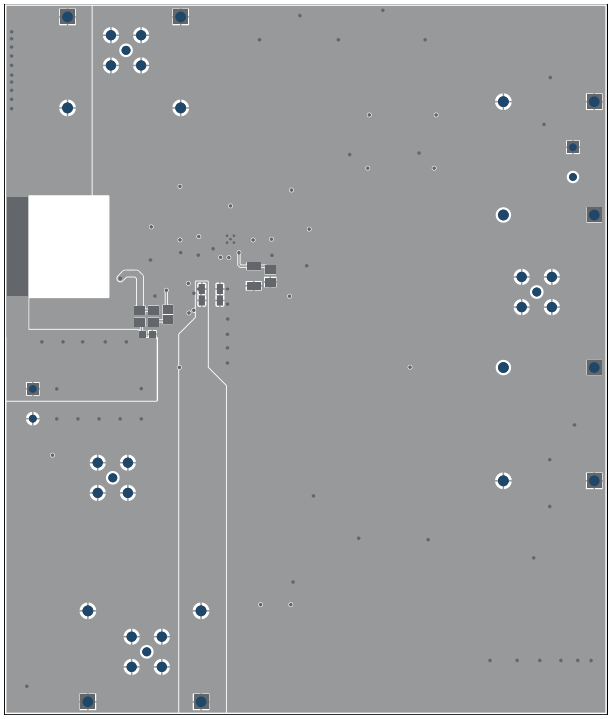

Figure 3-7. Bottom Layer Routing

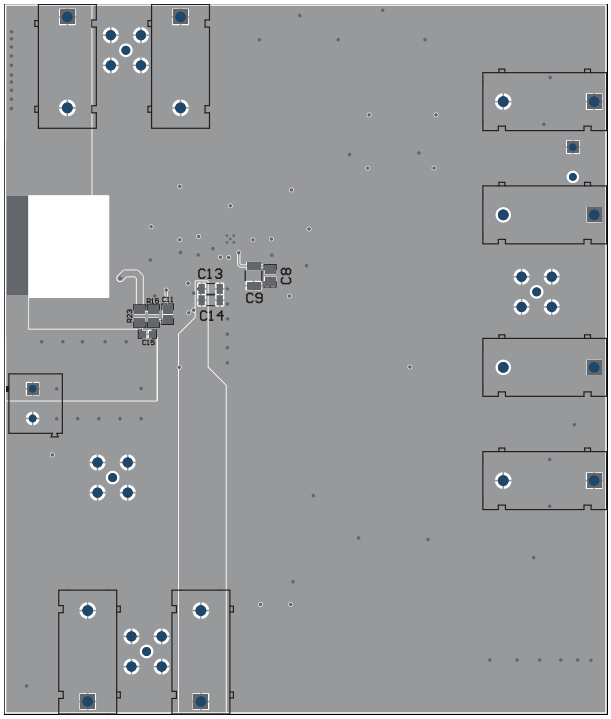

Figure 3-8. Bottom Assembly Layer and Silkscreen

4 TPS7A57EVM-056 Schematics

Figure 4-1 and Figure 4-2 illustrate schematics for the TPS7A57EVM-056 and the onboard load transient circuit, respectively.

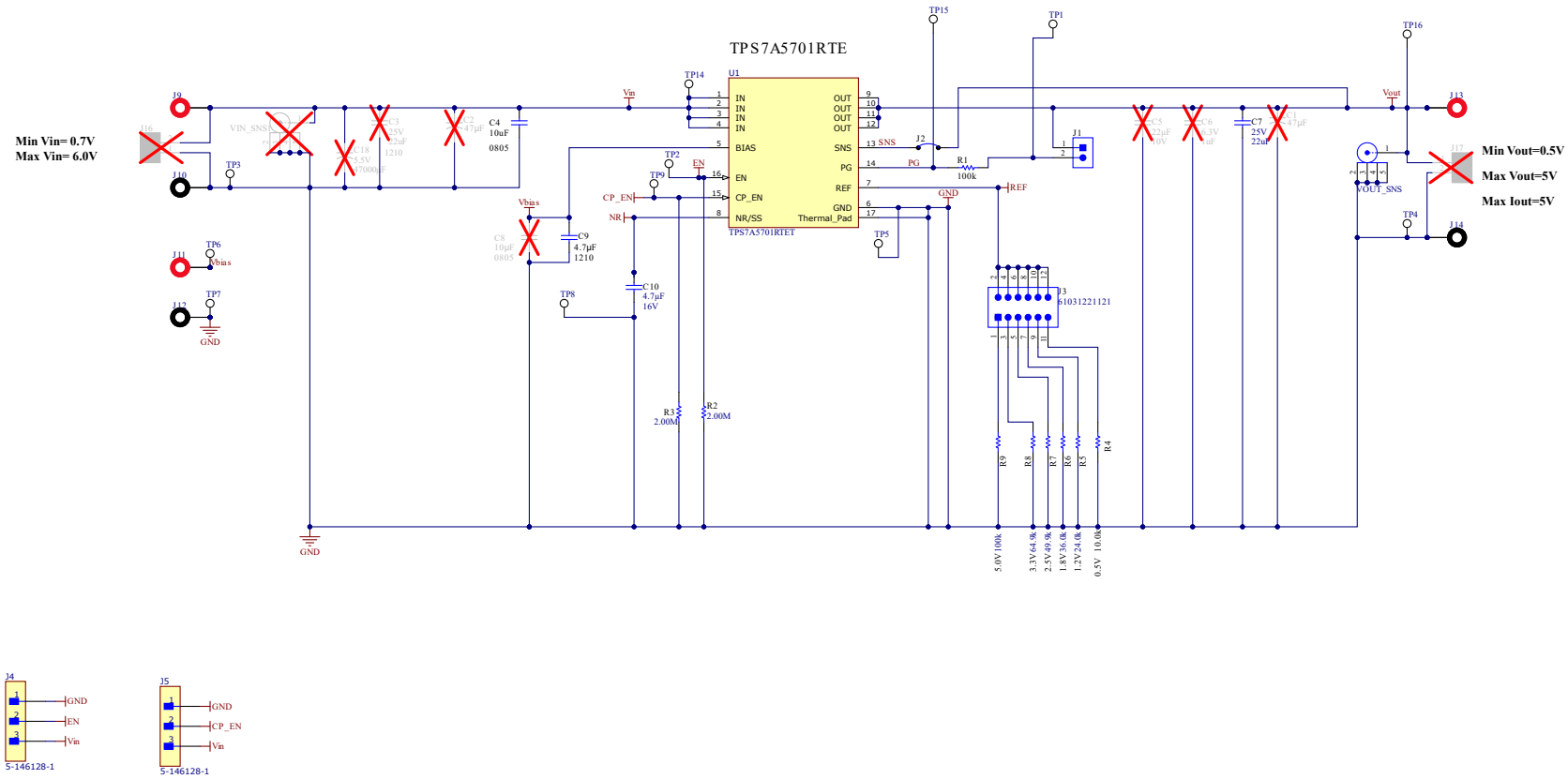

Figure 4-1. Schematic

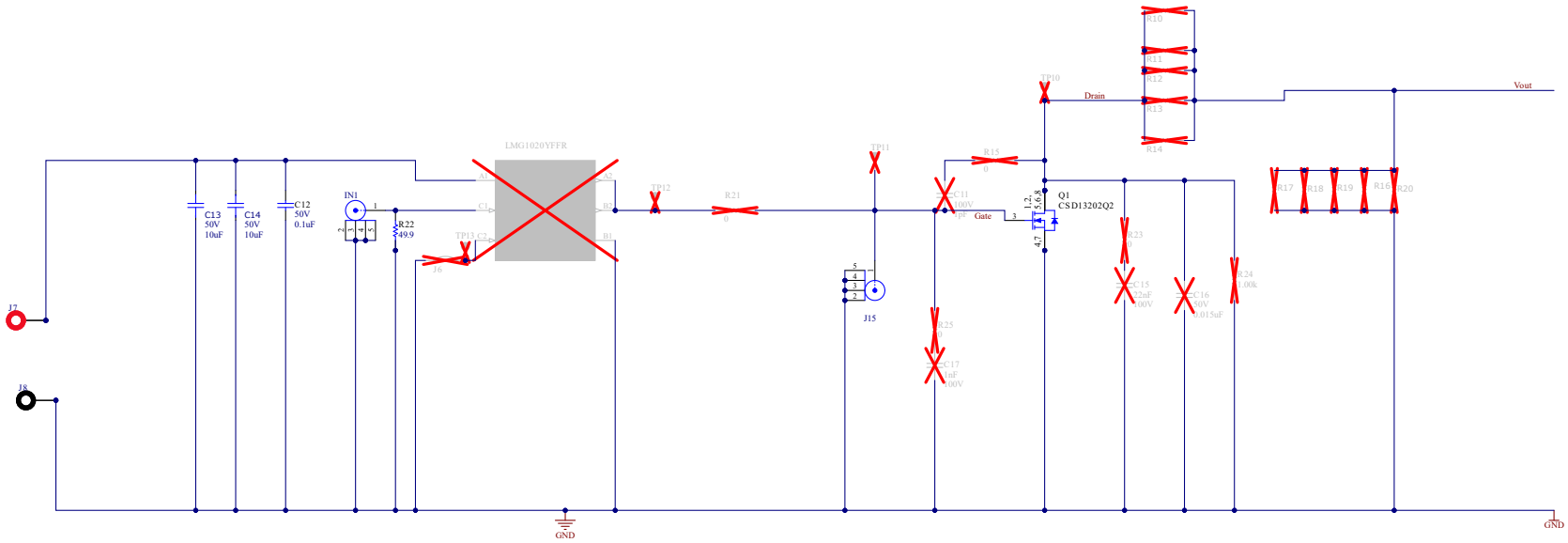

Figure 4-2. Load Transient Schematic

5 Bill of Materials

Table 5-1 shows the bill of materials for the TPS7A57EVM-056.

Table 5-1. Bill of Materials

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LP056	Any		
C4	1	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 0805	805	GRM21BZ71E106KE15L	MuRata		
C7	1	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata		
C9	1	4.7uF	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X8R, AEC-Q200 Grade 0, 1210	1210	CGA6P3X8R1E475K250AB	TDK		
C10	1	4.7uF	CAP, CERM, 4.7 uF, 16 V,+/- 10%, X7R, 0603	603	GRM188Z71C475KE21D	MuRata		
C12	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	402	C1005X7R1H104K050BB	TDK		
C13, C14	2	10µF	10 µF ±10% 50V Ceramic Capacitor X7R 1206 (3216 Metric)	1206	GMC31X7R106K50NT	Cal-Chip Electronics		
IN1, J15, VOUT_SNS	3		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
FID1, FID2, FID3, FID4	4		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1	1		Header, 100mil, 2x1, Tin, SMD	SMD, 2-Leads, Body 200x100mil	TSM-102-01-T-SV-P-TR	Samtec		
J2	1		Jumper, SMT	shorting jumper, SMT	JMP-36-30X40SMT	Any		
J3	1		Header, 2.54mm, 6x2, Gold, SMT	Header, 2.54mm, 6x2, Gold, TH	61031221121	Wurth Elektronik		
J4, J5	2		Headers & Wire Housings 1X03P .1 230/SMT HDR VT 30AU	HDR3		TE		
J7, J9, J11, J13	4		Standard Banana Jack, insulated, 10A, red	571-0500	571-0500	DEM Manufacturing		
J8, J10, J12, J14	4		Standard Banana Jack, insulated, 10A, black	571-0100	571-0100	DEM Manufacturing		
Q1	1	12V	MOSFET, N-CH, 12 V, 22 A, DQK0006C (WSON-6)	DQK0006C	CSD13202Q2	Texas Instruments		
R1	1	100k	RES, 100 k, 1%, 0.2 W, 0805	805	MCU08050C1003FP500	Vishay/Beyschlag		
R2, R3	2	2.00Meg	RES, 2.00 M, 1%, 0.1 W, 0603	603	RC0603FR-072ML	Yageo		
R4	1	10.0k	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	CRCW080510K0FKEA	Vishay-Dale		
R5	1	24.0k	RES, 24.0 k, 0.5%, 0.1 W, 0805	805	RR1220P-243-D	Susumu Co Ltd		
R6	1	36.0k	RES, 36.0 k, 0.5%, 0.1 W, 0805	805	RR1220P-363-D	Susumu Co Ltd		

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R7	1	49.9k	RES, 49.9 k, 0.5%, 0.1 W, 0805	805	RR1220P-4992-D-M	Susumu Co Ltd		
R8	1	64.9k	RES, 64.9 k, 0.1%, 0.125 W, 0805	805	RG2012P-6492-B-T5	Susumu Co Ltd		
R9	1	100k	RES, 100 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEYJ104V	Panasonic		
R22	1	49.9	RES, 49.9, 1%, 0.15 W, 0805	805	M55342K06B49D9T	TT Electronics/IRC		
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP14, TP15, TP16	12		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U1	1		5-A, Low-VIN (0.7V), Low-Noise, High-Accuracy, Ultra-Low Dropout (LDO) Voltage Regulator	WQFN16	TPS7A5701RTET	Texas Instruments		
C1, C2	0	47uF	CAP, TA, 47 µF, 50 V, +/- 10%, 0.24 ohm, SMD	6.2x6mm	597D476X9050Z2T	Vishay-Sprague		
C3	0	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	1210	GRM32ER71E226KE15L	MuRata		
C5	0	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X7R, 0805	805	GRM21BZ71A226ME15L	MuRata		
C6	0	1uF	CAP, CERM, 1 uF, 6.3 V,+/- 10%, X7R, 0402	402	GRM155R70J105KA12D	MuRata		
C8	0	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 0805	805	GRM21BZ71E106KE15L	MuRata		
C11	0	1pF	CAP, CERM, 1 pF, 100 V, +/- 5%, C0G/NP0, 0805	805	GQM2195C2A1R0CB01D	MuRata		
C15	0	0.022uF	CAP, CERM, 0.022 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	603	CGA3E2X7R2A223K080AA	TDK		
C16	0	0.015uF	CAP, CERM, 0.015 uF, 50 V, +/- 10%, X7R, 0402	402	GRM155R71H153KA12D	MuRata		
C17	0	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	603	06031C102JAT2A	AVX		
C18	0	47000uF	CAP, Electric Double Layer, 47000 µF, 5.5 V,+80/-20%, 50 ohm, D10.5xL5.5mm SMD	D10.5xL5.5mm	FC0H473ZFTBR24	Kemet		
J6	0		Jumper, SMT	shorting jumper, SMT	JMP-36-30X40SMT	Any		
J16, J17	0		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik		
R10, R11, R12, R13, R14, R16, R17, R18, R19, R20	0	8.2	8.2 Ohms ±1% 6W Chip Resistor 2512 (6432 Metric) Flame Proof, Moisture Resistant, Non-Magnetic, Safety Thin Film	2512	PCNM2512K8R20FST5	Vishay		
R15, R21, R23, R25	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic		

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R24	0	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1001V	Panasonic		
TP10, TP11, TP12, TP13	0		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U2	0		5V, 7A/5A Low Side GaN Driver With 60MHz/1ns Speed, YFF0006AEAE (DSBGA-6)	YFF0006AEAE	LMG1020YFFR	Texas Instruments	LMG1020YFFT	
VIN_SNS1,	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		

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