CDCM9102EVM Clock Evaluation Module

CDCM9102EVM is the evaluation module (EVM) for the CDCM9102, a low-jitter clock generator that provides reference clocks for communications standards such as PCI Express. This clock generator is easy to configure and use. It provides two, 100-MHz, differential clock ports. The supported output types for these ports include LVPECL, LVDS, or a pair of LVCMOS buffers. An ac-coupled network supports HCSL signaling. The user configures the desired output buffer type by strapping device pins. Additionally, the EVM has a single-ended, 25-MHz clock output port. Uses for this port include general-purpose clocking, clocking Ethernet PHYs, or providing a reference clock for additional clock generators. All generated clocks derive from a single, 25-MHz crystal that is external to the device. This fully assembled and factory-tested evaluation board allows complete validation of all device functions.

Contents

List of Figures

List of Tables

1 Features

- Easy-to-use evaluation module (EVM) to generate clock signals with low jitter and phase noise
- Easy device setup
- Control pins configurable through jumpers
- Requires 3.3-V power supply
- Single-ended or crystal input clock reference
- Termination available for LVPECL, LVDS, and LVCMOS output clocks

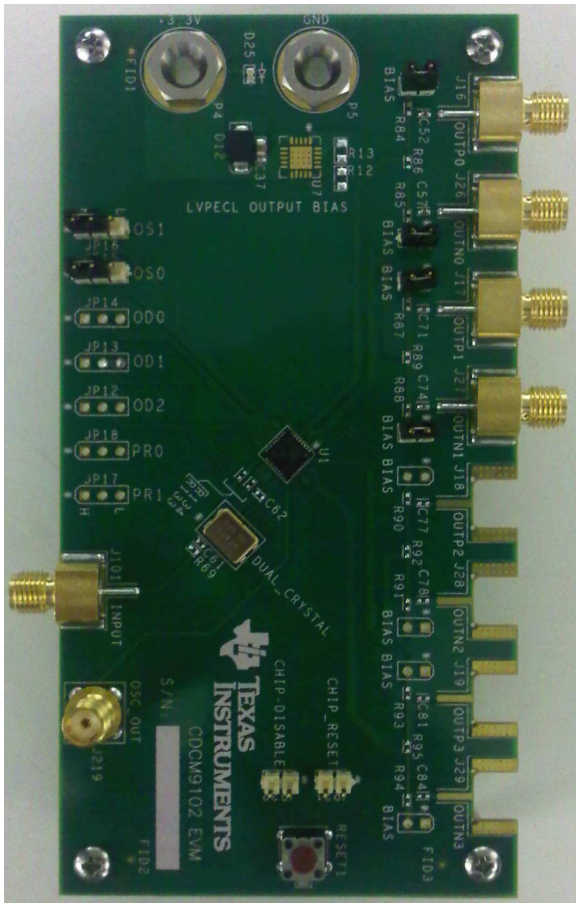


Figure 1. CDCM9102EVM Evaluation Module

2 General Description

The CDCM9102 is a high-performance, low-phase-noise clock generator. The CDCM9102 has one crystal and low-voltage CMOS (LVCMOS) input buffer and two universal outputs.

This device is a programmable clock generator with control pins only. No EEPROM or programming interface is necessary to program these devices.

For optimum performance, the EVM has 50-Ω SMA connectors and well-controlled, 50-Ω-impedance microstrip transmission lines.

For additional information about the CDCM9102 device, see the data sheet *Low-Noise Two-Channel 100-MHz Clock Generator* (SCAS922).

3 Signal Path and Control Circuitry

The CDCM9102 supports either a crystal input or a single-ended clock with a 25-MHz input frequency. Supported output types include LVPECL, LVDS, and LVCMOS. An optional bypassed LVCMOS output is also available.

4 Getting Started

The EVM has self-explanatory labeling. Additionally, the naming conventions for the EVM correspond to those in the device data sheet. Words in ***bold italics*** in this document show the same name and label as on the EVM board. The EVM can use either a crystal input or external, single-ended clock input.

4.1 Power-Supply Connection

Connect the power-supply source to the banana plug with a ***3.3V*** (P4) label, and connect the ground of the power-supply source to ***GND (P5)***. Decoupling capacitors and ferrite bead isolate the device power pins dedicated for the PLL from the other power pins.

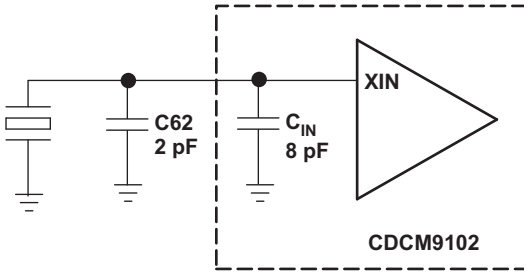
This EVM can operate from a 3-V to 3.6-V supply voltage.

5 Input Clock Selection

The CDCM9102EVM offers the options to use either a crystal or a single-ended clock source as the clock input.

5.1 Configuring a Crystal Input

The EVM is available with an optional 25-MHz crystal. The EVM offers a dual footprint for a 6-pin (5 mm x 7 mm) and 4-pin (3 mm x 5 mm) crystal. For a parallel-load resonant crystal, the configuration must be similar to that in Figure 2.



NOTE: This configuration assumes that the crystal is placed very close to the XIN pin on the device.

Figure 2. CDCM9102EVM Configuration With Parallel-Load Resonant Crystal Clock Source

5.2 Configuring a Single-Ended Input

For a single-ended clock input, remove the crystal if the board already has one. Use the SMA connector J101 for a single-ended input clock. Place a 50-Ω resistor in R69 if a signal generator provides the clock, and if the signal generator requires a 50-Ω load for its operation. If another board or the LVCMOS buffer provides the input clock, do not place any resistor here. For an external clock, set the input signal swing to ***2.5V*** (and not ***3.3V***, as the input is only compatible with 2.5-V input signals), and set the input signal frequency to 25 MHz.

Capacitor ***C61*** (100 nF) is necessary for ac coupling, (Figure 3).

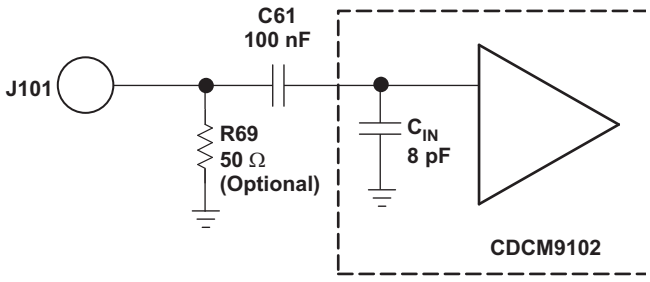


Figure 3. Single-Ended Connection Configuration

6 Operating Mode Selection

The CDCM9102 is a PLL-based device and offers multiple modes of operation.

6.1 Output Buffer Type Selection

JP16 (OS1) and ***JP15 (OS0)*** are the jumpers for output buffer selection (LVCMOS, LVDS, or LVPECL). Each output pair provides two, in-phase LVCMOS clocks.

Table 1 shows the output buffer options.

Table 1. Output Buffer Options[(1)]

Control Inputs		Output Type
OS1	OS0	
0	0	LVCMOS, OSC_OUT Off
0	1	LVDS, OSC_OUT Off
1	0	LVPECL, OSC_OUT Off
1	1	LVPECL, OSC_OUT On

(1) A bypassed output (same as the reference clock frequency) is only available with LVPECL outputs.

6.2 Using ENABLE and RESET Pins

JP22 (CHIP_DISABLE) is the jumper for the OE pin. This pin has an internal 150-kΩ pullup resistor; use the internal pullup resistor only for logic *1*.

Table 2 summarizes the power-down configuration.

Table 2. Power-Down Configuration

OE (Pin 7)	Mode	Device Core	Output
0	Power down	Power down	Hi-Z
1	Normal	Active	Active

Do not connect this jumper for normal operation.

The RESET pin connects to both ***CHIP_RESET*** jumper ***JP21*** and push-button switch ***RESET1***. Either option can reset the device (including recalibrating the PLL).

Table 3 summarizes the RESET configuration options.

Table 3. Reset Configuration

RESET (Pin 12)	Operating Mode	Device Output
0	Device reset	Hi-Z
0 → 1	Clock generator calibration	Hi-Z
1	Normal	Active

7 Output Buffer Termination

This EVM supports proper termination for all three types of output buffers. To ensure that the chosen output buffer works properly with the correct termination, select or place the proper components. Figure 4 shows different ways to terminate the outputs of the device.

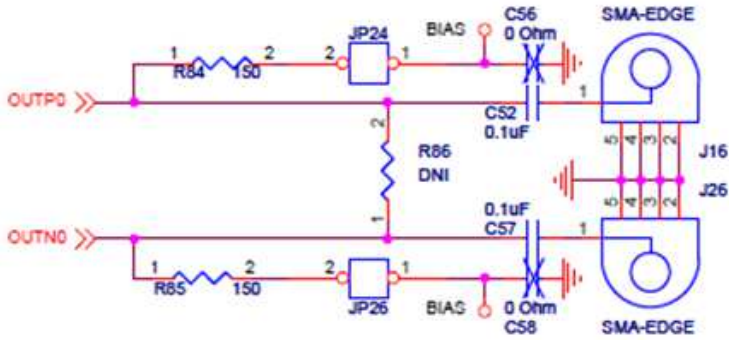


Figure 4. EVM Output Termination Options

7.1 Output Buffer Examples

LVPECL Output Buffer: Use jumpers ***J24*** and ***J26***.

LVDS Output Buffer: Remove jumpers ***J24*** and ***J26***. Place a 100-Ω resistor at the R85 placeholder, if necessary. If the output pair connects to an oscilloscope through 50-Ω SMA cables, then the oscilloscope 50-Ω to ground connection takes care of this termination, and the 100-Ω resistor is no longer necessary.

LVCMOS Output Buffer: This LVCMOS buffer typically has 30-Ω internal impedance. For a 50-Ω impedance characteristic line, use an external 22-Ω series resistor. For an SMA connection to an oscilloscope, connect the output as ac-coupled (using ***C52, C57, C71,*** and ***C74***). A lower-than-expected swing occurs because the LVCMOS driver is not capable of driving a 50-Ω to ground load.

7.2 Availability of Optional Output

An optional bypassed output (***OSC_OUT***) is only available if the user chooses the PLL output(s) at an LVPECL signaling level. ***J219*** is the SMA for this output.

8 Schematic

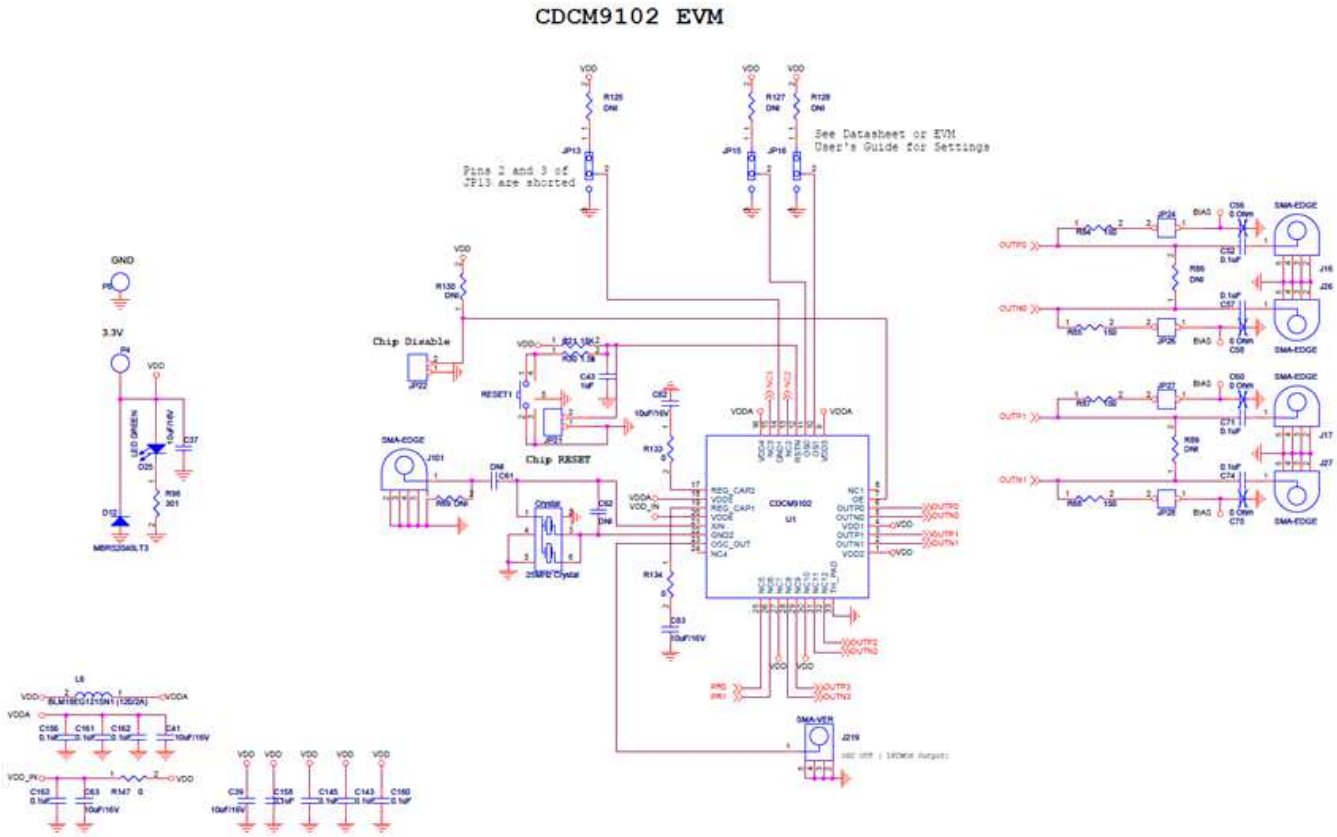


Figure 5. CDCM9102EVM Schematic

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FCC Interference Statement for Class B EVM devices

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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Concerning EVMs including radio transmitters

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This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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For EVMs annotated as IC – INDUSTRY CANADA Compliant

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Concerning EVMs including radio transmitters

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Concerning EVMs including detachable antennas

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1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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