# User's Guide TMUX-24PW-EVM User's Guide

# TEXAS INSTRUMENTS

### ABSTRACT

This document is the EVM user's guide for the TMUX-24PW-EVM, which provides a quick way to evaluate TI devices that use a 24-pin PW package.

# **Table of Contents**

2 General Texas Instruments High Voltage Evaluation Module (TI HV EVM) User Safety Guidelines       5         3 Information About Cautions and Warnings       6         4 Features       6         5 TMUX-24PW-EVM Header Connections and Test Points       7         6 TMUX-24PW-EVM Setup       10         7 Layout       12         8 Schematics       13         9 Bill of Materials       17         10 Revision History       18	1 Introduction	2
4 Features 6 5 TMUX-24PW-EVM Header Connections and Test Points 7 6 TMUX-24PW-EVM Setup 10 7 Layout 12 8 Schematics 13 9 Bill of Materials 17	2 General Texas Instruments High Voltage Evaluation Module (TI HV EVM) User Safety Guidelines	5
5 TMUX-24PW-EVM Header Connections and Test Points	3 Information About Cautions and Warnings	6
6 TMUX-24PW-EVM Setup	4 Features	6
7 Layout 12 8 Schematics 13 9 Bill of Materials 17	5 TMUX-24PW-EVM Header Connections and Test Points	7
8 Schematics	6 TMUX-24PW-EVM Setup	10
9 Bill of Materials	7 Layout	12
	8 Schematics	13
10 Revision History	9 Bill of Materials	17
	10 Revision History	18

# **List of Figures**

Figure 1-1. TMUX-24PW-EVM Top View	2
Figure 1-2. TMUX-24PW-EVM Bottom View	. 3
Figure 1-3. TMUX-24PW-EVM 3D View	.4
Figure 5-1. Header J3 for U1.3	.7
Figure 5-2. Pinout of Headers	7
Figure 5-3. Test Point Colors	
Figure 6-1. DUT Footprint U1	10
Figure 6-2. Signal Line Circuitry (3D)	10
Figure 6-3. Signal Line Circuitry	11
Figure 6-4. Signal Line Circuitry Bottom Layer	11
Figure 7-1. Illustration of TMUX-24PW-EVM Layout	12
Figure 8-1. TMUX-24PW-EVM Schematic Page 1 (Editor View)	13
Figure 8-2. TMUX-24PW-EVM Schematic Page 2 (Editor View)	14
Figure 8-3. TMUX-24PW-EVM Schematic Page 1 (DNI)	
Figure 8-4. TMUX-24PW-EVM Schematic Page 2 (DNI)	16

# **List of Tables**

Table 5-1. Connections by Header Pin Number	7
Table 5-2. Test Point Connections	8
Table 9-1. TMUX-24PW-EVM Bill of Materials	.17

# Trademarks

All trademarks are the property of their respective owners.



# **1** Introduction

This user's guide describes the TMUX-24PW-EVM evaluation module (EVM) and its intended use. This board allows for the quick prototyping and DC characterization of TI's line of TMUX products that use 24-pin TSSOP packages (PW).

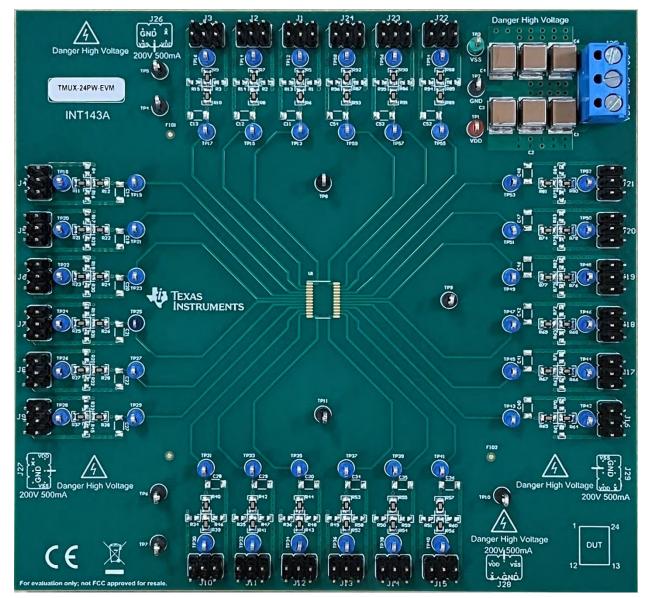


Figure 1-1. TMUX-24PW-EVM Top View



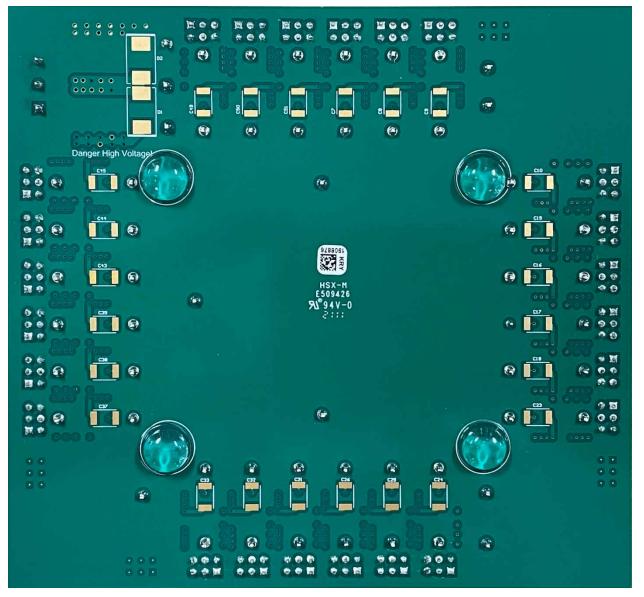


Figure 1-2. TMUX-24PW-EVM Bottom View





Figure 1-3. TMUX-24PW-EVM 3D View



# 2 General Texas Instruments High Voltage Evaluation Module (TI HV EVM) User Safety Guidelines



Always follow TI's setup and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http:// support/ti./com for further information.

#### Save all warnings and instructions for future reference.

#### WARNING

Failure to follow warnings and instructions may result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic product typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

- 1. Work Area Safety
  - a. Keep work area clean and orderly.
  - b. One or more qualified observers must be present anytime circuits are energized.
  - c. Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
  - d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
  - e. Use stable and nonconductive work surface.
  - f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.

#### 2. Electrical Safety

As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.

- a. De-energize the TI HV EVM and all its inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
- b. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment connection, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
- c. After EVM readiness is complete, energize the EVM as intended.

#### WARNING

While the EVM is energized, never touch the EVM or its electrical circuits, as they could be at high voltages capable of causing electrical shock hazard.

- 3. Personal Safety
  - a. Wear personal protective equipment (for example, latex gloves or safety glasses with side shields) or protect EVM in an adequate lucent plastic box with interlocks to protect from accidental touch.

#### Limitation for safe use:

EVMs are not to be used as all or part of a production unit.



# **3 Information About Cautions and Warnings**

The information in the warning statement is provided for personal protection and the information in the caution statement is provided to protect the equipment from damage. Read each caution and warning statement carefully.



#### CAUTION

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, see <u>Electrostatic Discharge (ESD)</u>.

# 4 Features

The TMUX-24PW-EVM has the following features:

- 3 power supply decoupling capacitors from VDD to GND (3 × 3.3 μF)
- 1 protection diode pad from VDD to GND available near power supply (6.9 mm × 5.8 mm)
- 3 power supply decoupling capacitors from VSS to GND (3 × 3.3 μF)
- 1 protection diode pad from VSS to GND available near power supply (6.9 mm × 5.8 mm)
- Terminal block power supply connection
- DUT footprint compatible with 24-pin PW (TSSOP) packages
- 24 length-matched signal inputs corresponding to the 24 pins of the DUT
- Selectable connections to VDD, VSS, or GND for each signal input using 2.54 mm shunt
- Footprints for pull-up and pull-down resistors for each signal input (2 × 0603 footprint on each of 24 signals)
- Footprints for series resistors for each signal input (2 × 0805 footprint on each of 24 signals)
- Footprints for decoupling capacitors for each input (1 × 1206 footprint and 1 × 1812 footprint on each of 24 signals)
- 2 test points for each signal input
- Multiple GND test point connections around board



## 5 TMUX-24PW-EVM Header Connections and Test Points

There are 24 headers located around the board with designators J1 through J24. These 3-by-2 headers serve as connections to power planes and to signals of the DUT (U1). Each pin of the DUT has similar header and test point configuration. At four different locations around the board, a legend shows the connections of the pins of the nearby five headers. Figure 5-1 shows a representation of the header associated with pin 3 of U1.

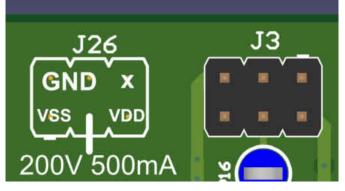


Figure 5-1. Header J3 for U1.3

The silkscreen legend represents the connections of the pins of J3. Figure 5-2 shows the pin numbers of this header from this same perspective.

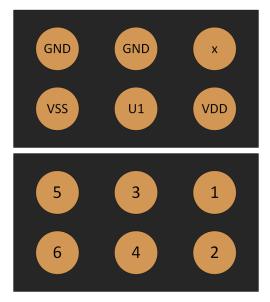


Figure 5-2. Pinout of Headers

Table 5-1 also shows the connections.

······································			
Header pin number	Connection		
1	No connection		
2	VDD		
3	GND		
4	U1		
5	GND		
6	VSS		
L			

For all headers J1 through J24, the connections are the same, but are rotated by a multiple of 90° according to their position on the board. A legend is included for each rotation.

7



In addition to headers, multiple test points are located around the board. Black test points (TP2 and TP4-TP11) are connected to GND, the red test point (TP1) is connected to VDD, and the green test point (TP3) is connected to VSS. The remaining blue test points (TP12-TP59) are connected along the signal paths of the pins of U1.

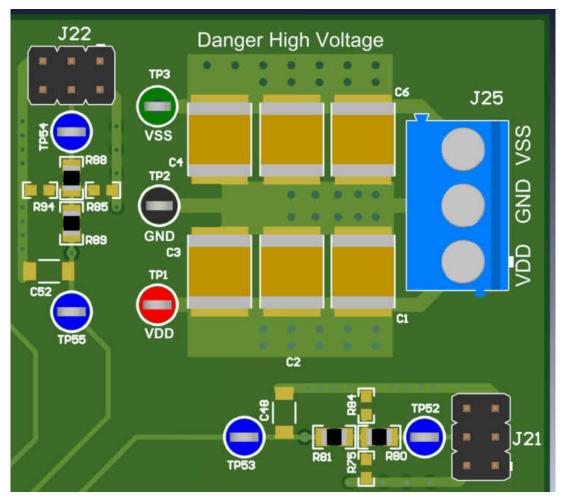


Figure 5-3. Test Point Colors

Table 5-2 shows the test point connections.

#### Table 5-2. Test Point Connections

Designator	Connection
TP1	VDD
TP2	GND
TP3	VSS
TP4	GND
TP5	GND
TP6	GND
TP7	GND
TP8	GND
TP9	GND
TP10	GND
TP11	GND
TP12	J1.4
TP13	U1.1
TP14	J2.4

Table 5-2. Test Point Connections (continue           Designator         Connection			
TP15	U1.2		
TP16	J3.4		
TP17	U1.3		
TP18	J4.4		
TP19	U1.4		
TP20	J5.4		
TP21	U1.5		
TP22	J6.4		
TP23	U1.6		
TP24	J7.4		
TP25	U1.7		
TP26	J8.4		
TP27	U1.8		
TP28	J9.4		
TP29	U1.9		
TP30	J10.4		
TP31	U1.10		
TP32	J11.4		
TP33	U1.11		
TP34	J12.4		
TP35	U1.12		
TP36	J13.4		
TP37	U1.13		
TP38	J14.4		
TP39	U1.14		
TP40	J15.4		
TP41	U1.15		
TP42	J16.4		
TP43	U1.16		
TP44	J17.4		
TP45	U1.17		
TP46	J18.4		
TP47	U1.18		
TP48	J19.4		
TP49	U1.19		
TP50	J20.4		
TP51	U1.20		
TP52	J21.4		
TP53	U1.21		
TP54	J22.4		
TP55	U1.22		
TP56	J23.4		
TP57	U1.23		
TP58	J24.4		
TP59	U1.24		

#### Table 5-2. Test Point Connections (continued)



Terminal block J25 is the power input for the board. Three power rails (VSS, GND, and VDD) are labeled on the board's silkscreen layer, indicating the identities of the input pins of the header. Connect the power supply rails at this terminal block to power the board.

### 6 TMUX-24PW-EVM Setup

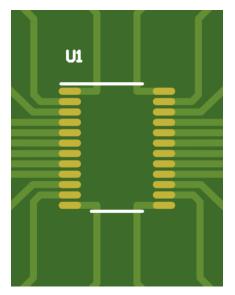


Figure 6-1. DUT Footprint U1

The TMUX-24PW-EVM will not have any device connected at footprint U1, and there are not any devices included with the EVM for this footprint. Attach any compatible Texas Instruments TMUX device to this location, which will serve as the Device Under Test (DUT). Compatible devices include 24-pin parts with PW package names.

The headers of the TMUX-24PW-EVM can be easily connected to a power rail using 2.54 mm shunts on J1-J24. Connecting the shunt between pin 4 of the header and pin 3 (GND) to connect the corresponding pin of U1 to GND. Alternatively, the pins of U1 can be shorted to VDD or VSS by connecting between pin 4 of the header and pin 2 or pin 6 respectively. Figure 5-2 and Table 5-1 includes detailed descriptions of the connections on J1 through J24.



Figure 6-2. Signal Line Circuitry (3D)

As shown in Figure 6-2 and Figure 6-3 as R4 and R16 on the J4 (pin 4 of U1) signal line, the TMUX-24PW-EVM includes 0  $\Omega$  series resistors (0805 package) on each signal line.



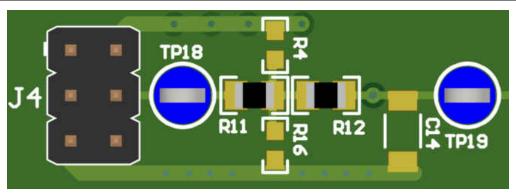


Figure 6-3. Signal Line Circuitry

These can be substituted for different resistors as desired. Additionally, there are pads for pull-up and pull-down resistors to VDD and GND respectively. Add any 0603 resistor to the footprint shown as R4 to provide pull-up to VDD, and add any 0603 resistor to the footprint shown as R16 to provide pull-down to GND.

Each signal line also includes two footprints that allow for the user to attach capacitors or other devices with matching footprints. On the top side of the board, shown in Figure 6-2 and Figure 6-3 as C14, a standard 1206 footprint exists between the U1 pin signal and the GND signal. The user can solder a capacitor to this footprint to provide capacitance to the signal line.

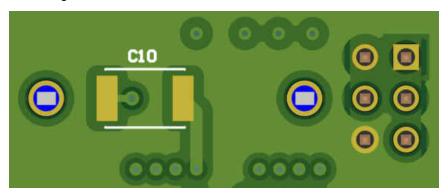


Figure 6-4. Signal Line Circuitry Bottom Layer

On the back side of the board, shown in Figure 6-4 as C10, a standard 1812 footprint exists, also allowing for connection of a capacitor between the U1 pin signal and GND. The user can solder a capacitor to this footprint to provide capacitance to the signal line.

# 7 Layout

Figure 7-1 shows the layout of the EVM PCB.

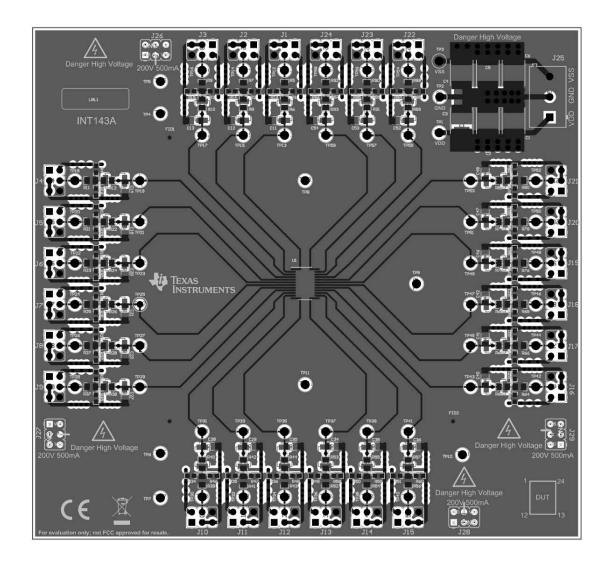
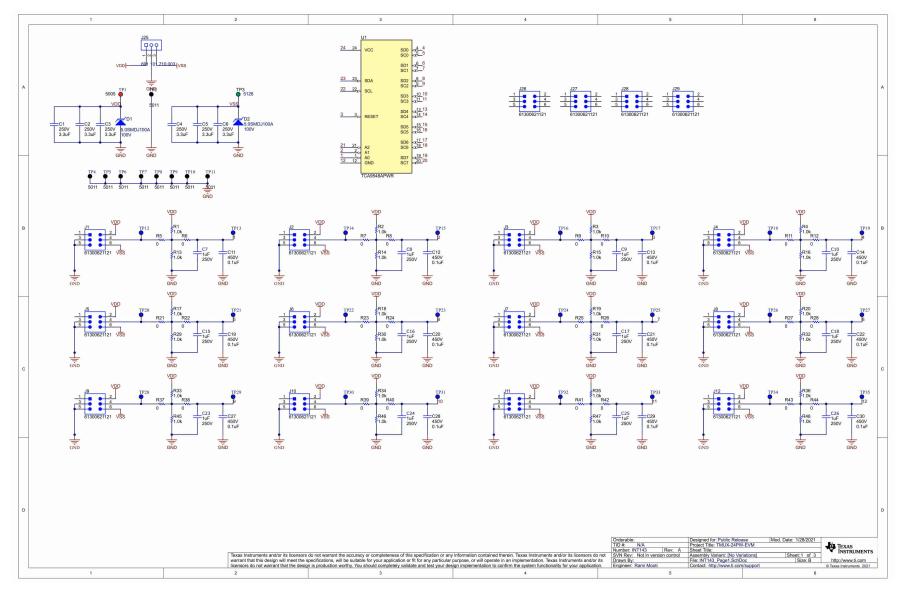


Figure 7-1. Illustration of TMUX-24PW-EVM Layout



# 8 Schematics

Figure 8-1 and Figure 8-2 are schematic views of the TMUX-24PW-EVM that includes all the parts and connections.







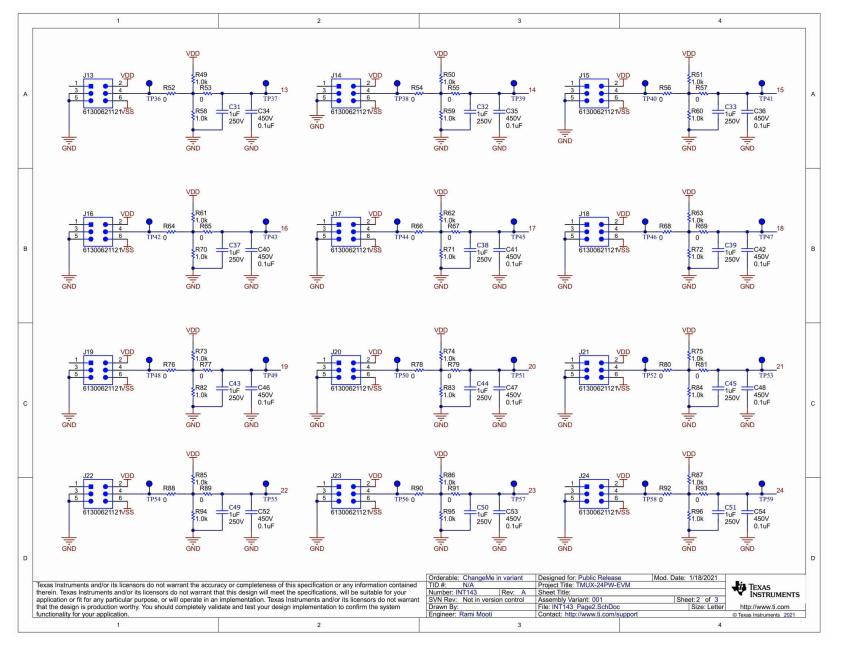
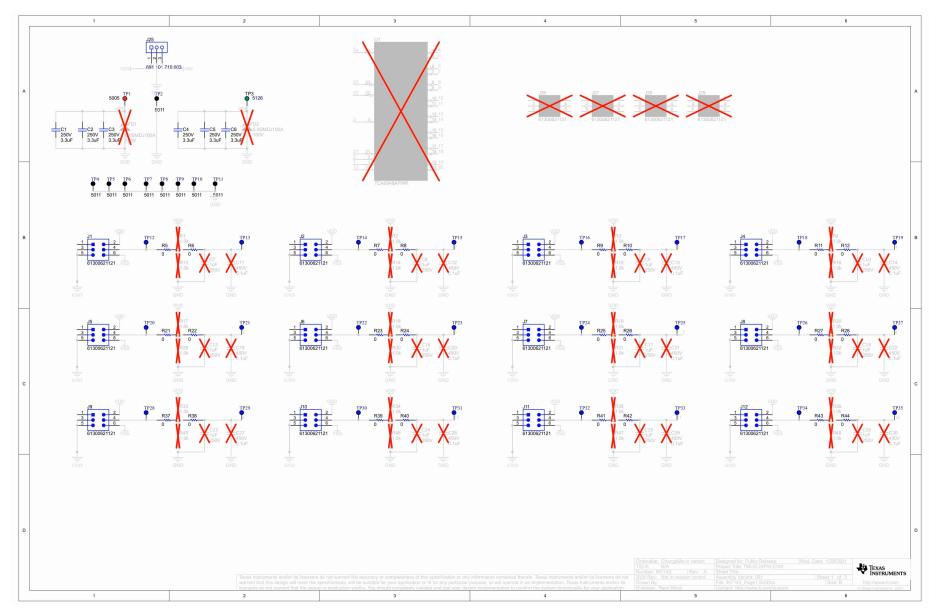


Figure 8-2. TMUX-24PW-EVM Schematic Page 2 (Editor View)



Figure 8-3 and Figure 8-4 are schematic views of the TMUX-24PW-EVM that show only the parts that are included in the EVM and excludes the parts that are DNI.





Layout

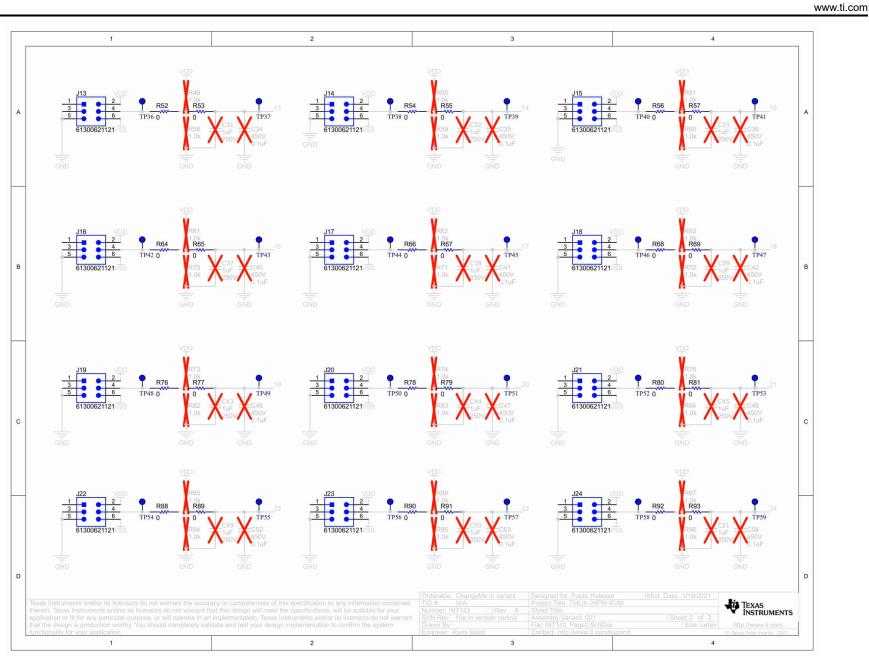


Figure 8-4. TMUX-24PW-EVM Schematic Page 2 (DNI)

- ji

**T**EXAS

INSTRUMENTS



# 9 Bill of Materials

Designator	Component	Manufacturer	Description	Quantity	
C1, C2, C3, C4, C5, C6	CKG57NX7T2E335M500J H	ТDК	CAP, CERM, 3.3 μF, 250 V, ± 20%, X7T, AEC-Q200 Grade 1, 6×5×5 mm	6	
H1, H2, H3, H4	SJ-5303 (CLEAR)	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear	4	
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24	61300621121	Wurth Elektronik	Header, 2.54 mm, 3×2, Gold, TH	24	
J25	691 101 710 003	Wurth Elektronik	Terminal Block, 5 mm, 3×1, Tin, TH	1	
LBL1	THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	1	
R5, R6, R7, R8, R9, R10, R11, R12, R21, R22, R23, R24, R25, R26, R27, R28, R37, R38, R39, R40, R41, R42, R43, R44, R52, R53, R54, R55, R56, R57, R64, R65, R66, R67, R68, R69, R76, R77, R78, R79, R80, R81, R88, R89, R90, R91, R92, R93	PMR10EZPJ000	Rohm	RES, 0, 0%, W, AEC- Q200 Grade 0, 0805	48	
TP1	5005	Keystone	Test Point, Compact, Red, TH	1	
TP2, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11	5011	Keystone	Test Point, Multipurpose, Black, TH	9	
TP3	5126	Keystone	Test Point, Multipurpose, Green, TH	1	
TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP54, TP55, TP56, TP57, TP58, TP59	5122	Keystone	Test Point, Compact, Blue, TH	48	

#### Table 9-1. TMUX-24PW-EVM Bill of Materials



**10 Revision History** NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2021	*	Initial Release

### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2022, Texas Instruments Incorporated