

XIO2200A Implementation Guide

Interface Business Unit

ABSTRACT

This document is provided to assist platform designers using the XIO2200A PCI Express to PCI Translation Bridge with 1394a OHCI and two-port PHY. Detailed information can be found in the XIO2200A Data Manual. However, this document provides board design suggestions for the various device features when designing in the XIO2200A.

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1 XIO2200A Typical System Implementation

Figure 1 represents a typical implementation of the XIO2200A PCI Express to PCI Translation Bridge with 1394a OHCI and two-port PHY. This solution provides robust PCI Express link to 1394a cable port protocol conversion in a single semiconductor package. The XIO2200A operates only with the PCI Express link as the primary interface and the 1394a cable ports as the secondary interface.

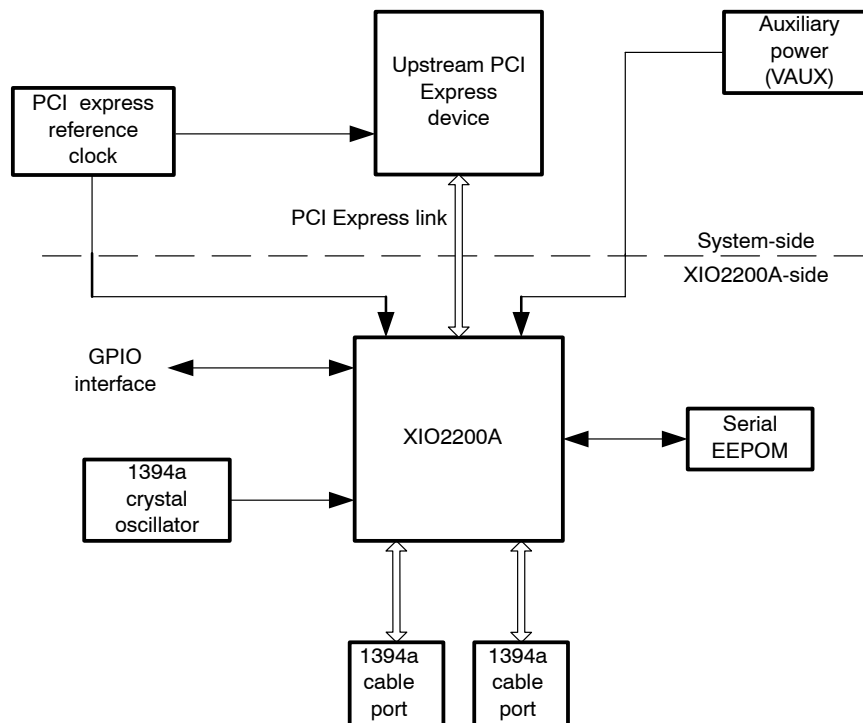


Figure 1. Typical System Implementation

Either a common differential 100-MHz PCI Express reference clock or an asynchronous single-ended 125-MHz reference clock is supported. Figure 1 illustrates the common 100-MHz reference clock option.

The 1394a core requires the standard 24.576-MHz crystal oscillator as described in the 1394a specification.

If V_{AUX} power states are a system requirement, then the XIO2200A maintains the necessary information in sticky configuration register bits.

The EEPROM can be used to set various configuration registers, but is not necessary if those registers are settable via system software/BIOS.

Up to eight general-purpose inputs and outputs (GPIO) exist for further system customization.

2 Power Considerations

2.1 1.5-V and 3.3-V Digital Supplies

The 1.5-V terminals are named V_{DD15} . These terminals supply power to the digital core. The 1.5-V core allows for a significant reduction in both power consumption and logic switching noise.

The 3.3-V terminals are named V_{DD33} and supply power to most of the input and output cells.

Both the V_{DD15} and V_{DD33} supplies must have 0.1- μ F bypass capacitors to V_{SS} (ground) in order for proper operation. The recommendation is one capacitor for each power terminal.

The circuit board via associated with the H14 terminal pad must connect to a 1000-pF bypass capacitor. The other side of the capacitor must connect to V_{SS} (ground) for proper operation. When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

2.2 1.5-V and 3.3-V Analog Supplies

Both 1.5-V and 3.3-V analog power is required by the XIO2200A. Since circuit noise on the analog power terminals must be minimized, the following Pi filters are recommended.

1. All V_{DDA15} terminals must be connected together and share a Pi filter.
2. All V_{DDA33} terminals must be connected together and share a Pi filter.

Both the 1.5-V and 3.3-V analog supplies must have 0.1- μ F bypass capacitors connected to V_{SSA} (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. In addition, one 1000-pF capacitor per Pi filter is recommended. This 1000-pF capacitor is attached to the device side of the Pi filter and to V_{SSA} (ground). High-speed board design rules must be followed when connecting bypass capacitors to V_{DDA} and V_{SSA} .

2.3 Combined Power Outputs

To support V_{AUX} system requirements, the XIO2200A internally combines main power with V_{AUX} power. There are three combined power rails in the XIO2200A. These three power rails are distributed to the analog circuits, digital logic, and I/O cells that must operate during the V_{AUX} state. Each of the three power rails has an output terminal for the external attachment of bypass capacitors to minimize circuit switching noise. These terminals are named V_{DD15_COMB} , V_{DD33_COMB} , and V_{DD33_COMBIO} .

The recommended bypass capacitors for each combined output terminal are 1000 pF, 0.01 μ F, and 1.0 μ F. When placing these capacitors on the bottom side of the circuit board, the smallest value capacitor is positioned next to the via associated with the combined output terminal and the largest value capacitor is the most distant from the via. The circuit board trace width connecting the combined output terminal via to the capacitors must be at least 12 to 15 mils wide with the trace length as short as possible.

Other than the three recommended capacitors, no other external components are attached to these combined output terminals.

2.4 Auxiliary Power

If V_{AUX} power is available in the system, the XIO2200A has the V_{DD33_AUX} terminal to support this feature. Without fully understanding a system's V_{AUX} power distribution design, recommending external components for the XIO2200A is difficult. At a minimum, a 0.1- μ F bypass capacitor is placed near the XIO2200A and attached to the system's V_{AUX} power supply. A robust design may include a Pi filter with bulk capacitors (5 μ F to 100 μ F) to minimize voltage fluctuations. When the system is cycling main power or is in the V_{AUX} state, the V_{DD33_AUX} terminal requirements are that the input voltage cannot exceed 3.6-V or drop below 3.0-V for proper operation of the bridge.

If V_{AUX} power is not present within the system, this terminal is connected to V_{SS} thru a resistor with a value greater than 3.0 k Ω .

2.5 V_{SS} and V_{SSA} Terminals

For proper operation of the XIO2200A, we recommend a unified V_{SS} and V_{SSA} ground plane. The circuit board stack-up recommendation is to implement a layer 2 ground plane directly under the XIO2200A device. Both the circuit board vias and ground trace widths that connect the V_{SS} and V_{SSA} ball pads to this ground plane must be oversized to provide a low-impedance connection.

2.6 Capacitor Selection Recommendations

When selecting bypass capacitors for the XIO2200A device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low-frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell "D" size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. These bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

2.7 Power-Up/-Down Sequencing

All XIO2200A analog and digital power terminals must be controlled during the power-up and power-down sequence. During power sequencing, all power terminals must remain within 3.6-V to prevent damaging the XIO2200A.

For additional power sequencing requirements, see the XIO2200A Data Manual (SCPS098) and the *PCI-Express Card Electromechanical Specification*, Revision 1.0a.

NOTE: The power sequencing recommendations in this section exclude the $V_{DD_33_AUX}$ terminal.

2.8 Power Supply Filtering Recommendations

To meet the PCI-Express and 1394a OHCI jitter specifications, low-noise power supplies are required on several of the XIO2200A voltage terminals. The power terminals that require low-noise power include V_{DDA_5} and V_{DDA33} . This section provides guidelines for the filter design to create low-noise power sources.

The least expensive solution for low-noise power sources is to filter existing 3.3-V and 1.5-V power supplies. This solution requires analysis of the noise frequencies present on the power supplies. The XIO2200A has external interfaces operating at clock rates of 100 MHz, 125 MHz, 200 MHz, 400 MHz, and 2.5 GHz. Other devices located near the XIO2200A may produce switching noise at different frequencies. Also, the power supplies that generate the 3.3-V and 1.5-V power rails may add ripple noise. Linear regulators have feedback loops that typically operate in the 100-kHz range. Switching power supplies typically have operating frequencies in the 500-kHz range. When analyzing power supply noise frequencies, the first, third, and fifth harmonic of every clock source must be considered.

Critical analog circuits within the XIO2200A must be shielded from this power supply noise. The fundamental requirement for a filter design is to reduce power supply noise to a peak-to-peak amplitude of less than 25 millivolts. This maximum noise amplitude should apply to all frequencies from 0 Hz to 6.25 GHz.

The following information should be considered when designing a power supply filter:

1. Ideally, the series resonance frequency for each filter component should be greater than the fifth harmonic of the maximum clock frequency. With a maximum clock frequency of 1.25 GHz, the third harmonic is 3.75 GHz and the fifth harmonic is 6.25 GHz. Finding inductors and capacitors with a series resonance frequency above 6.25 GHz is both difficult and expensive. Components with a series resonance frequency in the 4 to 6 GHz range are a good compromise.
2. The inductor(s) associated with the filter must have a DC resistance low enough to pass the required current for the connected power terminals. The voltage drop across the inductor must be low enough to meet the minus 10% voltage margin requirement associated with each XIO2200A power terminal. Power supply output voltage variation must be considered as well as voltage drops associated with any connector pins and circuit board power distribution geometries.
3. The Q versus frequency curve associated with the inductor must be appropriate to reduce power terminal noise to less than the maximum peak-to-peak amplitude requirement for the XIO2200A. Recommending a specific inductor is difficult because every system design is different and therefore the noise frequencies and noise amplitudes are different. Many factors will influence the inductor selection for the filter design. Power supplies must have adequate input and output filtering. A sufficient number of bulk and bypass capacitors are required to minimize switching noise. Assuming that board level power is properly filtered

and minimal low frequency noise is present, frequencies less than 10 MHz, an inductor with a Q greater than 20 from approximately 10 MHz to 3 GHz should be adequate for most system applications.

4. The series component(s) in the filter may either be an inductor or a ferrite bead. Testing has been performed on both component types. When measuring PCI-Express link jitter, the inductor or ferrite bead solutions produce equal results. When measuring circuit board EMI, the ferrite bead is a superior solution. Note: The XIO2200A reference schematics include ferrite beads in the analog power supply filters.
5. When designing filters associated with power distribution, the power supply is a low impedance source and the device power terminals are a low impedance load. The best filter for this application is a “T” filter. Please see Figure 2 for a T filter circuit. Some system may require this type of filter design if the power supplies or nearby components are exceptionally noisy. This type of filter design is recommended if a significant amount of low frequency noise, frequencies less than 10 MHz, is present in a system.
6. For most applications a “Pi” filter will be adequate. Please see Figure 2 for a Pi filter circuit. When implementing a Pi filter, the two capacitors and the inductor must be located next to each other on the circuit board and must be connected together with wide low impedance traces. Capacitor ground connections must be short and low impedance.
7. If a significant amount of high frequency noise, frequencies greater than 300 MHz, is present in a system, creating an internal circuit board capacitor will help reduce this noise. This is accomplished by locating power and ground planes next to each other in the circuit board stack-up. A gap of 0.003 mils between the power and ground planes will significantly reduce this high frequency noise.
8. Another option for filtering high-frequency logic noise is to create an internal board capacitor using signal layer copper plates. When a component requires a low-noise power supply, usually the Pi filter is located near the component. Directly under the Pi filter, a plate capacitor may be created. In the circuit board stack-up, select a signal layer that is physically located next to a ground plane. Then, generate an internal 0.25 inch by 0.25 inch plate on that signal layer. Assuming a 0.006-mil gap between the signal layer plate and the internal ground plane, this will generate a 12-pF capacitor. By connecting this plate capacitor to the trace between the Pi filter and the component’s power terminals, an internal circuit board high frequency bypass capacitor is created. This solution is extremely effective for switching frequencies above 300 MHz.

Figure 2 illustrates two different filter designs that may be used with the XIO2200A to provide low-noise power to critical power terminals.

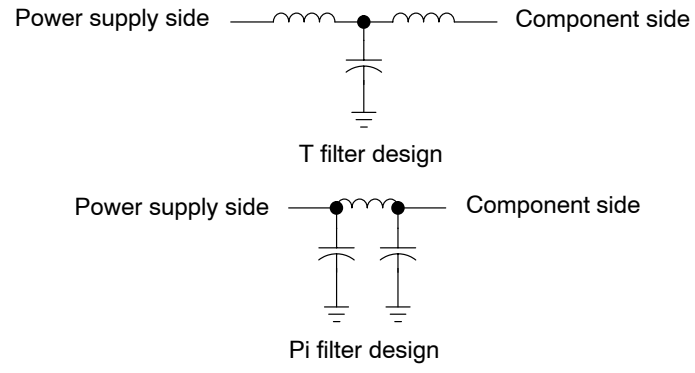


Figure 2. Filter Designs

3 PCI Express Interface Considerations

The XIO2200A has an x1 PCI Express interface that is fully compliant to the *PCI Express Base Specification*, Revision 1.0a. The remainder of this chapter describes implementation considerations for the XIO2200A's primary PCI Express interface.

3.1 2.5 Gbps Transmit and Receive Link

The XIO2200A TX and RX terminals attach to the upstream PCI Express device over a 2.5 Gbps high-speed differential transmit and receive PCI Express x1 Link. The connection details are provided in the following table.

XIO2200A Terminal Name	Upstream PCI Express Device Terminal Name	Comments
TXP (H17)	RXP	XIO2200A's transmit positive differential terminal connects to the upstream device's receive positive differential terminal.
TXN (H16)	RXN	XIO2200A's transmit negative differential terminal connects to the upstream device's receive negative differential terminal.
RXP (E17)	TXP	XIO2200A's receive positive differential terminal connects to the upstream device's transmit positive differential terminal.
RXN (E16)	TXN	XIO2200A's receive negative differential terminal connects to the upstream device's transmit negative differential terminal.

The XIO2200A TXP and TXN terminals comprise a low-voltage, 100- Ω , differentially driven, signal pair. The RXP and RXN terminals for the XIO2200A receive a low-voltage, 100- Ω , differentially driven, signal pair. The XIO2200A has integrated 50- Ω termination resistors to V_{SS} on both the RXP and RXN terminals eliminating the need for external components.

Each lane of the differential signal pair must be ac-coupled. The recommended value for the series capacitor is 0.1 μ F. To minimize stray capacitance associated with the series capacitor circuit board solder pads, 0402-sized capacitors are recommended.

When routing a 2.5-Gb/s low-voltage, 100- Ω differentially driven signal pair, the following circuit board design guidelines must be considered:

1. The PCI-Express drivers and receivers are designed to operate with adequate bit error rate margins over a 20" maximum length signal pair routed through FR4 circuit board material.
2. Each differential signal pair must be 100- Ω differential impedance with each single-ended lane measuring in the range of 50- Ω to 55- Ω impedance to ground.
3. The differential signal trace lengths associated with a PCI Express high-speed link must be length matched to minimize signal jitter. This length matching requirement applies only to the P and N signals within a differential pair. The transmitter differential pair does not need to be length matched to the receiver differential pair. The absolute maximum trace length difference between the TXP signal and TXN signal must be less than 5 mils. This also applies to the RXP and RXN signal pair.
4. If a differential signal pair is broken into segments by vias, series capacitors, or connectors, the length of the positive signal trace must be length matched to the negative signal trace for each segment. Trace length differences over all segments are additive and must be less than 5 mils.

5. The location of the series capacitors is critical. For add-in cards, the series capacitors are located between the TXP/TXN terminals and the PCI-Express connector. In addition, the capacitors are placed near the PCI Express connector. This translates to two capacitors on the motherboard for the downstream link and two capacitors on the add-in card for the upstream link. If both the upstream device and the downstream device reside on the same circuit board, the capacitors are located near the TXP/TXN terminals for each link.
6. The number of vias must be minimized. Each signal trace via reduces the maximum trace length by approximately 2 inches. For example: If 6 vias are needed, the maximum trace length is 8 inches.
7. When routing a differential signal pair, 45-degree angles are preferred over 90-degree angles. Signal trace length matching is easier with 45-degree angles and overall signal trace length is reduced.
8. The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.
9. If vias are used to change from one signal layer to another signal layer, it is important to maintain the same 50- Ω impedance reference to the ground plane. Changing reference planes causes signal trace impedance mismatches. If changing reference planes cannot be prevented, bypass capacitors connecting the two reference planes next to the signal trace vias will help reduce the impedance mismatch.
10. If possible, the differential signal pairs should be routed on the top and bottom layers of a circuit board. Signal propagation speeds are faster on external signal layers.

3.2 PCI Express Transmitter Reference Resistor

The REF0_PCIE (L16) and REF1_PCIE (L17) terminals connect to an external resistor to set the drive current for the PCI Express TX driver. The required resistor value is 14,532 Ω with a 1% tolerance.

A 14,532- Ω resistor is a custom value. To eliminate the need for a custom resistor, two series resistors are recommended, a 14,300- Ω 1% resistor and a 232- Ω 1% resistor. Trace lengths must be kept short to minimize noise coupling into the reference resistor terminals.

3.3 PCI-Express Reference Clock Inputs

The XIO2200A requires an external reference clock for the PCI-Express interface. The *PCI Express Base Specification* and *PCI Express Card Electromechanical Specification* provide information concerning the requirements for this reference clock. The XIO2200A is designed to meet all stated specifications when the reference clock input is within all PCI Express operating parameters. This includes both standard clock oscillator sources or spread spectrum clock oscillator sources.

The XIO2200A supports two options for the PCI Express reference clock: a 100-MHz common differential reference clock or a 125-MHz asynchronous single-ended reference clock. Both implementations are described below.

The first option is a system-wide, 100-MHz differential reference clock. A single clock source with multiple differential clock outputs is connected to all PCI Express devices in the system. The differential connection between the clock source and each PCI Express device is point-to-point. This system implementation is referred to as a common clock design.

The XIO2200A is optimized for this type of system clock design. The REFCLK+ (C17) and REFCLK- (C16) terminals provide differential reference clock inputs to the XIO2200A. The circuit board routing rules associated with the 100-MHz differential reference clock are the same as the 2.5-Gb/s TX and RX link routing rules itemized in Section 3.1. The only difference is that the differential reference clock does not require series capacitors. The requirement is a dc connection from the clock driver output to the XIO2200A receiver input. Electrical specifications for these differential inputs are included in the XIO2200A Data Manual.

Terminating the differential clock signal is circuit board design specific. But, the XIO2200A design has no internal 50- Ω -to-ground termination resistors. Both REFCLK inputs, at approximately 20 k Ω to ground, are high-impedance inputs.

The second option is a 125-MHz asynchronous single-ended reference clock. For this case, the devices at each end of the PCI Express link have different clock sources. The XIO2200A has a 125-MHz single-ended reference clock option for asynchronous clocking designs. When the REFCLK_SEL input terminal (A16) is tied to V_{DD_33}, this clocking mode is enabled.

The single-ended reference clock is attached to the REFCLK+ (C17) terminal. The REFCLK+ input, at approximately 20 k Ω , is a high-impedance input. Any clock termination design must account for a high-impedance input. The REFCLK- (C16) terminal is attached to a 0.1- μ F capacitor. The capacitor's second terminal is connected to V_{SSA}. Electrical specifications for this single-ended input are included in the XIO2200A Data Manual.

When using a single-ended reference clock, care must be taken to ensure interoperability from a system jitter standpoint. The *PCI Express Base Specification* does not ensure interoperability when using a differential reference clock commonly used in PC applications along with a single-ended clock in a noncommon clock architecture. System jitter budgets will have to be verified to ensure interoperability. See the *PCI Express Jitter and BER White Paper* from the PCI-SIG.

3.4 PCI Express Reset

The XIO2200A PCI Express Reset ($\overline{\text{PERST}}$) terminal (J17) connects to the upstream PCI Express device's $\overline{\text{PERST}}$ output. The J17 input cell has hysteresis and is operational during both the main power state and V_{AUX} power state. No external components are required.

Please reference the XIO2200A Data Manual and PCI-Express Card Electromechanical Specification to fully understand the $\overline{\text{PERST}}$ electrical requirements and timing requirements associated with power-up and power-down sequencing. In addition, the Data Manual configuration register sections identify all register bits that are reset by $\overline{\text{PERST}}$.

3.5 PCI Express Wake

$\overline{\text{WAKE}}$ is an open-drain output from the XIO2200A that is driven low to re-activate the PCI Express link hierarchy's main power rails and reference clocks. This PCI Express side-band signal is connected to the $\overline{\text{WAKE}}$ input on the upstream PCI Express device. $\overline{\text{WAKE}}$ is operational during both the main power state and V_{AUX} power state.

Since $\overline{\text{WAKE}}$ is an open-drain output, a system-side pullup resistor is required to prevent the signal from floating. The drive capability of this open-drain output is 4 mA. Therefore, the value of the selected pullup resistor must be large enough to assure a logic low signal level at the receiver. A robust system design will select a pullup resistor value that de-rates the output driver's current capability by a minimum of 50%. At 3.3 V with a de-rated drive current equal to 2 mA, the minimum resistor value is 1.65 k Ω . Larger resistor values are recommended to reduce the current drain on the V_{AUX} supply.

4 1394a Port Interface Considerations

The XIO2200A has two 1394a cable ports that can operate at 100, 200, or 400 Mbps. These ports are compliant with the *IEEE Std 1394a-2000*, Amendment 1. This section describes implementation considerations for the XIO2200A's secondary 1394a cable ports.

- The cable not active (CNA) terminal (U09) is an output that reflects the state of the incoming 1394a cable port bias voltage. If no cable bias voltage is detected by the XIO2200A, then this output is asserted high. If terminal U09 is not used, then it must be connected to V_{SS} through a 43-k Ω resistor.
- The cable power status (CPS) terminal (T10) is an input that drives an internal comparator for the purpose of detecting the presence of 1394a cable power. Normally, terminal T10 is connected to the 1394a cable power source through a 400-k Ω resistor. However, if this detection feature is not used, then CPS is connected directly to V_{SSA} .
- PC2 (R09), PC1 (T09), and PC0 (U10) are the power class programming inputs. On the de-assertion of $\overline{\text{PERST}}$, these inputs are captured and loaded into the power class field in the 1394a PHY base configuration registers. Since the binary value associated with the power class field is implementation specific, the system designer must reference the 1394a power class description table in the XIO2200A Data Manual to determine the appropriate PC2:0 input levels. Each terminal is connected to either V_{SS} or V_{DD_33} to specify the appropriate power class binary value. This connection may either be direct or through a weak resistor.
- R0_1394 (T17) and R1_1394 (R16) are provided to set the operating current of the cable driver. A 6.34-k $\Omega \pm 1\%$ resistor is required to meet the IEEE Std 1394a-1995 output voltage limits. One side of the resistor is connected to the T17 terminal and the other side of the resistor to the R16 terminal. Signal traces must be short to minimize noise coupling into the two terminals.
- TPA0P, TPA0N, TPB0P, TPB0N, and TPBIAS0 comprise the five major terminals associated with 1394a PHY port 0. TPA0P (T12) and TPA0N (U12) are the cable A differential signals. TPB0P (T11) and TPB0N (U11) are the cable B differential signals. Terminal U13 (TPBIAS0) provides the 1.86-V nominal bias required for proper driver/receiver operation and for active cable connection signaling to the remote node. The 1394a TPA and TPB differential pairs must follow the same routing guidelines as the PCI Express TX and RX differential pairs except for the differential impedance requirement of 110 Ω . For an unused port, all five terminals can be left as no connects. Please see the attached schematics for external circuit recommendations between the XIO2200A and 1394a cable connector.
- TPA1P, TPA1N, TPB1P, TPB1N, and TPBIAS1 comprise the five major terminals associated with 1394a PHY port 1. TPA1P (T15) and TPA1N (U15) are the cable A differential signals. TPB1P (T14) and TPB1N (U14) are the cable B differential signals. Terminal U16 (TPBIAS1)

provides the 1.86-V nominal bias required for proper driver/receiver operation and for active cable connection signaling to the remote node. The 1394a TPA and TPB differential pairs must follow the same routing guidelines as the PCI Express TX and RX differential pairs except for the differential impedance requirement of 110 Ω . For an unused port, all five terminals can be left as no connects. Please see the attached schematics for external circuit recommendations between the XIO2200A and 1394a cable connector.

- The crystal oscillator terminals are named XI (P17) and XO (P16). An IEEE 1394a recommended 24.576-MHz parallel resonance fundamental mode crystal must be attached to these two terminals. Also, based on the selected crystal, a 16-pF capacitor from each crystal oscillator terminal to V_{SSA} is recommended. Please see Section 7.2 for external crystal circuit recommendations. The XIO2200A supports a second reference clock option. A single-ended 24.576-MHz clock source may be connected to the XI terminal. In this configuration, the XO terminal is left floating. For both clocking options, a stable 1394a reference clock is required prior to the de-assertion of \overline{PERST} .

5 Miscellaneous Terminal Considerations

5.1 GPIO Terminals

There are eight general-purpose input/output (GPIO) terminals in the XIO2200A. All eight GPIO terminals are 3.3-V tolerant. Three of the GPIO terminals are shared with other miscellaneous functions. The remaining five terminals are always general-purpose inputs or outputs.

One Classic PCI configuration register defines the GPIO terminal direction as either an input or an output. A second register either defines the GPIO output state or reports the GPIO input state. The power-up default is GPIO input mode. The power-up default signal level for each GPIO terminal is determined by either an internal active pullup transistor or any externally attached components. Internal active pullup transistors are present on GPIO terminals 0, 1, 2, 3, 4, 6, and 7. When a GPIO terminal is configured as an input, the internal active pullup transistor is enabled. If a GPIO terminal is configured as an output, the internal active pullup transistor is disabled.

The following list of GPIO terminals have special requirements that must be considered when interfacing to the GPIO terminals:

1. GPIO2: This terminal must be a logic one at the de-assertion of \overline{PERST} to enable PCI Express 1.0a compatibility mode. After the de-assertion of \overline{PERST} , this terminal operates as a standard GPIO bit.
2. GPIO4//SCL and GPIO5//SDA: These terminals share the SCL and SDA signals for the external EEPROM. If the GPIO5//SDA terminal is a 1b at the de-assertion of \overline{PERST} , the serial EEPROM interface is enabled. A 0b disables the serial EEPROM interface. If the serial EEPROM interface is enabled, external pullup resistors to V_{DD_33} are required on both terminals per the serial EEPROM specification. Otherwise, these terminals operate as standard GPIO bits.
3. GPIO0, GPIO1, GPIO3, GPIO6, and GPIO7: These terminals always operate as GPIO bits.

5.2 $\overline{\text{GRST}}$ Terminal

$\overline{\text{GRST}}$ is a global reset terminal that is provided for custom reset requirements. When this input is asserted low, all registers, state machines, digital logic, and analog circuits are returned to their power-up default state. This reset is asynchronous to all external reference clock and internal clock domains. The $\overline{\text{GRST}}$ input buffer has hysteresis and an internal active pullup resistor. This input is powered either by main power or by V_{AUX} power. Therefore, global resets may be initiated during either power state.

During an XIO2200A device power-up from the $D3_{\text{cold}}$ power state, there is no requirement to assert this terminal low. An internal power-up reset function performs an equivalent reset to $\overline{\text{GRST}}$. Since this input is powered during V_{AUX} states, it is imperative that any external circuits connected to $\overline{\text{GRST}}$ do not erroneously drive this input low when main power is lost. This results in the reset of sticky control bits and power management state machines.

If the system designer has no need for a custom reset, the $\overline{\text{GRST}}$ terminal can simply be left floating. An internal active pullup resistor will guarantee a non-reset state.

5.3 Reserved Terminals

The XIO2200A has multiple reserved input and output terminals. The recommendation for all output terminals is a no-connect state. Do not connect these output terminals to other signals or external components. Doing so may increase power consumption or cause output driver signal conflicts.

The input terminals must be connected to either V_{DD_33} or V_{SS} . The reserved terminal table in the XIO2200A Data Manual provides connection requirements. The connection may either be a direct short to the recommended supply/ground plane or through a pullup/pulldown resistor. Leakage currents associated with each input must be considered when selecting the resistor option. The minimum leakage current is $\pm 1 \mu\text{A}$ and the maximum is $\pm 100 \mu\text{A}$. Since the leakage current varies from input to input, the safest resistor option is to assume $\pm 100 \mu\text{A}$.

The M15 reserved terminal has special pullup requirements. If a V_{AUX} supply is present within a system, the M15 terminal must be connected to the V_{AUX} supply through a weak pullup resistor. If a V_{AUX} supply is not implemented, the M15 terminal must be connected to the V_{DD_33} supply through a weak pullup resistor.

6 Software Considerations

The basic XIO2200A programming model consists of a 1394a OHCI controller with a two-port PHY that sits behind a PCI Express-to-PCI Translation Bridge. All operating systems that support this system configuration will properly configure the standard functionality within the XIO2200A.

To be more specific, the PCI Express-to-PCI Translation Bridge supports the classic PCI-to-PCI bridge programming model with a type 1 PCI bridge header. Also, if the operating system supports revision 1.1 of the 1394a OHCI controller specification and the IEEE standards 1394a-1995 and 1394a-2000, then the 1394a OHCI controller will be configured properly. All other XIO2200A advanced features default to a disabled state and do not require configuration register initialization for basic operation.

However, to fully utilize advanced features within the XIO2200A, custom device drivers will be required. The best example of an advanced feature is the PCI Express Extended Virtual Channel Configuration Register space. Software for this feature is not presently supported by either today's operating systems or directly by Texas Instruments. Designers should plan to develop custom device drivers if this advanced feature is required in a system.

6.1 Interrupt Configuration

The 1394a OHCI core only generates PCI bus interrupts on $\overline{\text{INTA}}$. When the 1394a OHCI core asserts or de-asserts an interrupt, the bridge core asynchronously detects the state change and generates upstream PCI Express interrupt messages. The PCI Express interface must be link trained and in the L0 link active state for interrupt messages to be sent upstream. The XIO2200A Data Manual illustrates the PCI Express message format for assert and deassert $\overline{\text{INTA}}$ messages.

6.2 Serial EEPROM Interface Configuration

An external serial EEPROM port is provided on the XIO2200A for power-up configuration support. Typically, the system BIOS will initialize the configuration registers associated with the serial EEPROM feature. But for custom systems or PCI-Express add-in cards, this feature is provided to automate basic XIO2200A configuration register initialization.

The registers loaded by the serial EEPROM feature are located in the classic PCI configuration space for the bridge. For the 1394a controller, both classic PCI configuration registers and OHCI memory-mapped configuration registers are loaded.

NOTE: The serial EEPROM also loads TI proprietary registers. The data loaded into these proprietary registers must not be changed from the values specified in the EEPROM register loading map. Otherwise, the operational state of the XIO2200A will be indeterminate.

Terminal T07, named GPIO5 // SDA, provides a basic EEPROM enable or disable option. Upon de-assertion of $\overline{\text{PERST}}$, the logic state of this terminal is checked. If a 1b is detected, then the serial EEPROM interface is enabled. A 0b disables the interface. An external pullup or pulldown resistor is required to generate the appropriate logic state.

Immediately after the detection of a 1b state on terminal T07, the XIO2200A performs the following actions:

1. Bit 3 (SBDETECT) in the serial-bus control and status register is set.
2. Bit 4 (ROMBUSY) in the serial-bus control and status register is set and a serial EEPROM download is initiated to device address 1010000b and word address 00h.
3. The EEPROM data byte located in word address 00h is checked. If bit 7 is asserted, then this indicates an end-of-list indicator and the serial-bus state machine aborts the download. A 00h value indicates a valid PCI Express-to-PCI bus bridge function header. EEPROM word address 00h must only be loaded with 00h, 80h or FFh. Other byte values must not be used because they may cause configuration register download errors and leave the XIO2200A in an indeterminate state.
4. After a valid function header is detected, the EEPROM data byte located in word address 01h is read. This location determines the number of bytes that are downloaded into the bridge configuration registers and must equal 1Eh.

5. The starting EEPROM word address is 02h and the ending address is 1Fh. While downloading the 1Eh data bytes, each byte is loaded into the specified bridge configuration register. The XIO2200A Data Manual includes an EEPROM register loading map.
6. When the bridge function download is finished, the next EEPROM data byte is checked for a valid 1394a OHCI function header. If a 01h value is detected, then the EEPROM download continues. If bit 7 is asserted, then this indicates an end-of-list indicator and the serial-bus state machine aborts the download. EEPROM word address 20h must only be loaded with 01h, 80h or FFh. Other byte values must not be used because they may cause configuration register download errors and leave the XIO2200A in an indeterminate state.
7. The next EEPROM data byte is checked for the length of the 1394a OHCI download. The length information must equal 17h.
8. The starting EEPROM word address is 22h and the ending address is 38h. While downloading the 17h data bytes, each byte is loaded into the specified 1394a OHCI configuration register.
9. The last data byte at word address 39h is checked for a valid end-of-list indicator byte. This data byte must equal 80h.
10. When the serial EEPROM interface state machine is finished, the ROMBUSY status bit is deasserted. If any errors are detected during the download procedure, then bit 0 (ROM_ERR) in the serial-bus control and status register is set. If ROM_ERR status is asserted, then the state of any configuration register targeted by the EEPROM download is unknown.

Additional detail is provided in the XIO2200A Data Manual related to the serial EEPROM function and configuration register download map.

6.3 BIOS Considerations

This section provides a high-level overview of the registers which need to be programmed by the BIOS upon initialization of the XIO2200A. In general, the only registers which must be programmed for proper operation within a Windows operating system are those registers which are EEPROM loadable. Other registers may need to be changed according to system implementation. Microsoft provides the following reference documents concerning architecture and driver support for PCI and PCI Express devices in Windows:

<http://www.microsoft.com/whdc/system/bus/pci/default.mspx>

6.3.1 Bridge Classic PCI Configuration Registers

Primary Bus Number Register (PCI offset 18h) – This register indicates the bus number of the PCI bus segment that the primary PCI Express interface is connected to. The bridge uses this information to determine how to respond to a type 0 configuration transaction. The register default is 00h.

Secondary Bus Number Register (PCI offset 19h) – This register indicates the bus number of the PCI bus segment that the secondary PCI interface is connected to. The bridge uses this information to determine how to respond to a type 1 configuration transaction. The register default is 00h.

Subordinate Bus Number Register (PCI offset 1Ah) – This register indicates the bus number of the highest number PCI bus segment that is downstream of the bridge. For the XIO2200A, the subordinate bus number and secondary bus number registers must be equal. The register default is 00h.

Subsystem Vendor ID and Subsystem ID Registers (PCI offsets 84h and 86h) – These registers are used for subsystem and option card identification purposes. Typically, these registers contain the OEM vendor ID and an OEM identified designator. These fields can be programmed using the EEPROM or BIOS. If using BIOS, then the subsystem access register at offset D0h is written to update the subsystem vendor ID and subsystem ID registers.

GPIO Control and Data Registers (PCI offsets B4h and B6h) – These register determine the direction of the GPIO terminals and set the default state for all GPIO outputs. The initialization state for these registers is system architecture dependent. The control register default is GPIO input mode.

General Control Register (PCI offset D4h) – This register controls various bridge power management and interface operation specific functions that are fully described in the XIO2200A Data Manual. This register can be programmed using the EEPROM or BIOS.

Arbiter Control Register (PCI offset DCh) – This register controls the internal classic PCI Bus arbiter function and can be programmed using the EEPROM or BIOS.

1. EEPROM word address 0Dh bit 7 maps to arbiter control register bit 7 and controls the bus parking option.
2. EEPROM word address 0Dh bit 6 maps to arbiter control register bit 6 and controls the priority tier for the bridge.
3. EEPROM word address 0Dh bits 5–1 map to arbiter control register bits 5–1. These reserve bits must be set to 00000b.
4. EEPROM word address 0Dh bit 0 maps to arbiter control register bit 0 and controls the priority tier for the 1394a OHCI core.

Arbiter Request Mask Registers (PCI offset DDh) – This register controls the internal classic PCI bus arbiter function and can be programmed using the EEPROM or BIOS.

1. EEPROM word address 0Eh bit 7 maps to arbiter mask register bit 7 and controls the arbiter timeout option. A value of 0b is recommended.
2. EEPROM word address 0Eh bit 6 maps to arbiter mask register bit 6 and controls the automatic request mask option.
3. EEPROM word address 0Eh bits 5–1 map to arbiter mask register bits 5–1. These reserve bits must be set to 00000b.
4. EEPROM word address 0Eh bit 0 maps to arbiter mask register bit 0 and controls masking the PCI bus request signal for the 1394a OHCI core.

6.3.2 1394a OHCI Classic PCI Configuration Registers

Subsystem Vendor ID and Subsystem Device ID Registers (PCI offsets 2Ch and 2Eh) – These registers are used for subsystem and option card identification purposes. Typically, these registers contain the OEM vendor ID and an OEM device ID. These fields can be programmed using the EEPROM or BIOS. If using BIOS, then the subsystem access register at offset F8h is written to update the subsystem vendor ID and subsystem device ID registers.

MIN_GNT Register (PCI offset 3Eh) – This register assigns a minimum latency timer value to the OHCI controller and can be programmed using the EEPROM or BIOS. If the EEPROM download option is selected, then only the least significant 4 bits of the MIN_GNT register are updated. EEPROM word address 22h bits 3–0 map to MIN_GNT register bits 3–0. If the BIOS load option is selected, then the MIN_GNT register power-on default equals 02h until the register is updated.

MAX_LAT Register (PCI offset 3Fh) – This register assigns a maximum arbitration priority level to the OHCI controller and can be programmed using the EEPROM or BIOS. If the EEPROM download option is selected, only the least significant 4 bits of the MAX_LAT register are updated. EEPROM word address 22h bits 7–4 map to MAX_LAT register bits 3–0. If the BIOS load option is selected, then the MAX_LAT register power-on default equals 04h until the register is updated.

PHY Control Register (PCI offset ECh) – Bits 7, 3, and 1 may be programmed using the EEPROM or BIOS. The remaining PHY control register bits are not changed. The EEPROM byte at word address 38h initializes this register.

1. EEPROM bit 7 maps to PHY control register bit 7 and, if equal to 1b, enables the CNA output terminal.
2. EEPROM bit 3 maps to PHY control register bit 3. This reserved bit must always be set to 1b.
3. EEPROM bit 1 maps to PHY control register bit 1. This reserved bit must always be cleared to 0b.

Miscellaneous Control Register (PCI offset F0h) – Bits 9–7, 4, and 2–0 within this register may be downloaded from the EEPROM or loaded by the BIOS. Miscellaneous control register bits 9 and 8 are loaded from EEPROM word address 34h bits 1 and 0. While EEPROM word address 33h bits 7, 4, and 2–0 map to miscellaneous control register bits 7, 4, and 2–0.

1. Bits 9–8: MR_ENHANCE controls read command behavior for transactions greater than two data phases.
2. Bit 7: PM_VERSION_CTRL selects power management 1.1 or 1.2 compliance.
3. Bit 4: DIS_TGT_ABT selects either signaling target abort or returning indeterminate data equal to FFh.
4. Bit 2: DISABLE_SCLKGATE is a test mode for enabling or disabling the hardware auto-gating of the internal PHY clock to the PCI bus clock for the 1394a core. This is a test feature only and must be cleared to 0b.
5. Bit 1: DISABLE_PCIGATE is a test mode for enabling or disabling the hardware auto-gating of the internal OHCI clock to the PCI bus clock for the 1394a core. This is a test feature only and must be cleared to 0b.
6. Bit 0: KEEP_PCLK has no effect in the XIO2200A. The recommended default value is 0b.

Link Enhancement Control Register (PCI offset F4h) – Bits 15–12, 7, 2, and 1 within this register may be downloaded from the EEPROM or loaded by the BIOS. Link enhancement control register bits 15–12 are loaded from EEPROM word address 32h bits 7–4. While, EEPROM word address 27h bits 7, 2, and 1 map to link enhancement control register bits 7, 2, and 1.

1. Bit 15: DIS_AT_PIPELINE enables or disables AT pipelining.
2. Bit 14: This reserved bit must always be cleared to 0b.
3. Bits 13–12: ATX_THRESH defines the initial AT FIFO threshold value.
4. Bit 7: ENAB_UNFAIR controls responding to requests with priority arbitration.
5. Bit 2: This reserved bit must always be cleared to 0b.
6. Bit 1: ENAB_ACCEL enables or disables 1394a–2000 standard acceleration enhancements.

6.3.3 1394a OHCI Memory Mapped Configuration Registers

GUID ROM Register (OHCI offset 04h) – The mini-ROM field, bit 7–0, if not equal to 00h, indicates the starting location of the EEPROM mini-ROM data. This field is only loaded by the EEPROM.

GUID High and Low Registers (OHCI offsets 24h and 28h) – These registers represent the 64-bit global unique ID which maps to the third quadlet and chip ID low information in the bus info block. These registers may be downloaded from the EEPROM or loaded by the BIOS.

Host Controller Control Register (OHCI offset 50h) – Bit 23, PROGRAM PHY ENABLE, informs software that the 1394a link and PHY layers are configured for 1394a–2000 enhancements. This bit may be downloaded from the EEPROM or loaded by the BIOS. For the EEPROM download option, word address 27h bit 6 maps to the host controller control register bit 23.

7 Board Design Considerations

7.1 PHY Port Cable Connection

The following figure illustrates the recommended connection of the XIO2200A to a 1394a cable connector.

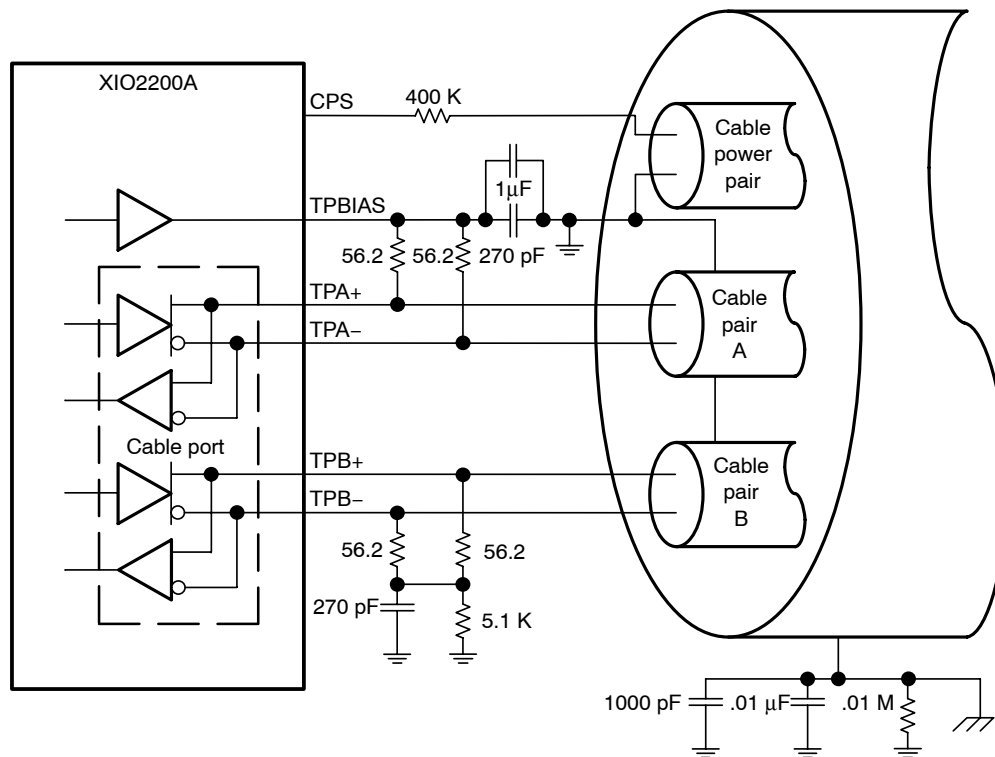


Figure 3. PHY to Port Cable Implementation

NOTE: The IEEE Std 1394–1995 calls for a 250-pF capacitor, which is a nonstandard component value. A 270-pF capacitor is recommended.

7.2 Crystal Selection

The XIO2200A device is designed to use an external 24.576-MHz crystal connected between the XI and XO pins to provide the reference for an internal oscillator circuit. This oscillator in turn drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S400 media data rates.

A variation of less than ± 100 ppm from nominal for the media data rates is required by IEEE Std 1394–1995. Adjacent PHYs may therefore have a difference of up to 200 ppm from each other in their internal clocks, and PHY devices must be able to compensate for this difference over the maximum packet length. Large clock variations may cause resynchronization overflows or underflows, resulting in corrupted packet data.

The following are some typical specifications for crystals used with the PHYs from TI in order to achieve the required frequency accuracy and stability:

- Crystal mode of operation: Fundamental
- Frequency tolerance @ 25°C: Total frequency variation for the complete circuit is ± 100 ppm. A crystal with ± 30 ppm frequency tolerance is recommended for adequate margin.
- Frequency stability (over temperature and age): A crystal with ± 30 ppm frequency stability is recommended for adequate margin.

NOTE: The total frequency variation must be kept below ± 100 ppm from nominal with some allowance for error introduced by board and device variations. Trade-offs between frequency tolerance and stability may be made as long as the total frequency variation is less than ± 100 ppm. For example, the frequency tolerance of the crystal may be specified at 50 ppm and the temperature tolerance may be specified at 30 ppm to give a total of 80 ppm possible variation due to the crystal alone. Crystal aging also contributes to the frequency variation.

- Load capacitance: For parallel resonant mode crystal circuits, the frequency of oscillation is dependent upon the load capacitance specified for the crystal. Total load capacitance (C_L) is a function of not only the discrete load capacitors, but also board layout and circuit. It is recommended that load capacitors with a maximum of $\pm 5\%$ tolerance be used.

For example, load capacitors (C9 and C10 in Figure 3) of 16 pF each were appropriate for the layout of the XIO2200A evaluation module (EVM), which uses a crystal specified for 12-pF loading. The load specified for the crystal includes the load capacitors (C9 and C10), the loading of the PHY pins (C_{PHY}), and the loading of the board itself (C_{BD}). The value of C_{PHY} is typically about 1 pF, and C_{BD} is typically 0.8 pF per centimeter of board etch; a *typical* board can have 3 pF to 6 pF or more. The load capacitors C9 and C10 combine as capacitors in series so that the total load capacitance is:

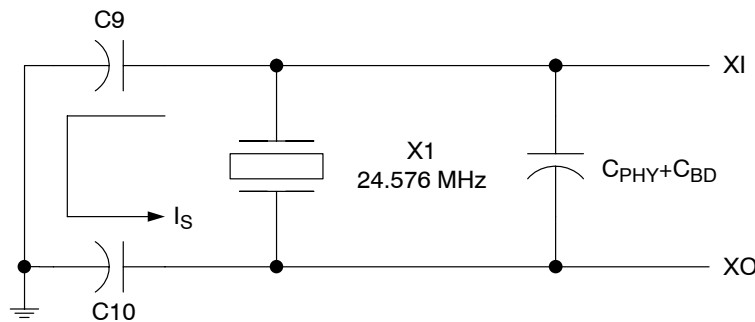


Figure 4. Crystal Load Capacitor Calculation

The layout of the crystal portion of the PHY circuit is important for obtaining the correct frequency, minimizing noise introduced into the PHY phase-lock loop, and minimizing any emissions from the circuit. The crystal and two load capacitors must be considered as a unit during layout. The crystal and the load capacitors must be placed as close as possible to one another while minimizing the loop area created by the combination of the three components. Varying the size of the capacitors may help in this. Minimizing the loop area minimizes the effect of the resonant current (I_s) that flows in this resonant circuit. This layout unit (crystal and load capacitors) must then be placed as close as possible to the PHY XI and XO pins to minimize etch lengths, as shown in Figure 4.

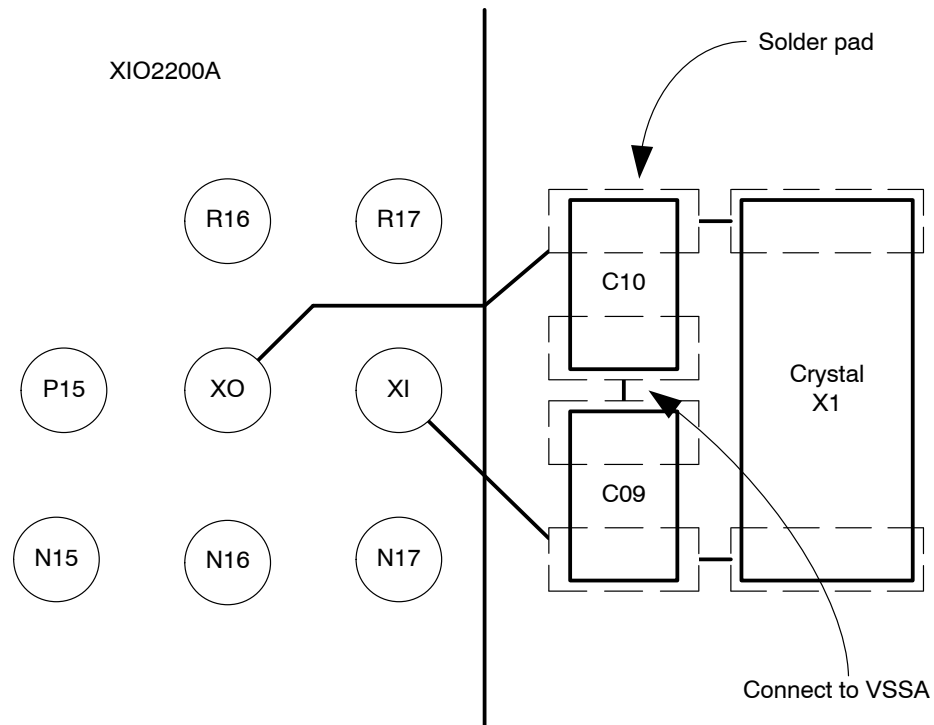


Figure 5. Crystal Layout Diagram (Top View)

For more details on crystal selection, see application report SLLA051 available from the TI website: <http://www.ti.com/sc/1394>.

7.3 EMI Guidelines

For electromagnetic interference (EMI) guidelines and recommendations send a request via e-mail to 1394-EMI@list.ti.com.

8 Power Management Considerations

8.1 D3/L2 Power Management Information

The *PCI Express Card Electromechanical Specification* contains a section that specifies the operation of a PCI Express device when transitioning from D0/L0 to D3/L2 and back to D0/L0 power management states. Since the primary interface on the XIO2200A is PCI Express, the bridge supports this specification for both D3hot and D3cold power management states. System software has the option to place the bridge into the D3/L2 power management state. This process is started in the bridge by setting the PWR_STATE field in the power management control and status register to 11b. By following the procedure outlined in the *PCI Express Card Electromechanical Specification*, the bridge may be transitioned to either the D3hot or D3cold states to reduce system power.

Within the bridge, a $V_{DD_33_AUX}$ power terminal, coupled with internal circuits that combine main power and V_{AUX} power, supplies power to the logic that controls the power management state transitions from D3cold back to D0/L0. Internal sticky logic maintains not only the content of the bridge's sticky register bits, but also information about the operational states of the bridge including state machine context and other internal mechanisms. Within the bridge, \overline{PERST} has no effect on the internal sticky logic.

The 1394a OHCI core has no sticky logic or control register bits. The assertion of $\overline{\text{PERST}}$, resets all logic and control registers within the 1394a core. The 1394a OHCI core within the XIO2200A has the required functionality to assert $\overline{\text{PME}}$ from D3hot, D2, D1 and D0. Since VAUX is not connected to the OHCI core, a power management state transition from D3cold to D0 must be managed by system software.

8.2 Active State Power Management Information

The PCI Express interface on the XIO2200A has the ability to automatically reduce power when there is no queued bus activity. Once this feature is enabled by software, the XIO2200A device automatically transitions into and out of a low-power state. The bridge supports both the L0's and L1 active state power management (ASPM) requirements.

In the PCI Express link capabilities registers, two 3-bit exit latency fields specify the latency time required for the bridge to transition from either the L0's or L1 state back to the L0 state. In the PCI Express device capabilities register, two 3-bit acceptable latency fields specify the maximum latency time that the bridge will tolerate for the attached upstream PCI Express device to transition from either the L0's or L1 state back to the L0 state. The acceptable latency fields are an indirect measure of the bridge's internal buffering.

Power management software uses the reported acceptable latency number to compare against the exit latencies reported by all components physically located on the PCI-Express link between the Bridge and the Root Complex to determine whether ASPM entry can be used with no significant impact to system performance.

8.3 PCI Bus Power Override Information

System software has the ability to manually reduce power on the secondary PCI bus using the bridge's power override feature. During system initialization, XIO2200A configuration registers must be loaded with system specific power information and power override instructions. After this initial setup, the PCI Express set slot power limit message may be used to either enable or disable the power override feature.

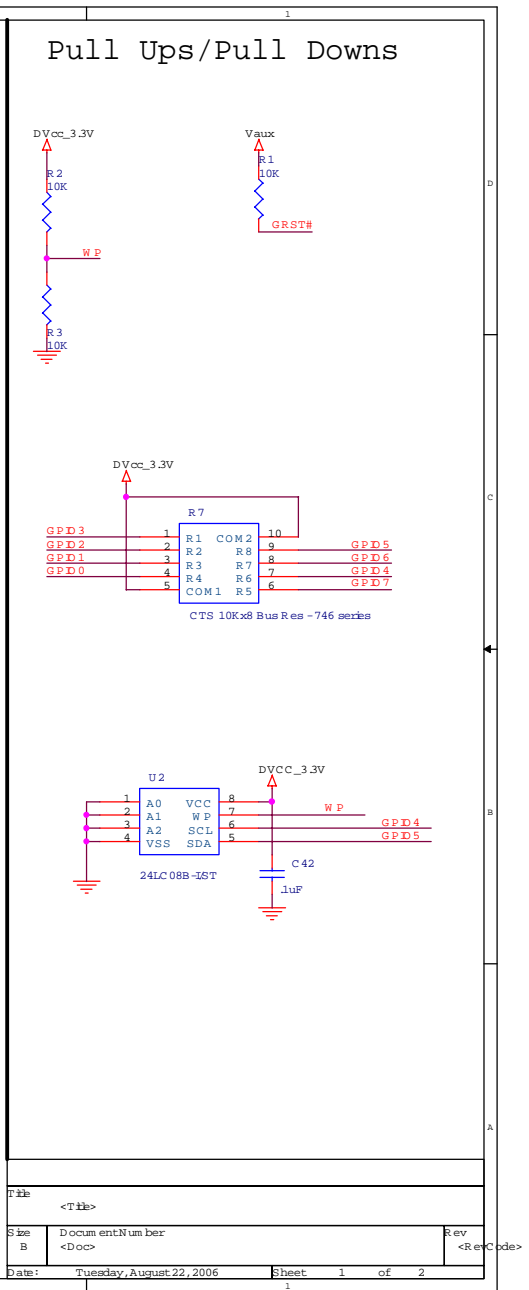
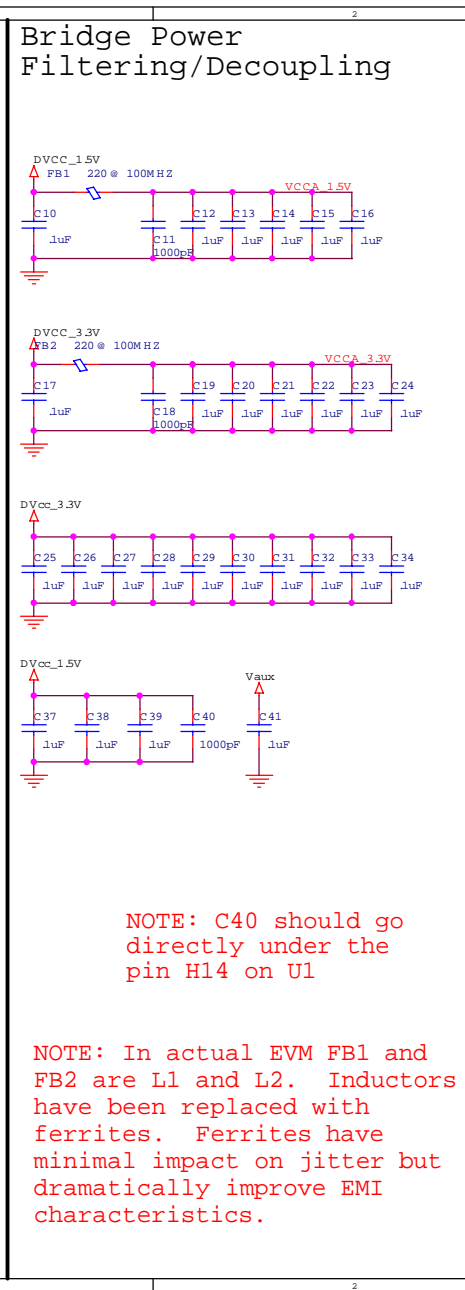
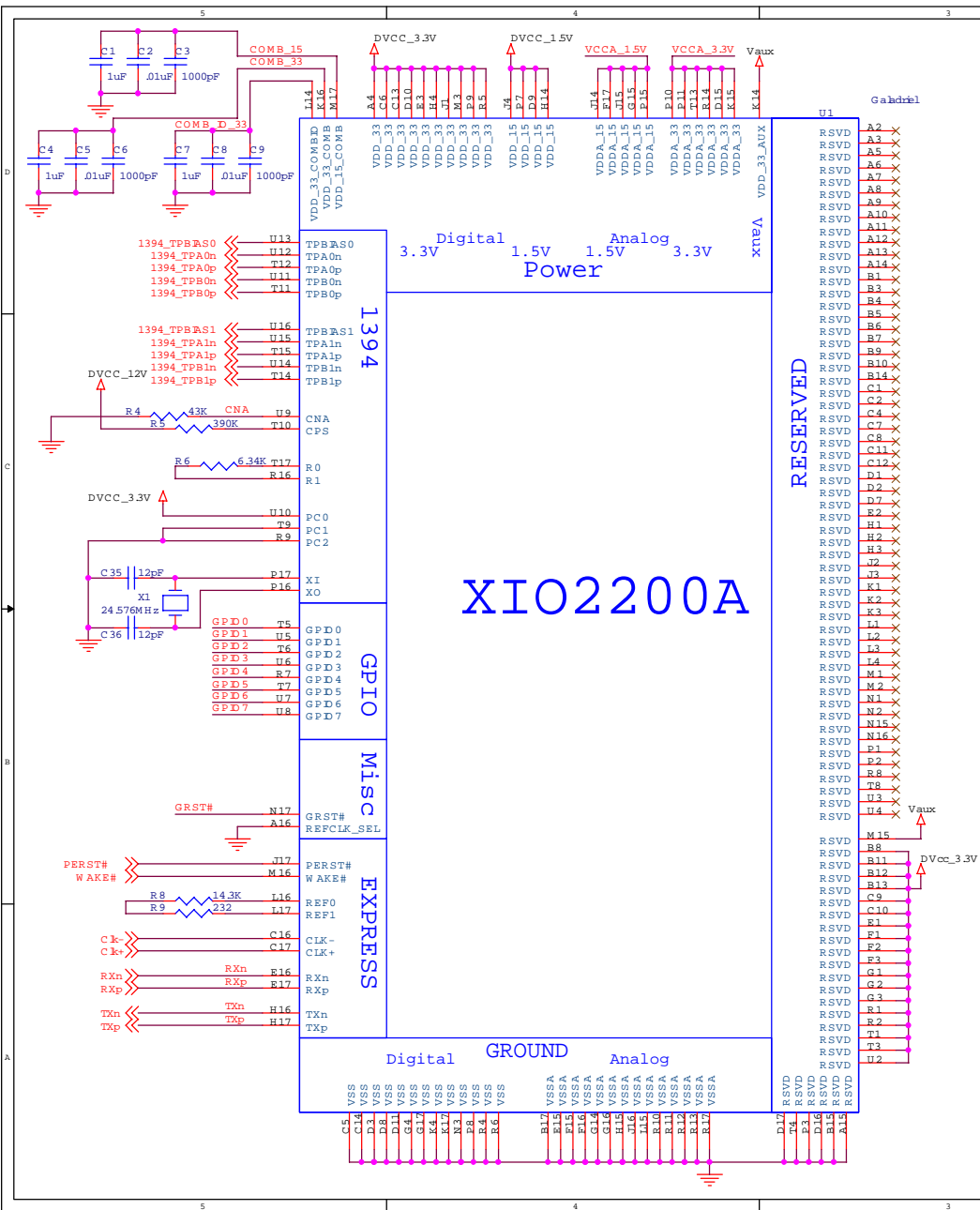
During system initialization the following configuration register fields are loaded. These fields are loaded by either the BIOS or serial EEPROM.

1. The general control register contains `MIN_POWER_SCALE` and `MIN_POWER_VALUE` fields that are loaded with the power information associated with the XIO2200A.
2. The general control register contains a `POWER_OVRD` field that is loaded with the secondary PCI bus power override option.
3. The power override option is initialized associated with responding to all transactions with unsupported request except for configuration transactions and set slot power limit messages.

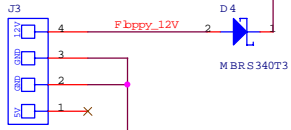
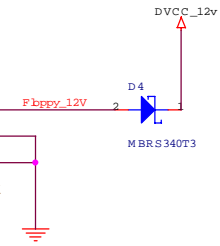
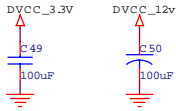
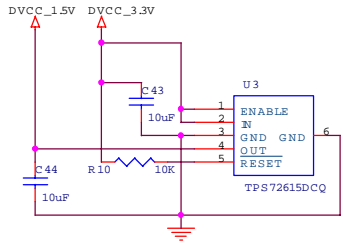
After the previously described initialization procedure, the PCI Express set slot power limit message may be used to either enable or disable the power override feature. If the scale and value power information in the PCI Express message is less than the general control register `SCALE` and `VALUE` fields, then the power override feature is enabled. If the scale and value power information in the PCI Express message is equal to or greater than the `SCALE` and `VALUE` fields, then the power override feature is disabled.

9 Reference Schematics GZZ/ZZZ Package

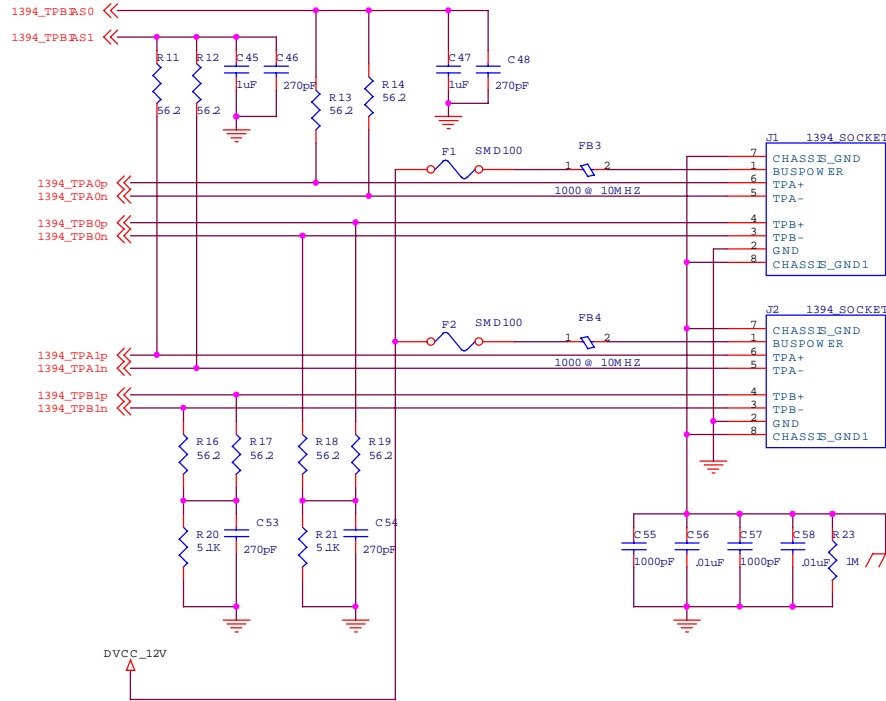
The following schematics show the most basic implementation of the XIO2200A possible. These schematics provide minimum bridge and 1394a OHCI functionality.



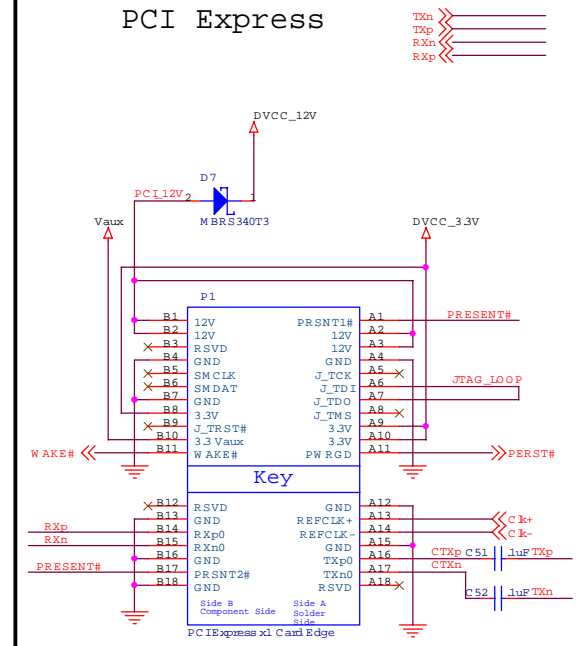
Power



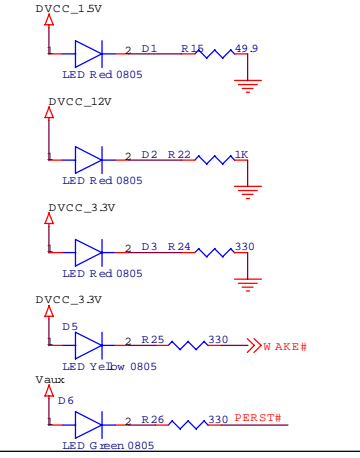
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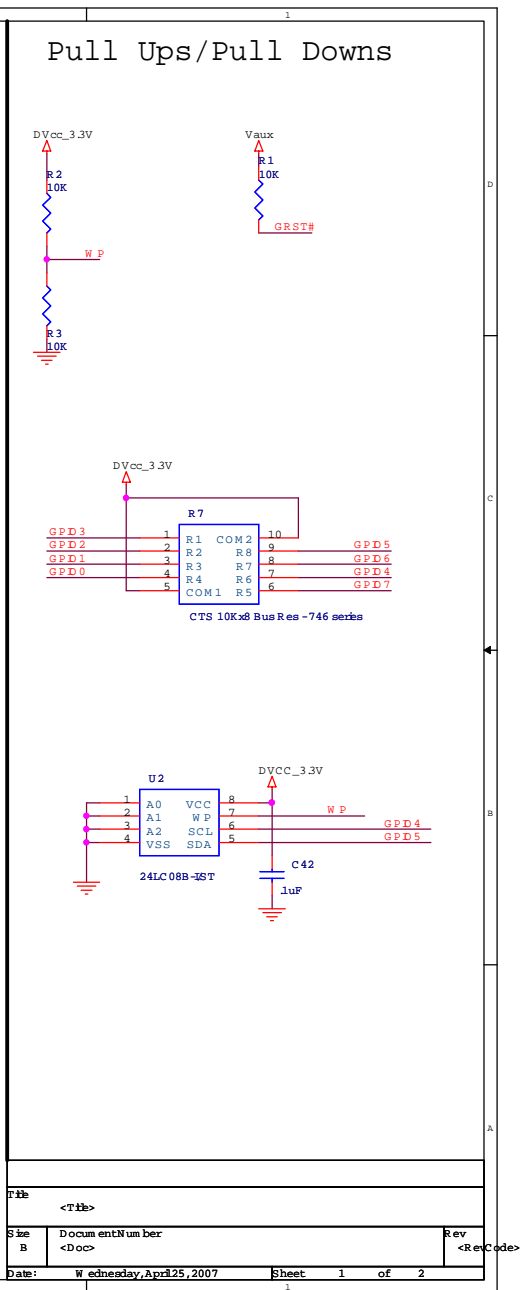
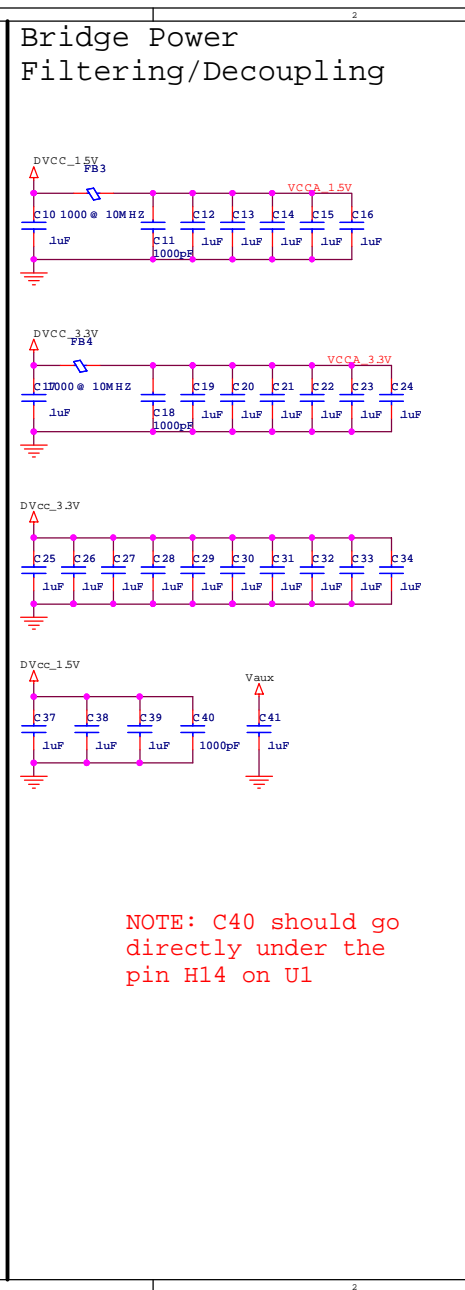
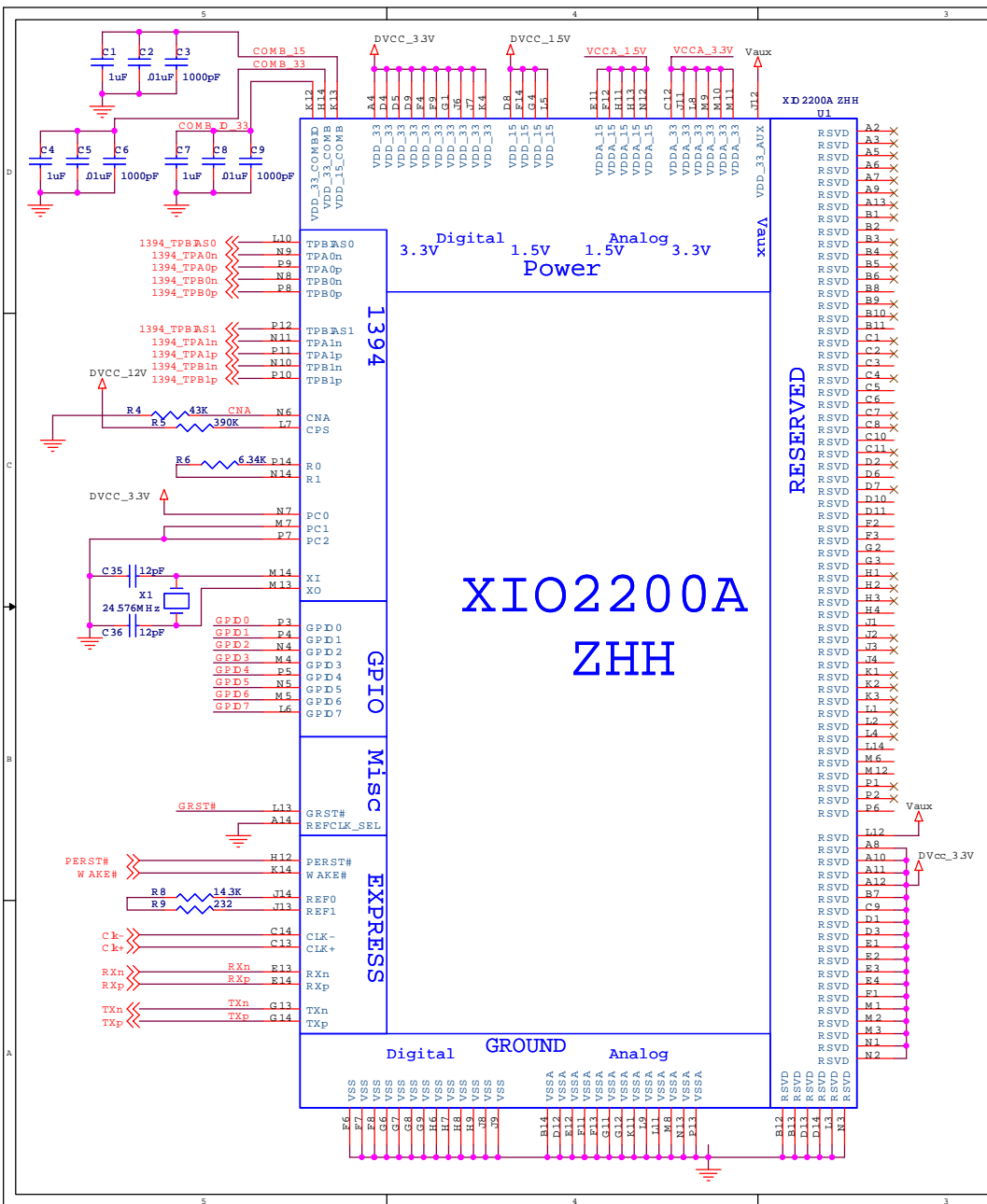
PCI Express



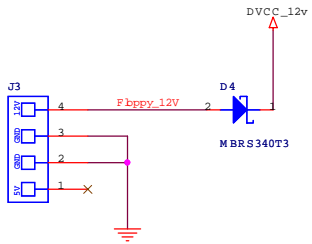
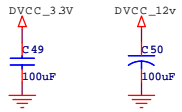
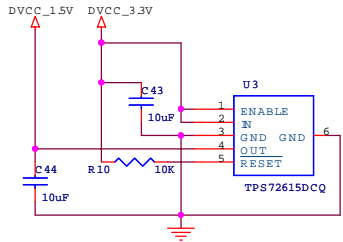
LEDs



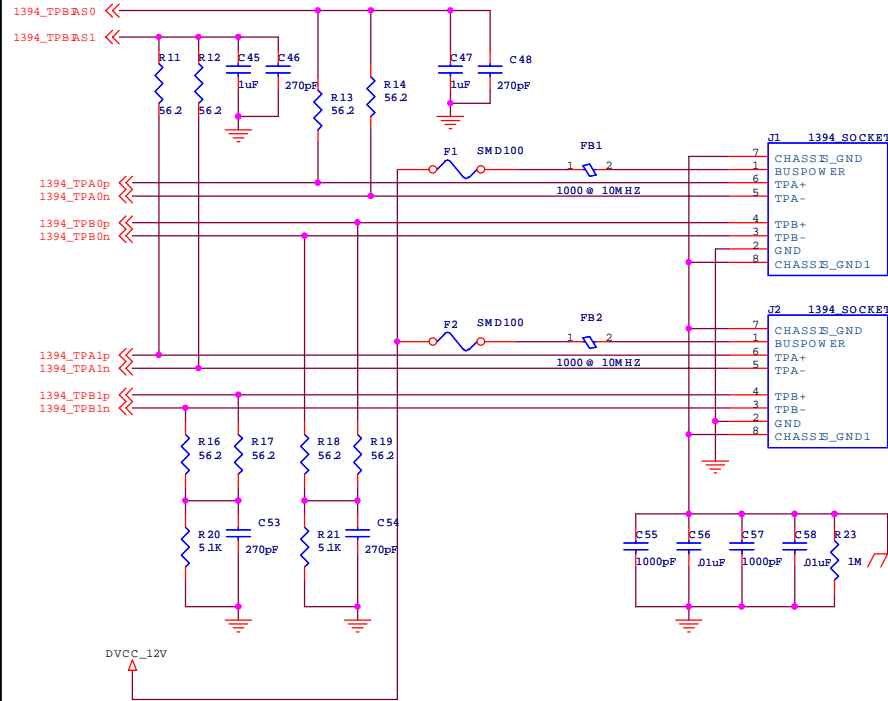
10 Reference Schematics ZHH Package



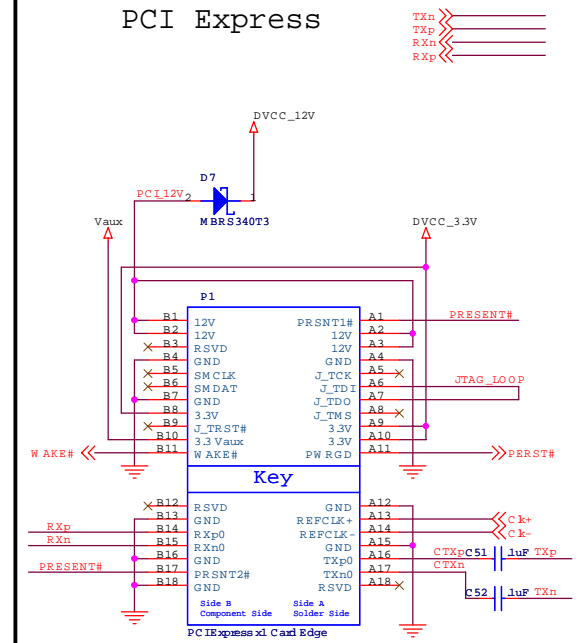
Power



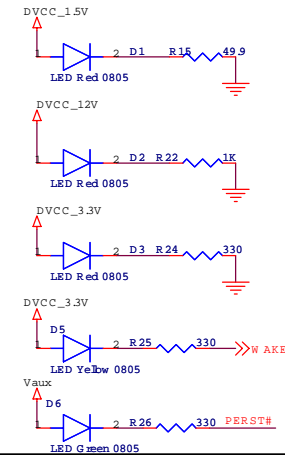
1394



PCI Express



LEDs



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Date:	Friday, March 10, 2006	Sheet 2 of 2
		Rev <Rev Code>

11 Reference Documents

1. PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
2. PCI Express Base Specification, Revision 1.0a
3. PCI Express Card Electromechanical Specification, Revision 1.0a
4. PCI Local Bus Specification, Revision 2.3
5. PCI-to-PCI Bridge Architecture Specification, Revision 1.2
6. PCI Bus Power Management Interface Specification, Revision 1.1 or 1.2
7. 1394 Open Host Controller Interface Specification (Release 1.1)
8. IEEE Standard for a High Performance Serial Bus (IEEE Std 1394–1995)
9. IEEE Standard for a High Performance Serial Bus—Amendment 1 (IEEE Std 1394a–2000)

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