# TLK2711 Serdes EVM Kit Setup and Usage

# **User's Guide**



Literature Number: SGLU001A November 2010-Revised August 2012



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## Introduction

The Texas Instruments TLK2711 serdes evaluation module (EVM) board is used to evaluate the TLK2711 device for point-to-point data transmission applications.

The board enables the designer to connect  $50-\Omega$  parallel buses to both transmitter and receiver connectors. The TLK2711, using high speed PLL technology, serializes, encodes (8b/10b), and transmits data along one differential pair. The receiver part of the device deserializes, decodes, and presents data on the parallel bus. The high-speed (up to 2.5 Gbps) data lines interface to four  $50-\Omega$  controlled-impedance Subminiature Version A (SMA) connectors.

#### 1.1 Introduction

The TLK2711 EVM board can be used to evaluate device parameters while acting as a guide for high-speed board layout. The evaluation board can be used as a daughter board that is plugged into new or existing designs. Because the TLK2711 operates over a wide range of frequencies, designers need to optimize designs for the frequency of interest. Additionally, designers may wish to use buried transmission lines and provide additional noise attenuation and EMI suppression to optimize their end product.

As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to  $50~\Omega$  for both the high-speed differential serial and parallel data connections. In addition, impedance mismatches are reduced by designing the component pad size to be as close as possible to the width of the connecting transmission lines. Vias are minimized and, when necessary, placed as close as possible to the device drivers. Because the board contains both serial and parallel transmission lines, care was taken to control both impedance and trace length mismatch (board skew).

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects is crucial when designing high-speed boards.

Some of the advanced features offered by this board include:

- · Printed-circuit board (PCB) is designed for high-speed signal integrity.
- SMA and parallel fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- Analog and digital power planes can be supplied through separate banana jacks for isolation or can be combined using ferrite bridging networks
- Onboard capacitors provide ac coupling of high-speed signals.

#### 1.2 TLK2711 EVM Kit Contents

☐ TLK2711 EVM board



## TLK2711 EVM Board Configuration

The TLK2711 EVM board gives the developer various options for operation, many of which are jumper selectable. Other options can be either soldered into the EVM or connected through input connectors.

The TX and RX parallel connectors provide a connection for both transmitted and received data. The reference clock is supplied through SMA connector J8, and jumper J5 must be installed between pins 1 and 2. A direct clock connection also can be made to J5 pins 1 and 3. The high-speed serial data is transmitted through J13 and J14 SMA connectors. The received recovered clock (RX\_CLK) is output through J15 header. Received data connects through SMA connectors J17 and J23 on the RX side of the board. Header J7 provides static signals (normally pulled high) to configure the device for different modes of operation.

The power planes are split two ways to provide power for different parts of the board. This minimizes coupling of switching noise between the analog and digital sections of the TLK2711. The VDD and VDDA connectors require 2.5 V and are joined together by a removable ferrite bead L3 that is installed in the default configuration. Thus, only the VDD connection is necessary to energize the TLK2711 device in the default configuration. In all sections of the board, the ground planes are common, and each ground plane is tied together at every component ground connection.

The board is normally delivered in a default configuration that requires external clock and data inputs. The TLK2711 is shipped with jumpers for default operation. Table 2-1 shows the default configuration for sending data.



### Table 2-1. Default Transceiver Board Configuration as Shipped

Designator	Function	Condition
J5	GTX CLK SEL	Jumper installed: J5 provides a method of supplying a input clock to the board.
J7	TESTEN	Jumper installed (Logic 0) Disables the TLK2711 test mode
J7	PRBSEN	Jumper installed (Logic 0) Disables the TLK2711 PRBS internal production test mode
J7	LCKREFN	Jumper not installed (Logical 1) Locks to received clock
J7	ENABLE	Jumper not installed (Logical 1) Enables the device for normal operation
J7	LOOPEN	Jumper installed (Logic 0) Disables the TLK2711 internal loop back mode
J31	PRE-EMPHASIS	Jumper not installed (Logical 1) 20% pre-emphasis enabled. Jumper to enable 5% pre-emphasis.
L3	VDD- bridge -VDDA	Joins VDD and VDDA power planes
C24, C25	TX ac coupling capacitors	These capacitors (normally installed) are provided to ac-couple the transmitted signal.
C22, C23	RX ac coupling capacitors	These capacitors (normally installed) are provided to ac-couple the received signal.

### Table 2-2. Configuration Changes Necessary for DC-Coupling of the High Speed Signals

Designator	Function	Condition or Changes Necessary for DC Coupling
C24, C25	TX ac-coupling capacitors	Install $0-\Omega$ resistors
C22, C23	RX ac-coupling capacitors	Install $0-\Omega$ resistors



### 2.1 Typical Test and Setup Configurations

The following configurations are used to evaluate and test the TLK2711 transceiver. The first configuration is a serial loopback of the high-speed signals shown in Figure 2-1. The serial loopback allows the designer to evaluate most of the functions of both transmitter and receiver sections of the TLK2711 device. To test a system, a parallel bit error rate tester (BERT) generates a predefined parallel bit pattern. The pattern is connected to the transmitter through parallel connectors TD0–TD15. Additionally, two control pins, TKLSB and TKMSB, must configured by the BERT for valid data transmission. For proper data transmission, TKLSB, and TKMSB must be programmed in the pattern to provide the necessary comma character to allow byte alignment to occur. See the TLK2711M data sheet for more information on the use of the TKMSB and TKLSB signals for providing syncronization. The TLK2711 device encodes, serializes, and presents the data on the high-speed serial pair. The serial TX data is then looped back to the receiver side, and the device deserializes, decodes, and presents the data on the receive side RD0-RD15. The data and controll bits (RKLSB and RKMSB) are received by the BERT and compared against the transmitted pattern and monitored for valid data and errors. If any bit errors are received, a bit error rate is evaluated at the parallel receive BERT.

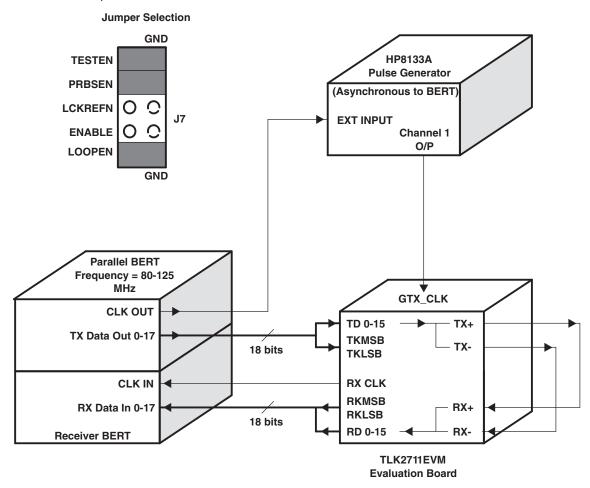


Figure 2-1. TLK2711 Serial Loop-Back Test Configuration



If a parallel BERT is not available, the designer can take advantage of the built-in test mode of the device (see Figure 2-2). If the designer asserts the PRBSEN pin high, this results in a pseudo random bit pattern to be transmitted. This pin also puts the receiver in a mode to detect a valid PRBS pattern. A valid pattern is indicated by the PRBSPASS(RKLSB) pin indicating high. This test validates only the high-speed serial portion of the device and system interconnects. The PRBS pattern is 2<sup>7</sup>-1 and is compatible with most serial BERT test equipment. This function allows the operator to isolate and test the transmitter and receiver independently. A typical configuration is shown in Figure 2-3. The dashed lines represent optional connections that can be made monitoring eye patterns and measuring jitter. This same test can be performed without the external serial connections with LOOPEN jumper removed. Removing LOOPEN, causes the transmitted data to be internally looped to the receiver with the transmitter disabled.

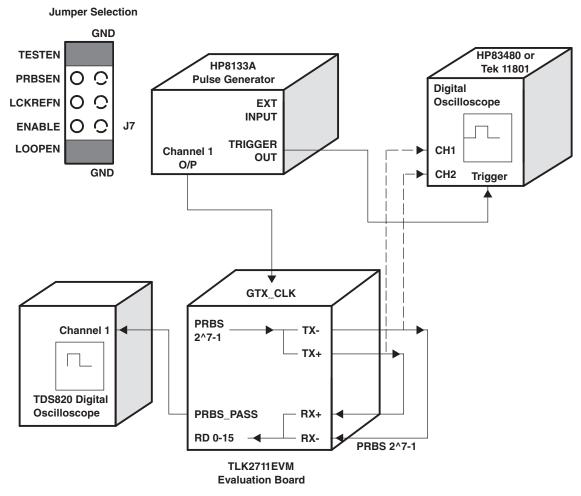


Figure 2-2. TLK2711 Serial Loop-Back Test Configuration



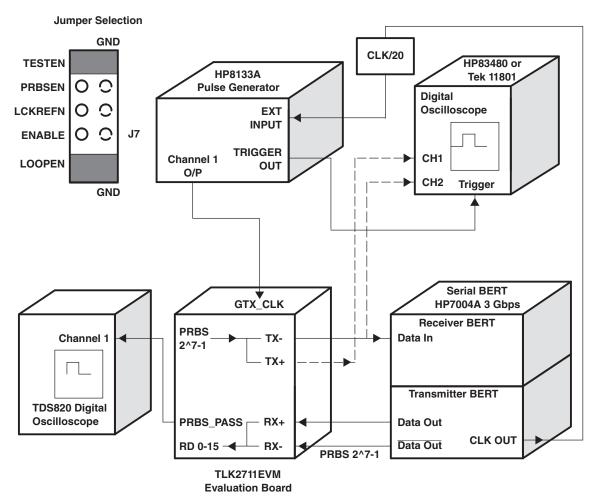


Figure 2-3. TLK2711 Serial PRBS BERT Test Configuration



A board-to-board communication link is a practical method of evaluating the TLK2711 in a system-like environment as shown in Figure 2-4. A Parallel BERT or a logic analyzer can be used to provide and monitor signals to and from the transceiver pairs. The BERT would need to configure the TKLSB and TKMSB signals for data transmission before any data is sent. On the receive side the RKMSB and RKLSB can monitor the device for errors. Both GTX\_CLK sources must have the same frequency within 200 PPM for asynchronous operation. Synchronous operation can be achieved by using either the BERT or a synchronized pulse generator to supply both boards with GTX\_CLK inputs.



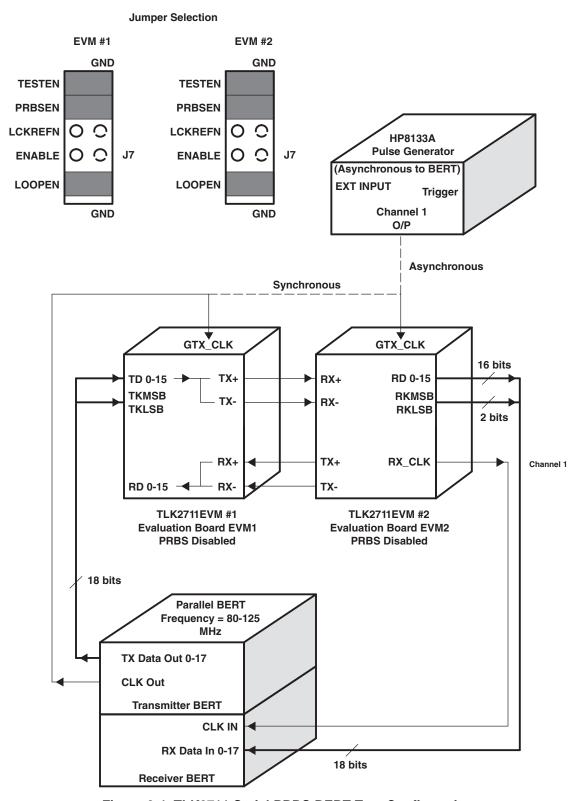


Figure 2-4. TLK2711 Serial PRBS BERT Test Configuration

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- · Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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