EVM User's Guide: TAC5412Q15B5EVM-K TAC5411Q15B5EVM-K TAA5412Q15B5EVM-K

TAx5x1xQ15B5EVM-K Evaluation Module

Description

The TAx5x1xQ15B5EVM-K evaluation module (EVM) allows the user to test the capabilities of Texas Instruments' two-channel high-performance ADC TAA5412-Q1, a two-channel TAC5412-Q1 or TAC5411-Q1, a single-channel high-performance codec. Other variants listed are also supported where users can replace the U1 unit with the device of interest. The evaluation module is paired with the AC-MB, a flexible motherboard that provides power, control, and digital audio data to the evaluation module.

Get Started

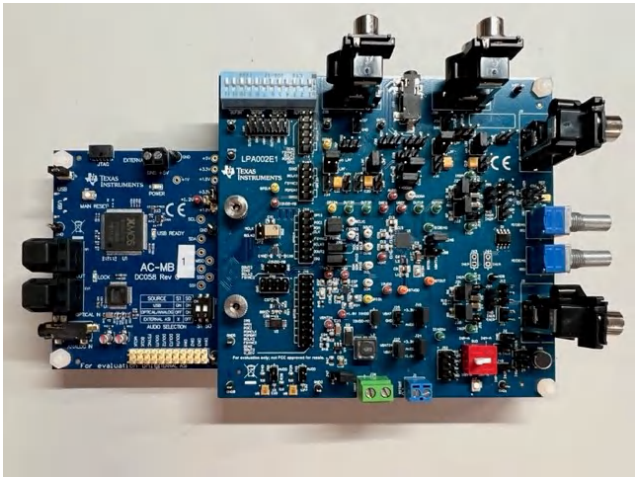
1. Order the EVM from the TAx5x12 product folder.
2. Download the latest TAx5x12 data sheet.
3. Request access and download the PPC3 GUI from the TAx5x12 product folder.

Features

- Complete evaluation kit for the TAC5x12-Q1 (two-channel codec), TAC5x11-Q1 (single-channel codec), or TAA5412-Q1 (two-channel ADC).
- High-performance mono/stereo codec dynamic range: 120 dB DAC and 110 dB ADC or standard performance 106 dB DAC and 102 dB ADC
- On-board microphones provided for voice recording testing
- Direct access to digital audio signals and control interface for simple end-system integration
- USB connection to PC provides power, control, and streaming audio data for easy evaluation
- On-board diagnostic scenarios for analog audio input

Applications

- Emergency E-Call
- Telematics control unit
- Automotive active noise cancellation
- Automotive head units



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1 Evaluation Module Overview

1.1 Introduction

The TAx5x1XQ15B5EVM is an evaluation module (EVM) designed to demonstrate the performance and functionality of the TAx5x1x-Q1 family of devices. This family includes the devices shown in Table 1-1 with differences in performance and function noted. This user's guide describes the functionality of the TAC5412Q15B5EVM-K, TAC5411Q15B5EVM, or TAA5412Q15B5EVM-K evaluation kit.

Table 1-1. TAx5x1x-Q1 Family

Device	ADC DR (dB)	DAC DR (dB)	Feature
TAC5412-Q1	110	120	Stereo codec
TAC5411-Q1	110	120	Mono codec
TAC5312-Q1	102	106	Stereo codec
TAC5311-Q1	102	106	Mono codec
TAA5412-Q1	110	NA	Stereo ADC

1.2 Kit Contents

- TAC5412-Q1, TAC5411-Q1 or TAA5412-Q1 device
- TAx5x1XQ15B5 EVM/daughterboard
- AC-MB controller/motherboard

1.3 Specification

The TAx5x1XQ15B5EVM-K evaluation module (EVM) paired with the AC-MB, a flexible motherboard that provides power, control, and digital audio data to the evaluation module, allows the user to record and playback audio signals. The configuration for the TAx5x1x-Q1 family of devices is done through the PurePath™ Console 3 (PPC3) GUI.

1.4 Device Information

- TAC5412-Q1, a low-power, high-performance, stereo audio codec with integrated programmable boost, mic bias, and diagnostics.
- TAC5411-Q1, a low-power, high-performance, mono audio codec with integrated programmable boost, mic bias, and diagnostics.
- TAC5312-Q1, a low-power stereo audio codec with integrated programmable boost, mic bias, and diagnostics.
- TAC5311-Q1, a low-power mono audio codec with integrated programmable boost, mic bias, and diagnostics.
- TAA5412-Q1, a low-power, high-performance, stereo audio ADC with integrated programmable boost, mic bias, and diagnostics.

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2 Hardware

2.1 System Overview

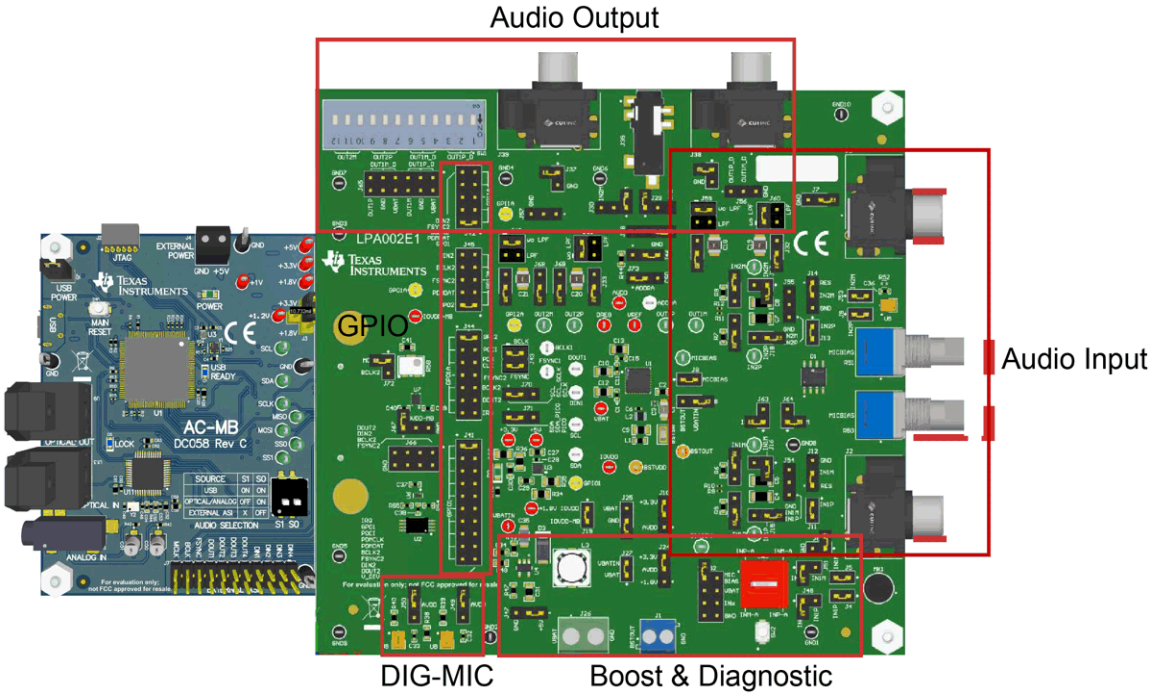

Figure 2-1. System Overview

2.2 Hardware Overview

The evaluation kit consists of the TAx5x1XQ15B5EVM daughterboard and the AC-MB controller board. The controller board provides the evaluation module power, control, and digital audio signals. The daughterboard contains the TAx5x12-Q1 device and the input and output connections. Some components are not populated in the EVM depending on the selected device.

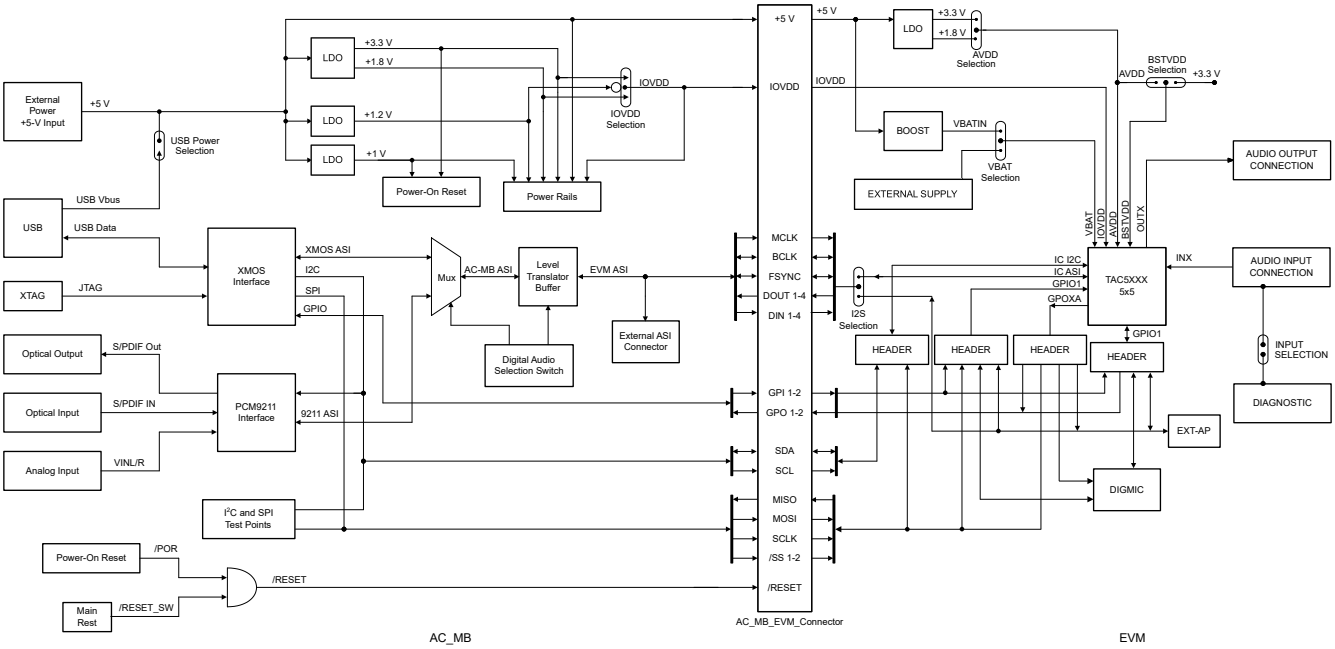

Figure 2-2. TAx5x1xQ1 EVM Block Diagram

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2.2.1 AC-MB Settings

2.2.1.1 Audio Serial Interface Settings

The AC-MB provides the digital audio signals to the evaluation module (EVM) from the universal serial bus (USB), optical jack, stereo audio jack, and external audio serial interface (ASI) header. Figure 2-3 shows a block diagram of the ASI routing on the AC-MB.

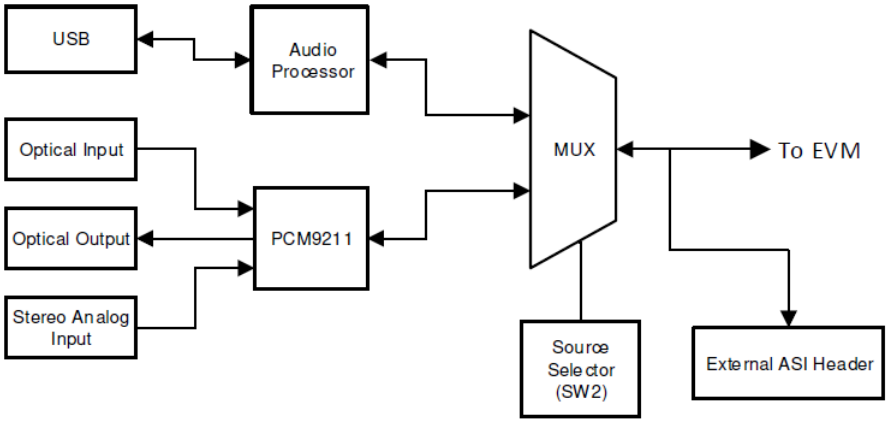

Figure 2-3. AC-MB Audio Interface Block Diagram

The SW2 switch on the AC-MB selects the audio serial bus that interfaces with the PCM6xx0EVM. Next to the SW2 switch, the AC-MB has a quick reference table to identify the audio serial interface source options and switch settings. The AC-MB acts as the controller for the audio serial interface. The AC-MB has three different modes of operation: USB, optical or analog, or external ASI.

The serial interface clocks and data are provided from the USB interface. The USB audio class driver on the operating system determines the sampling rate and format. The default settings for the USB audio interface are 32-bit frame size, 48-kHz sampling rate, BCLK and FSYNC ratio of 256, and the format is time-division multiplexing (TDM).

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2.2.1.1.1 USB Mode

The OS detects the AC-MB as an audio device named TI USB Audio UAC2.0. Figure 2-4 shows the AC-MB audio setting for the USB mode of operation.

Figure 2-4. AC-MB USB Audio Setting

2.2.1.1.2 Optical or Auxiliary Analog Audio Input Mode

Serial interface signals are provided from the PCM9211 digital transceiver, which is capable of sending digital data to the EVM from an analog input or optical input. Meanwhile, the data from the EVM can be streamed through the optical output.

Figure 2-5 shows the AC-MB audio setting for the optical and analog mode of operation.

Figure 2-5. AC-MB Optical or Auxiliary Analog Audio Input Setting

The optical output of the AC-MB streams the data captured on the EVM with the format determined by the input source used. When there is an optical input connected, the LOCK LED must be ON. The PCM9211 streams the audio serial interface clocks with the format determined by the optical input frame. The digital data from the optical input is streamed to the EVM. If the optical input is not connected, the PCM9211 captures the input signal provided through the analog input, and streams the signal to the EVM. This feature can be useful when a digital input digital-to-analog converter (DAC) is connected to the AC-MB, providing an analog input for quick evaluation. In auxiliary analog audio mode, the audio serial interface format is fixed to a 24-bit, 48-kHz, I2S mode.

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2.2.1.1.3 External Audio Interface Mode

In this mode, the audio serial interface clocks for the evaluation board are provided through connector J7 from an external source. This architecture allows an external system to communicate with the evaluation board, such as a different host processor or test equipment (Audio Precision™). The clocks generated from the USB interface and PCM9211 are isolated with this setting. Figure 2-6 shows the AC-MB audio setting for the external mode of operation.

Figure 2-6. AC-MB External Audio Interface Setting

Figure 2-7 shows how to connect the external audio interface. Odd-numbered pins are signal-carrying; even-numbered pins are connected to ground.

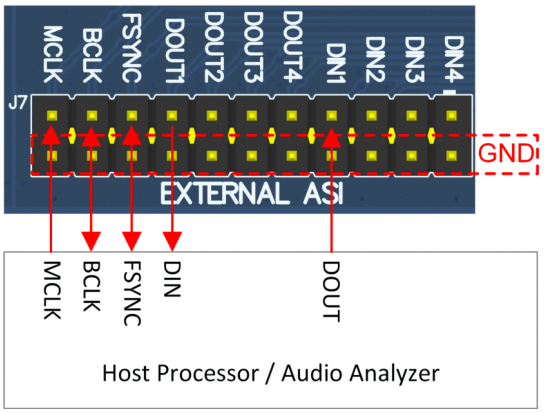

Figure 2-7. AC-MB Connection with External Audio Serial Interface

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2.2.1.2 AC-MB Power Supply

A single 5-V power supply powers the complete evaluation module system. However, the motherboard has different low-dropout regulators (LDOs) integrated that provide the required power supply to the different blocks of the board. Figure 2-8 shows a block diagram depicting the power structure of the AC-MB.

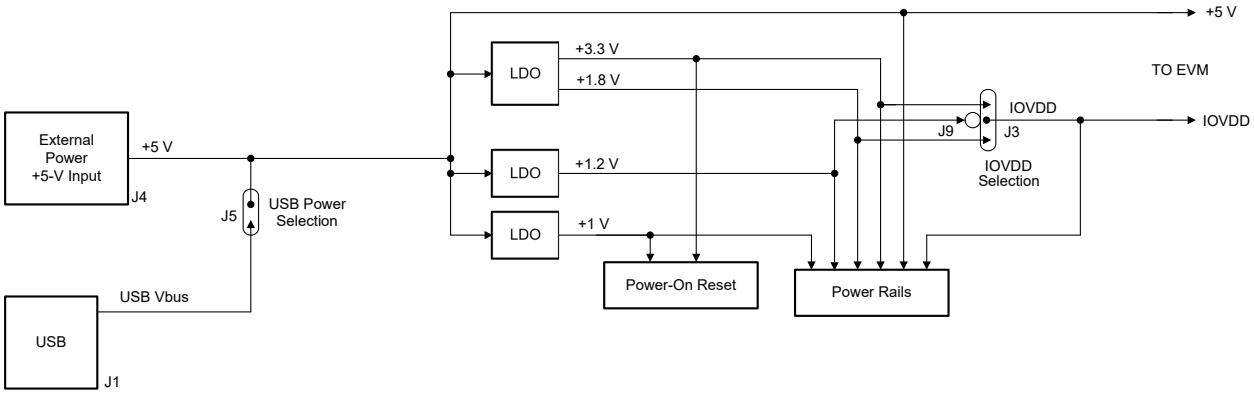

Figure 2-8. Power-Supply Distribution of the AC-MB

The AC-MB can be powered from the host computer using the USB 5-V power supply (VBUS) by shorting header J5, USB POWER. Additionally, the AC-MB can be powered from an external power supply connected to terminal J4, EXTERNAL POWER. Header J5 must be open for external supply operation. The IOVDD voltage for the digital signals provided to the EVM is generated on the motherboard from the main power supply (USB or external).

The voltage levels available are 1.2 V, 1.8 V, and 3.3 V and can be selected via the J9 and J3 IOVDD header. For 1.2-V operation, short pin 1 of header J9 and pin 2 of header J3; for 1.8-V operation, short pins 2 and 3 of header J3; for 3.3-V operation, short pins 1 and 2 of header J3. The green POWER LED (D3) turns ON when the motherboard is fully powered and the power supplies from the onboard LDOs are correct. The USB READY LED indicates a successful USB communication between the AC-MB and the host computer.

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2.2.2 TAx5x1xQ1EVM-K Hardware Settings

2.2.2.1 TAx5x1x-Q1 EVM Input Hardware Settings

The TAx5x1x-Q1 evaluation module has several input configuration options. The EVM allows the user to evaluate the device across multiple operation modes. The different operation modes are highlighted in this section.

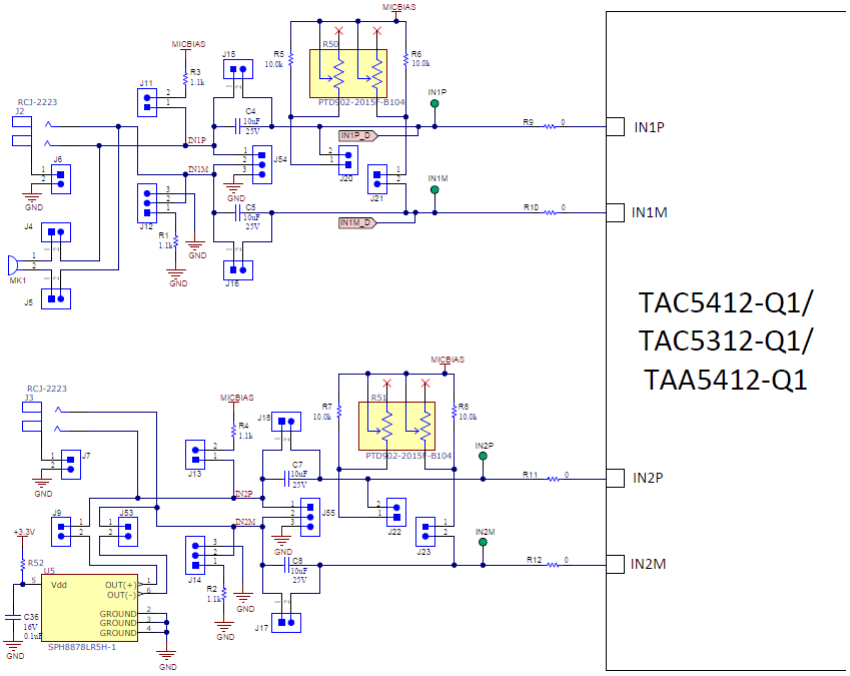

Figure 2-9. TAx5x12-Q1 EVM Input Architecture for Channel 1 and 2

The IN1 and IN2 input architecture allows these two channels to be quickly configured to support any of the supported operation modes. The INxP and INxM pins of the TAx5x1x-Q1 can optionally connect to onboard microphones for quick evaluation of a microphone in AC or DC-coupled modes. Jumper configuration details can be found in Table 2-1.

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For TAC5x11-Q1 evaluation module, the DIN1P and DIN1M can be connected to IN1P and IN1M respectively through jumper J63 and J64 as shown in Figure 2-10. Only IN1 Input Terminal is applicable in this evaluation module from the configuration table below.

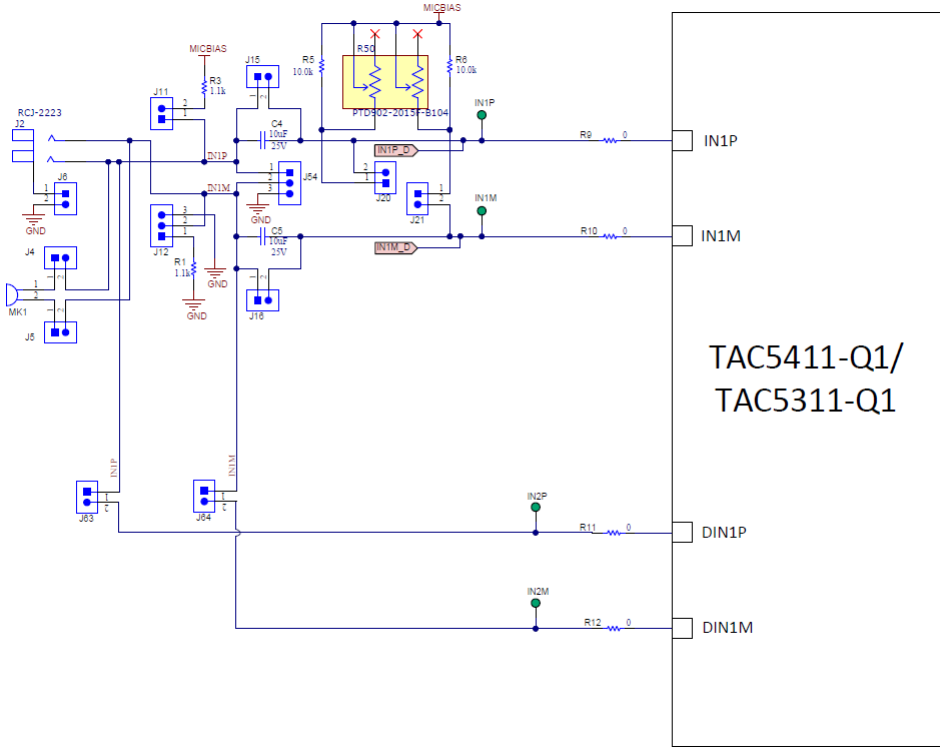


Figure 2-10. TAC5x11-Q1 EVM Input Architecture for Channel 1 and DIN1P/M

Table 2-1. Input Jumper Configuration

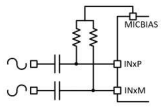
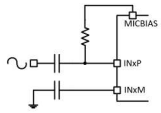
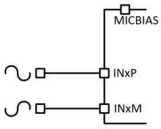
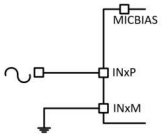
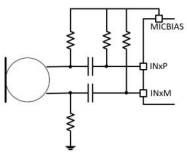
Input Terminal	Input Mode	Installed Jumpers	Uninstalled Jumpers	Input Swing	Topology	Register Setting
IN1	LINE-IN Differential, AC-coupled	J8, J20, J21	J4, J5, J6, J11, J12, J15, J16	10 V_{RMS}		B0_P0_R80, B0_P1_R115
	LINE-IN Single-ended, AC-coupled	J6, J8, J12 (2-3), J20, J21	J4, J5, J11, J15, J16	5 V_{RMS}		B0_P0_R80, B0_P1_R115
	LINE-IN Differential, DC-coupled	J15, J16	J4, J5, J6, J11, J12, J20, J21, J8 (DUT MICBIAS is not used)	10 V_{RMS}		B0_P0_R80
	LINE-IN Single-ended, DC-coupled	J6, J12 (2-3), J15, J16	J4, J5, J11, J20, J21, J8 (DUT MICBIAS is not used)	5 V_{RMS}		B0_P0_R80
	On-board Electret Condenser Microphone (ECM) Differential, AC-coupled	J4, J5, J8, J11, J12 (1-2), J20, J21	J6, J15, J16	Refer to Microphone data sheet		B0_P0_R80, B0_P1_R115

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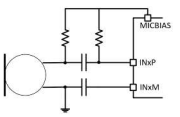
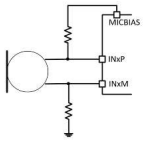
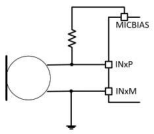
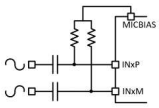
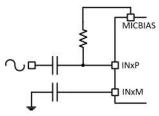
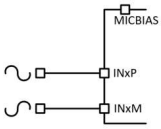
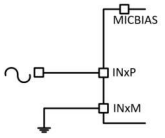
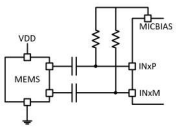
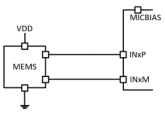
Table 2-1. Input Jumper Configuration (continued)

Input Terminal	Input Mode	Installed Jumpers	Uninstalled Jumpers	Input Swing	Topology	Register Setting
	On-board Electret Condenser Microphone (ECM) Single-ended, AC-coupled	J4, J5, J8, J11, J12 (2-3), J20	J6, J15, J16, J21	Refer to Microphone data sheet		B0_P0_R80, B0_P1_R115
	On-board Electret Condenser Microphone (ECM) Differential, DC-coupled	J4, J5, J8, J11, J12 (1-2), J15, J16	J6, J20, J21	Refer to Microphone data sheet		B0_P0_R80, B0_P1_R115
	On-board Electret Condenser Microphone (ECM) Single-ended, DC-coupled	J4, J5, J8, J11, J12 (2-3), J15, J16	J6, J20, J21	Refer to Microphone data sheet		B0_P0_R80, B0_P1_R115
IN2	LINE-IN Differential, AC-coupled	J8, J22, J23	J7, J9, J13, J14, J17, J18, J53	10 V_{RMS}		B0_P0_R85, B0_P1_R115
	LINE-IN Single-ended, AC-coupled	J7, J8, J14 (2-3), J22, J23	J9, J13, J17, J18, J53	5 V_{RMS}		B0_P0_R85, B0_P1_R115
	LINE-IN Differential, DC-coupled	J17, J18	J7, J9, J13, J14, J22, J23, J53, J8 (DUT MICBIAS is not used)	10 V_{RMS}		B0_P0_R85
	LINE-IN Single-ended, DC-coupled	J7, J14 (2-3), J17, J18	J9, J13, J22, J23, J53, J8 (DUT MICBIAS is not used)	5 V_{RMS}		B0_P0_R85
	On-board Analog MEMS microphone, AC-coupled	J8, J9, J22, J23, J53	J7, J13, J14, J17, J18	Refer to the Microphone data sheet.		B0_P0_R85, B0_P1_R115
	On-board Analog MEMS microphone, DC-coupled	J9, J17, J18, J53	J7, J13, J14, J22, J23, J8 (DUT MICBIAS is not used)	Refer to the Microphone data sheet.		B0_P0_R85, B0_P1_R115

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2.2.2.1.1 Line Inputs

For the line input configuration shown in Figure 2-9, the TAx5x1x-Q1 captures the audio signal provided through RCA terminals J2 (IN1), J3 (IN2), header J54, or J55. The RCA white connector is connected to the INxP. The RCA red connector is connected to the INxM. Depending on the differential or single-ended configuration, populate the J6 or J7 jumper as described in Table 2-1 accordingly. The input accepted in this mode is a differential 10-VRMS full-scale audio signal. If a single-ended source is used, the 5-VRMS signal is supported. The gang potentiometer R50 and R51 provide the input bias resistors for this AC-coupled input mode depending on the desired input swing and impedance.

Using the TAx5x1x-Q1 AC-Coupled external resistor calculator, enter the maximum input level and the desired MICBIAS voltage to determine the resistance required to achieve full input swing as shown in Figure 2-11.

From the calculator example below, the maximum resistance allowed is 2399.4 Ohm, and the closest standard resistance is 2375 Ohm. Based on this standard value resistance, the effective impedance looking into the device is about 2184 Ohm. This effective input impedance forms a high pass filter with the external capacitor. The Vcm is the common voltage for the respective MICBIAS and Input Swing. One can adjust the R50 and R51 potentiometer to get the common mode voltage (Vcm). By default, the EVM Vcm is set to 7.3 V.

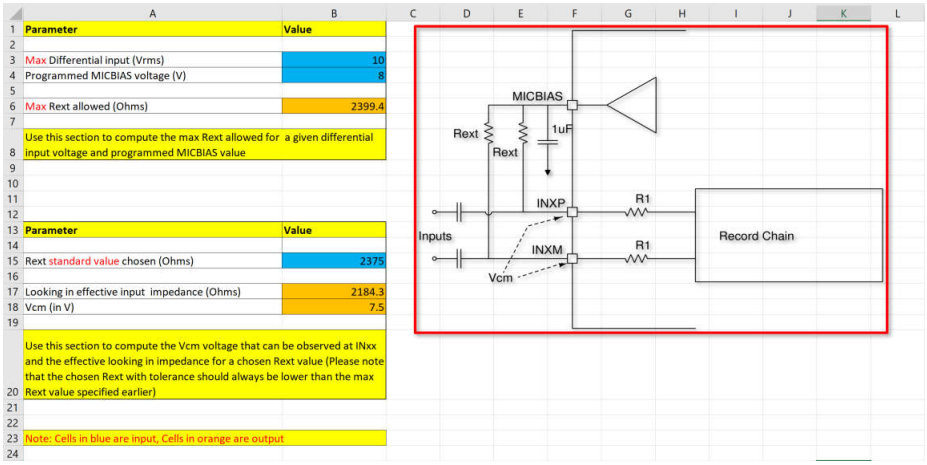

Figure 2-11. AC-Coupled External Resistor Calculator

2.2.2.1.2 On-Board Microphone Input

For the on-board microphone input configuration shown in Figure 2-9, the TAx5x1x-Q1 records the audio captured from MK1 (ECM) or U5 (Analog MEMS) microphones. For U5, the audio port is located at the bottom of the board. Electret Microphone (MK1) is connected to IN1P/M, and MICBIAS is used to power the onboard microphone, so header J8 must be installed. The MEMS microphone (U5) can be configured as a single-ended or differential input and connected to IN2P/M. There must not be any connections to J2 or J3 while the onboard microphone is used to preserve the performance of the microphone. Gain adjustment can be needed in the device depending on the microphone sensitivity.

2.2.2.2 TAx5x1x-Q1 EVM Output Hardware Settings

The TAx5x1x-Q1 evaluation module has several output configuration options and offers flexibility to allow the user to evaluate the device with different load conditions and configurations. The different configurations are highlighted in this section.

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2.2.2.2.1 TAx5x1x-Q1 Analog Audio Output

The EVM analog audio output port provides options for AC/DC-coupled and filter or filter-less paths for easy evaluation. By default, the filter components are not populated.

Switch SW1 allows users to select respective loads for each output pair for 16 Ω, 604 Ω, or 10 kΩ if needed. These resistors are for quick evaluation and can be bypassed for actual load. SW1 and the output RCA connectors are located on the top left-hand side, shown in Figure 2-13.

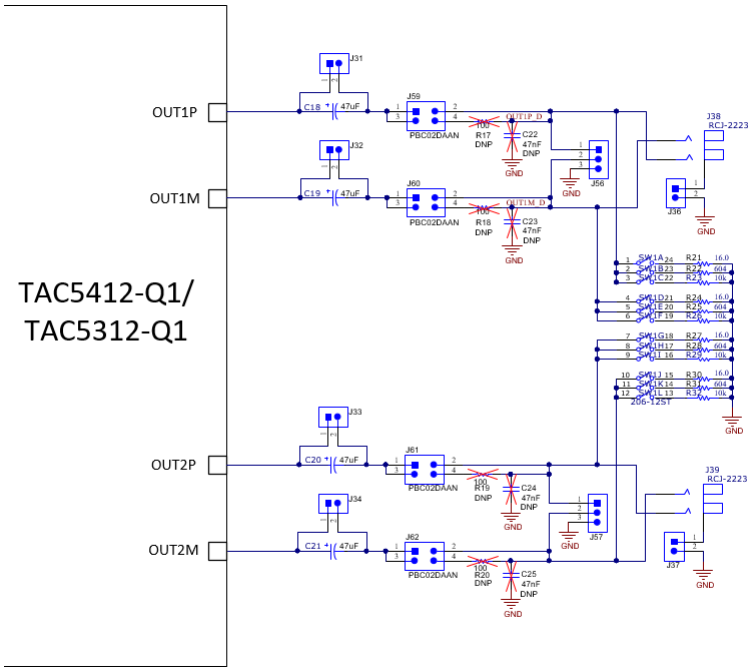

Figure 2-12. TAC5x12-Q1 EVM Output Architecture for Channel 1 and 2

OUT1 and OUT2 audio output pins have connection options with external load or the on-board load selections. A pair of RCA connectors, white from OUTP and red from OUTM, allow users to connect to external devices as differential or single-ended. Jumper header J36 or J37 must be populated if single-ended is desired or removed for differential configuration.

Table 2-2. SW1 Pin

SW1 pin	Load Configuration	Resistor Rating	Output Module Register Setting
1, 4, 7, 10	16 Ω	0.5 W	B0_P0_R101
2, 5, 8, 11	604 Ω	0.125 W	B0_P0_R101
3, 6, 9, 12	10 kΩ	0.4 W	B0_P0_R101

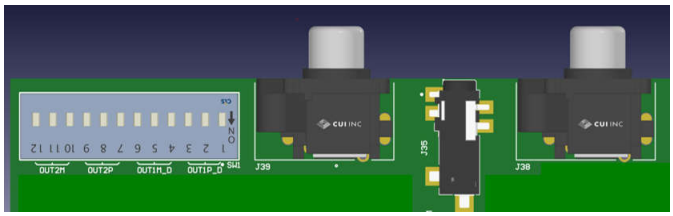

Figure 2-13. TAC5x12-Q1 Analog Output Connections

For TAC5411-Q1 or TAC5311-Q1, OUT2 components are not populated.

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2.2.3 Diagnostics Hardware Setup

The diagnostics test circuitry, as shown in Figure 2-14, is not connected to any channel by default. Populate J48 and J51 jumpers to enable IN1P and IN1M diagnostic test. Only one channel can be tested at a time with the on-board diagnostics test circuitry. A fault is introduced by pressing SW2.

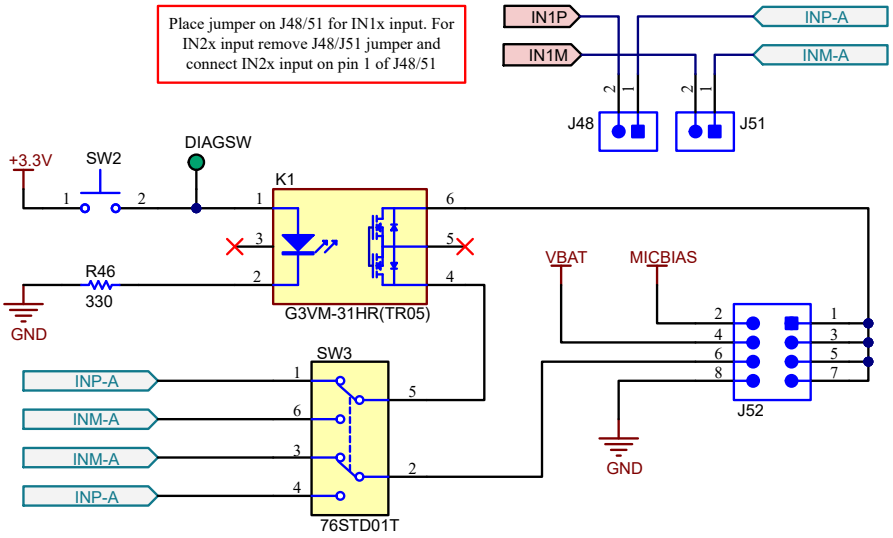

Figure 2-14. TAx5x1x-Q1 EVM Diagnostic Circuitry

The diagnostic test selection is done by populating one jumper at any time on the J52 header either for input to MICBIAS short, input to VBAT short, input to input short, or input to ground short. Once the connection is established, press SW2 to initiate the test; the fault detection can then be verified through the device register. The bidirectional arrow indicates moving the switch to the left for the IN1P test and to the right for the IN1M test.

TI's recommended settings for this diagnostics test circuit are discussed in this section. The following figures below are based on a newer EVM revision, which has IN1P and IN1M connected by default through J48 and J51.

2.2.3.1 Short to MICBIAS Setup

Figure 2-15 shows a short to the MICBIAS test. If using a single-ended input for the test channel, only connect INxP.

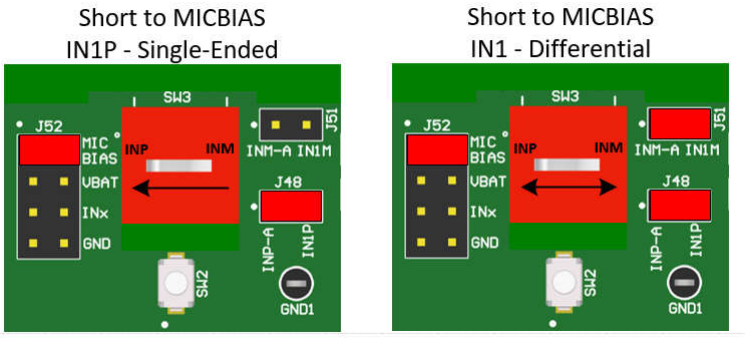

Figure 2-15. Short to MICBIAS Diagnostic Test Setup

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2.2.3.2 Short to VBAT Setup

A short to VBAT test requires an external voltage source connected to VBAT through J26 or onboard VBAT through J27. If onboard VBAT is used, populate the J47 pin 1-2 jumper to enable the U4 switch regulator.

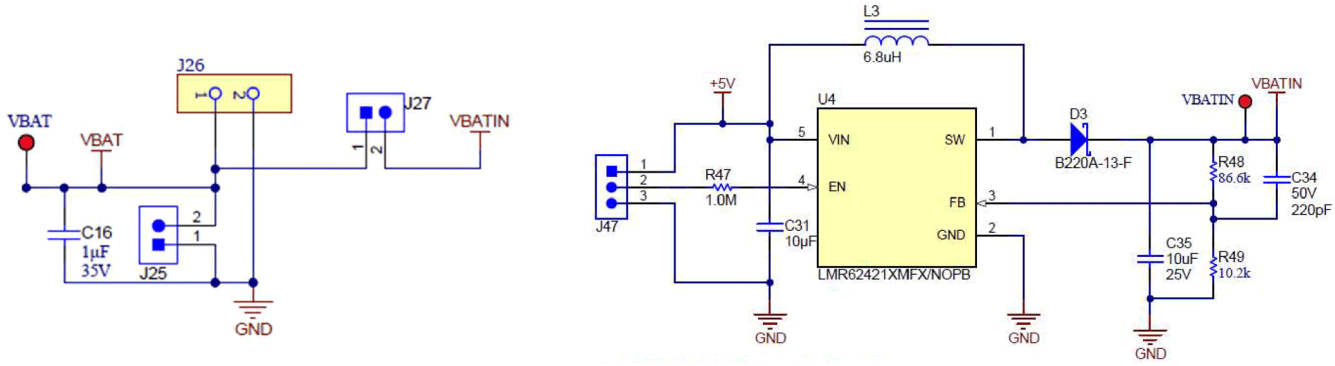

Figure 2-16. VBAT Connection

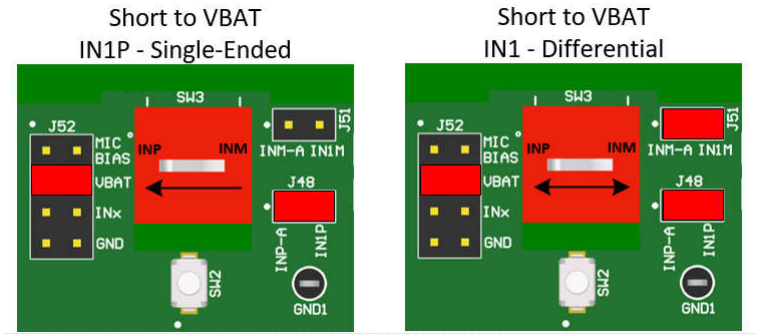

Figure 2-17. Short to VBAT Diagnostic Test Setup

2.2.3.3 Shorted Input Pins Setup

Shorted input diagnostic testing can be performed for differential inputs only.

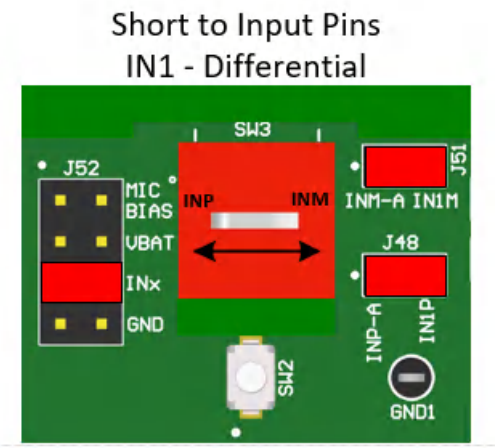

Figure 2-18. Short to Input Diagnostic Test Setup

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2.2.3.4 Short to GND Setup

Figure 2-19 shows the short to ground testing for the inputs.

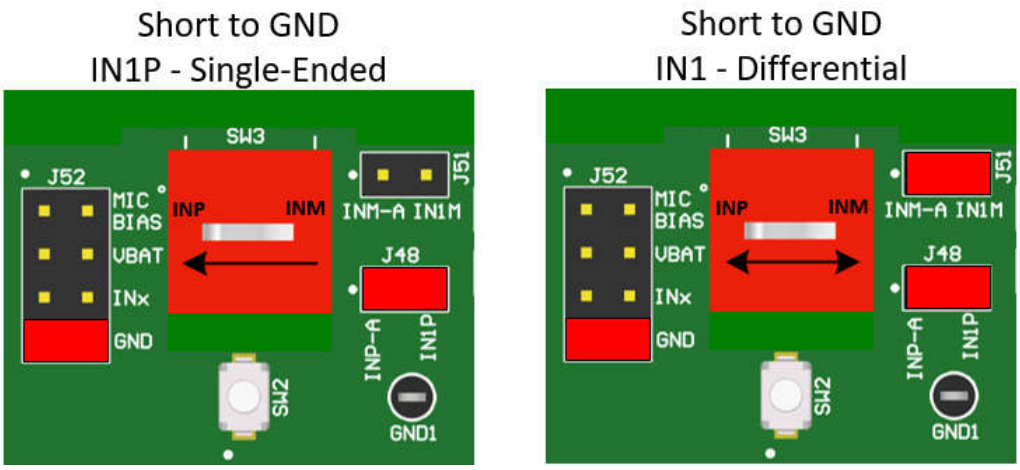

Figure 2-19. Short to Ground Diagnostic Test Setup

2.2.4 GPIO1 Hardware Configurations

GPIO1 has many configuration options through the J41 header, but only one setting is allowed at a time. GPIO1 can be configured for general-purpose input-output, a Serial Peripheral Interface (SPI), data for POCI (Peripheral Output Controller Input), a PDM/Digital MIC, or a second audio serial interface (ASI2). GPIO1 can be configured as the Digital Microphone Clock or Data for digital microphone applications. For the Audio Serial Interface, GPIO1 can be configured as either the WCLK, BCLK, DIN, or DOUT in the controller or peripheral mode, as shown in Figure 2-20.

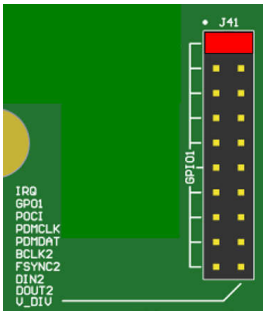

Figure 2-20. GPIO1 Configuration

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2.2.5 GPO1A Hardware Configurations

GPO1A has many output configuration options through the J44 header, but only one setting is allowed at a time. GPO1A can be configured for general-purpose output, a Serial Peripheral Interface (SPI), data for POCI, a PDM/Digital MIC clock, or a second audio serial interface (ASI2). For Audio Serial Interface, GPO1A can be configured as either the WCLK, BCLK, or DOUT in controller mode, as shown in Figure 2-21.

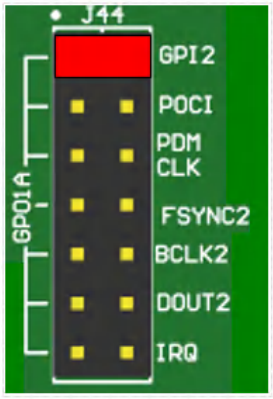

Figure 2-21. GPO1A Configuration

2.2.6 GPI1A Hardware Configurations

GPI1A supports input configuration options through the J42 header, but only one setting is allowed at a time. GPI1A can be configured for general-purpose input, PDM/Digital MIC data, or a second audio serial interface (ASI2). In Audio Serial Interface, GPI1A can be configured as either the WCLK, BCLK, or DIN in peripheral mode, as shown in Figure 2-22.

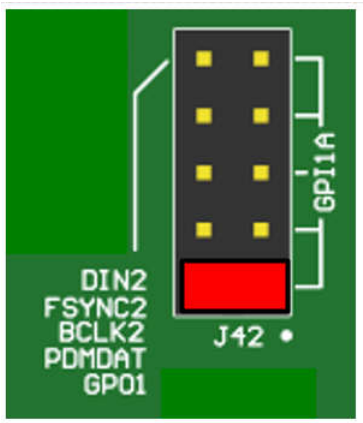

Figure 2-22. GPI1A Configuration

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2.2.7 GPI2A Hardware Configurations

GPI2A supports input configuration options through the J45 header, but only one setting is allowed at a time. GPI2A can be configured for general-purpose input, PDM/Digital MIC data, or a second audio serial interface (ASI2). In Audio Serial Interface, GPI2A can be configured as either the WCLK, BCLK, or DIN in peripheral mode, as shown in Figure 2-23.

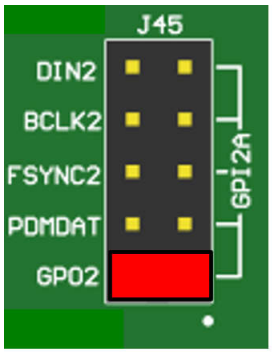

Figure 2-23. GPI2A Configuration

2.2.8 I2C Address Hardware Configurations

Configuring the address of the TAx5x1x-Q1 device on the EVM is typically not required for evaluation use; however, configuring the address is supported by placing jumper on header J46 to either low (ground) or high (pull-up to AVDD). Header J73 needs to be populated on pin 1-2.

ADDRA Level	Device Address (7-bit Addressing)	Device Address (8-bit Addressing)
AVDD	0x51	0xA2
GND	0x50	0xA0

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2.2.9 Audio Serial Interface Hardware Configurations

The TAx5x1x-Q1 EVM supports the Secondary Audio Serial Interface (SASI). By default, the EVM is configured for Primary Audio Serial Interface (PASI) from the AC-MB with jumpers populated on header J43 pin 1-2 and pin 3-4. If secondary ASI is desired from AC-MB, remove jumpers on header J43, place jumper on header J67 pin 1-2, and configure TAx5x1x-Q1 device for a secondary audio interface.

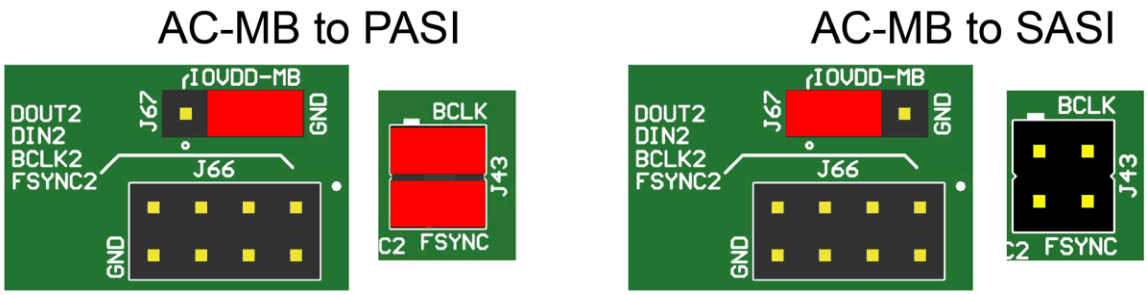

Figure 2-24. AC_MB Audio Serial Interface Connection

The external audio interface can also be used for SASI with header J66. To make parameter measurements on SASI with the external audio instrument, remove the jumpers on header J43 and place jumper on header J67 pin 2-3, as shown in Figure 2-25.

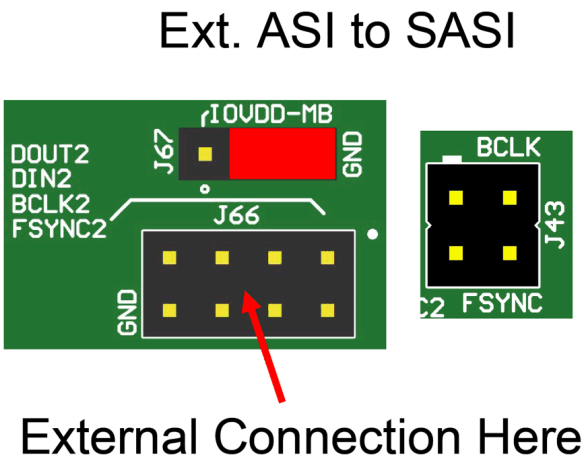

Figure 2-25. External Audio Serial Interface Connection

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3 Software

3.1 Software Description

Texas Instruments PurePath™ console 3 (PPC3) graphical user interface is a program that serves as a platform for many TI audio products. PPC3 is designed to simplify the evaluation, configuration, and debugging process associated with the development of audio products.

3.2 PurePath™ Console 3 Installation

The TAx5x1x-Q1 EVM GUI is an application that installs into the PPC3 framework. PPC3 must be installed before downloading the TAx5x1x-Q1 EVM GUI. Click here to download the PPC3 and request access. If the PPC3 is already installed, proceed to TAx5x1x-Q1 EVM GUI. Figure 3-1 shows the setup directory for the PPC3 installation.

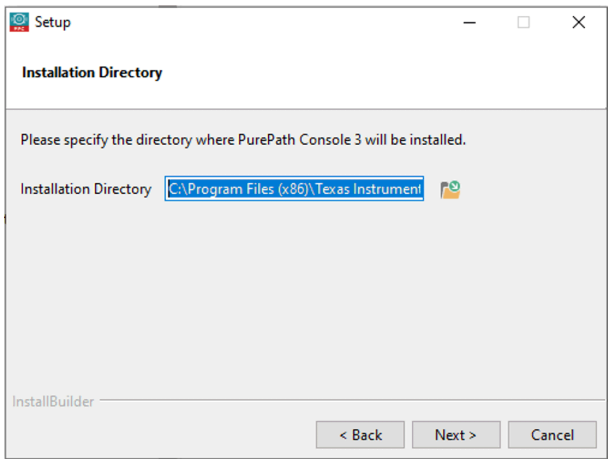

Figure 3-1. PurePath™ Console 3 Installation

Open the PPC3 installer and follow the instructions in the setup wizard.

3.2.1 USB Audio Setup

Note

When using the USB audio interface, the Texas Instruments USB audio device control panel, shown in Figure 3-2, opens with the input setting configured for eight channels, 32 bits. For USB audio, 32-bit mode must also be used on the EVM.

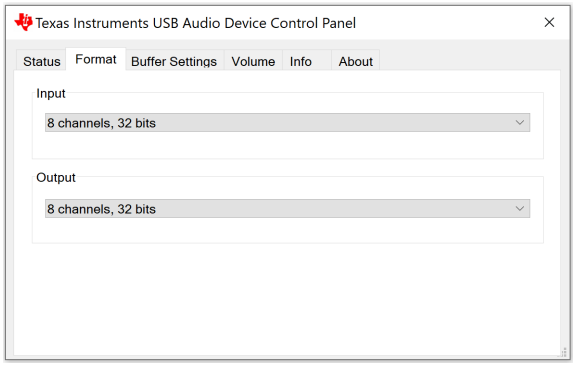

Figure 3-2. Texas Instruments USB Audio Device Control Panel

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3.3 TAx5x1x-Q1 EVM GUI

Open the PPC3 application in the directory chosen for the GUI installation in Section 3.2. Figure 3-3 shows the resulting app center window. Click on the TAC5x1x-Q1 app tile.

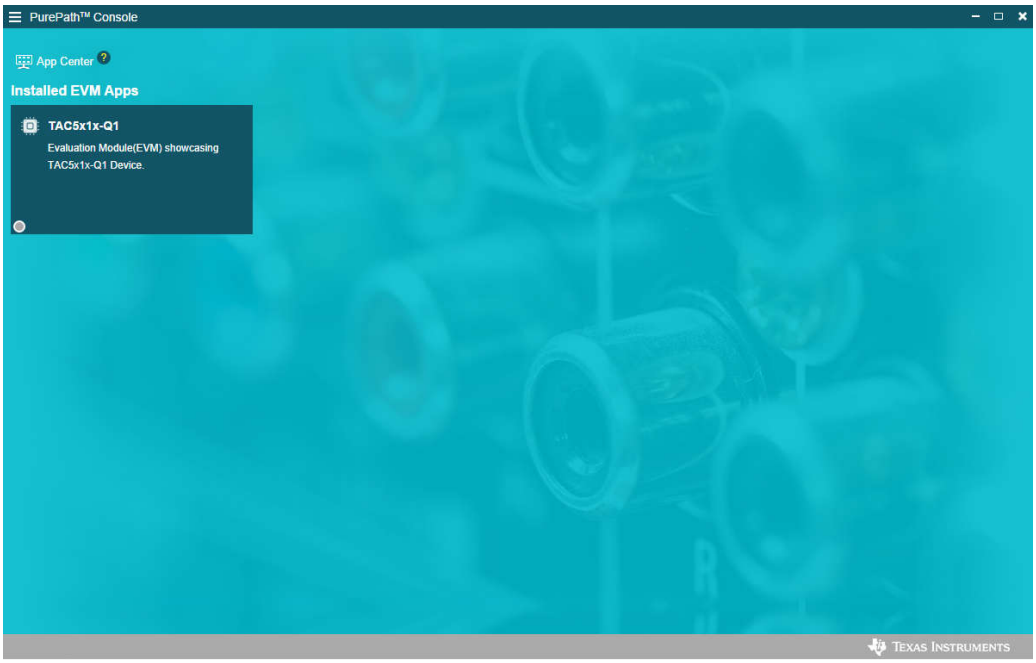

Figure 3-3. PurePath™ Console 3 App Center

The TAC5x1x-Q1 GUI is designed to work with up to four devices at any time. When an EVM is connected, the GUI auto-detects the device as shown in Figure 3-4. In this example, *TAC5412-Q1* (5x5) is detected and subsequent PPC3 Software sections are based on this device. Choose the *1 device* radio button and click *New*.

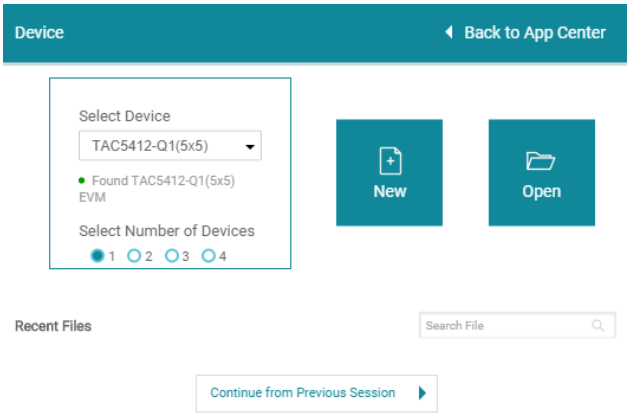

Figure 3-4. Device Selection

The GUI loads the default configuration and a warning message appears. Choose either to update the GUI with device values or overwrite the device with GUI values; either selection works for the initial setup.

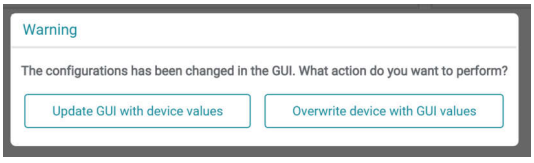

Figure 3-5. Update GUI-Device

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The default tabs of the connected device are displayed as shown below.

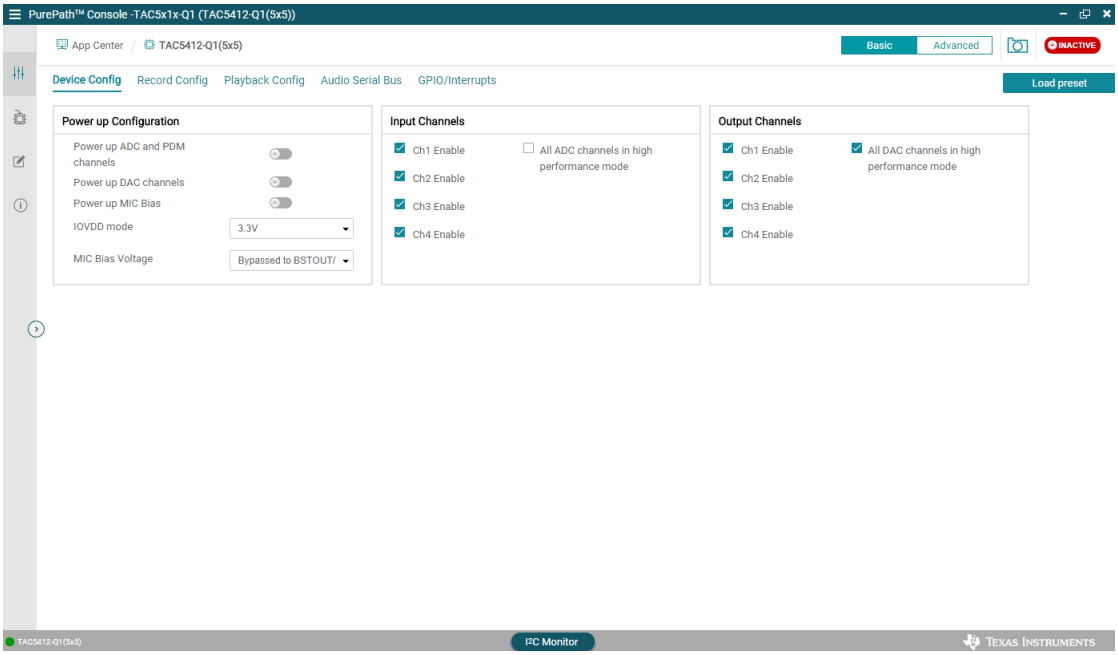

Figure 3-6. Device Config Tab

Before changing any parameters, check the lower left corner of the PPC3 window to verify that the EVM is connected. If no EVM is detected, the text reads TAC5412-Q1 - OFFLINE as shown in Figure 3-7. To connect, plug the USB cable to the computer.

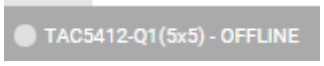

Figure 3-7. Hardware Offline

To activate the GUI, hit the *INACTIVE* red button to change to the *ACTIVE* green button. The GUI is now in operation. Users must first configure the device and then activate the PPC3. Once activated, some controls are grayed out until the *ACTIVE* button is deactivated.

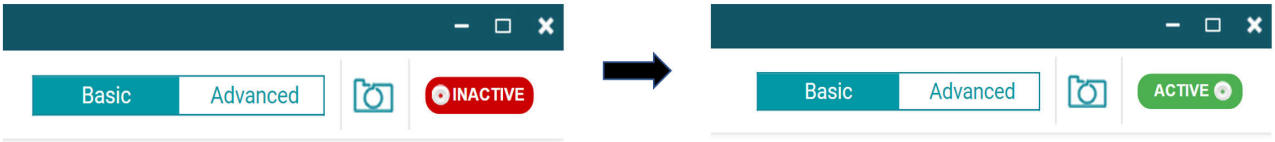

Figure 3-8. Activate GUI

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3.3.1 Software Overview

The TAx5x1x-Q1 EVM control software allows configuration of the TAx5x1x-Q1 EVM-PDK. The application has three main views: Configuration, End System Integration, and Register Map. These views are detailed in this section. Some controls in these tabs are grayed out when the tabs are not applicable to the selected device variant.

3.3.2 Configuration View

The configuration view, shown in Figure 3-9, contains all of the settings used to configure and program the TAx5x1x-Q1 EVM. This view has tabs associated to the device configuration.

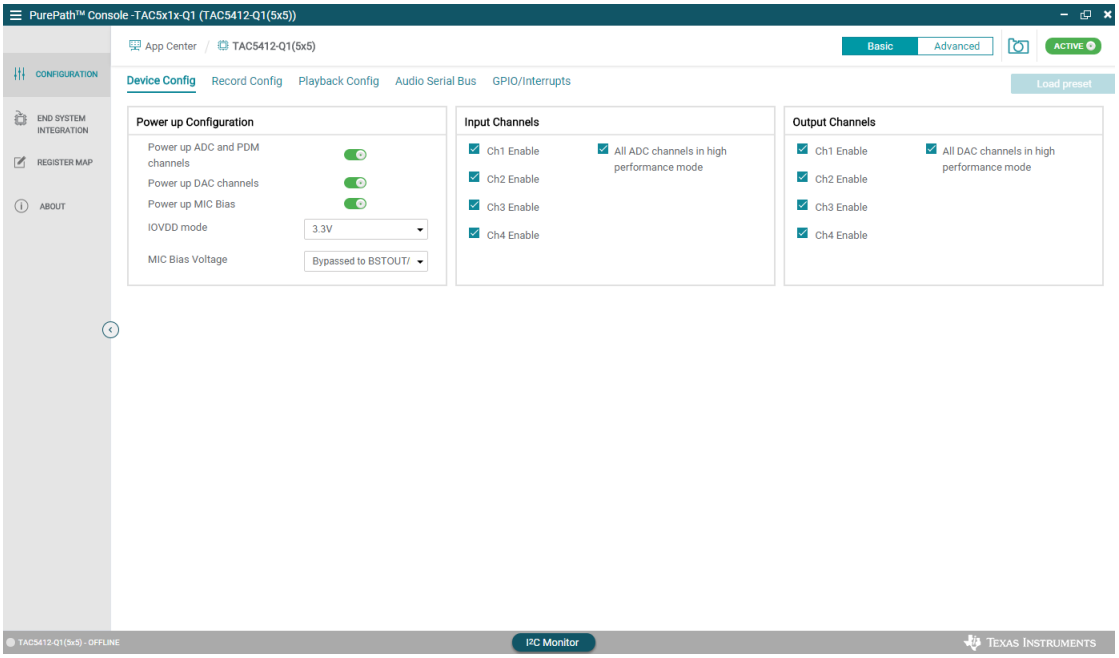

Figure 3-9. Configuration View

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3.3.2.1 Device Config Tab

The Device Config tab contains control to power/enable the analog blocks, the IO, MIC Bias level, the different input and output channel selections. Input channel 3 and channel 4 are associated with the PDM input channels.

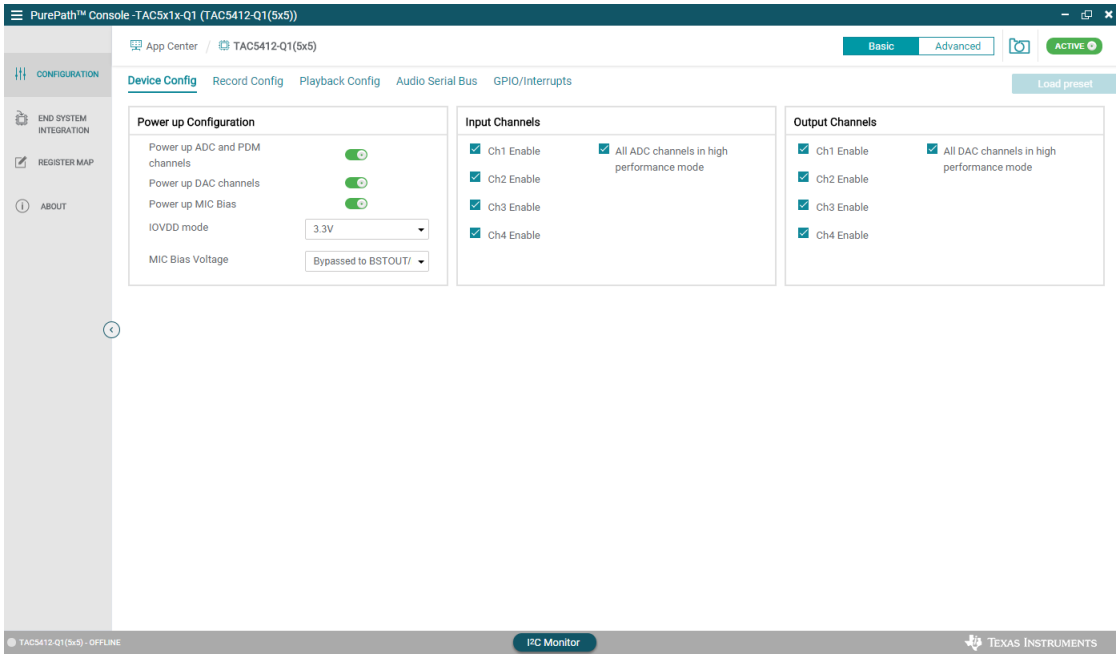

Figure 3-10. Device Config Tab

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3.3.2.2 Record Config Tab

The Record Config tab contains the controls for the analog inputs, the different input mode, the input impedance, the bandwidth and the level. The Record Config tab also has the slide buttons for adjusting the digital volume as well as the phase and gain calibrations. On the right hand side, there are pull down menus for selecting the HPF cutoff frequency and the latency of the decimation filter.

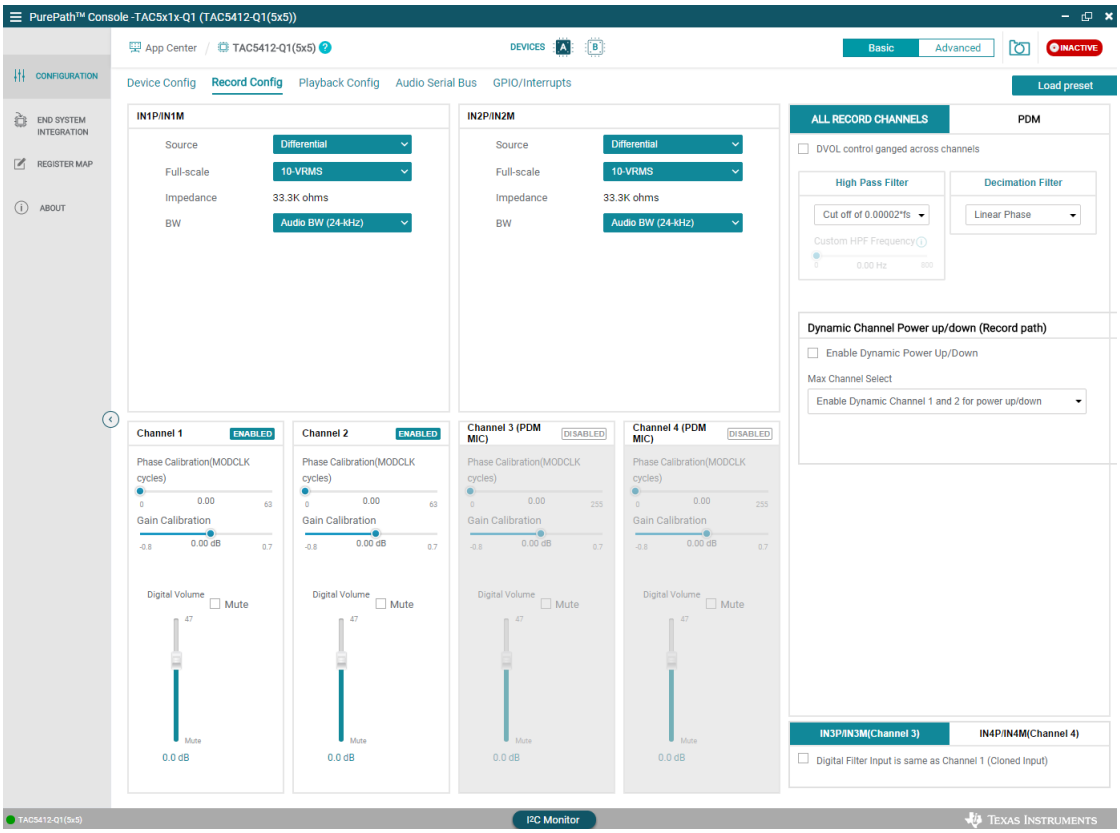

Figure 3-11. Record Config Tab

Input channel 3 and channel 4 are associated with Digital Microphone inputs. For PDM input, several PDM clock selections are available with the associated data and clock triggering in this record config tab.

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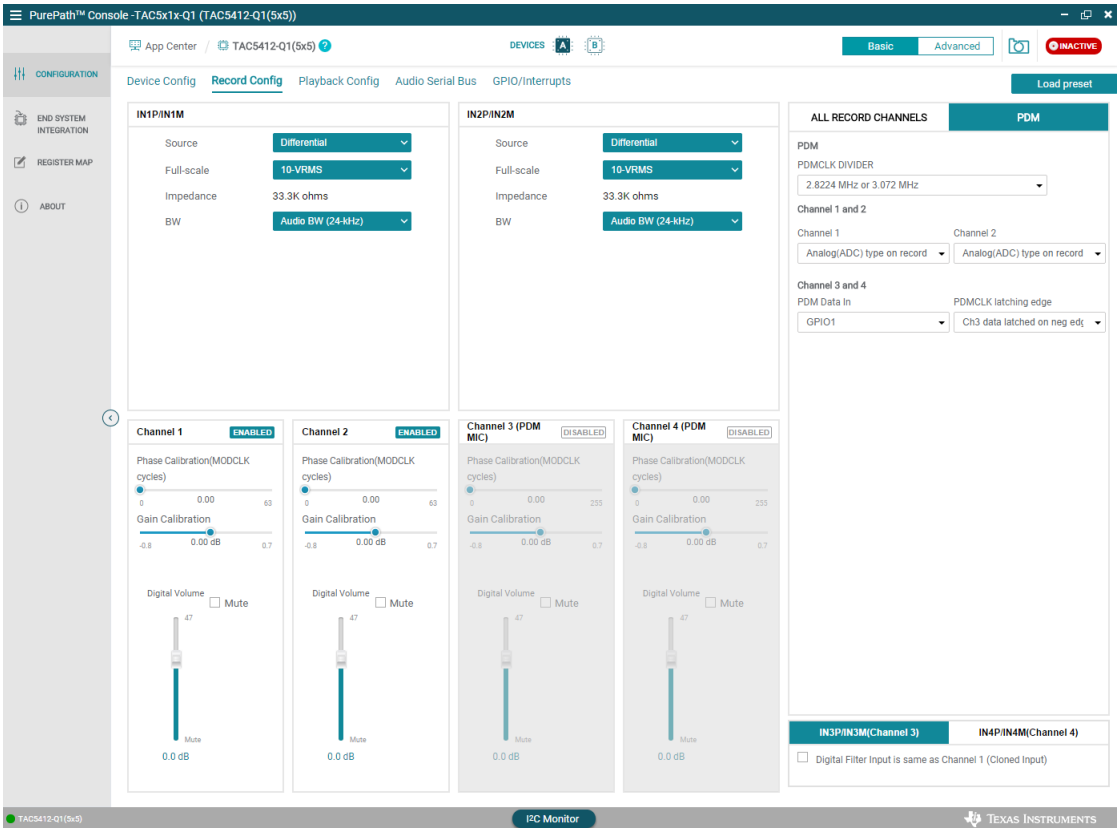

Figure 3-12. PDM Record Config Tab

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3.3.2.3 Playback Config Tab

In playback tab, the configurations to set the audio analog output path are provided here. The user can set the source of the output driver data, the output type, the output driver either LINEOUT or HEADPHONE and the output gain level. On the right hand side, the tab provides the high pass filter (HPF) cutoff frequency, the latency as well as the output common voltage (Vcom) and bandwidth. When gain is needed to compensate the output drivers, the gain calibration slide button can be used. Depending on the selection, some of the controls are grayed out, which means the controls are not available for configuration.

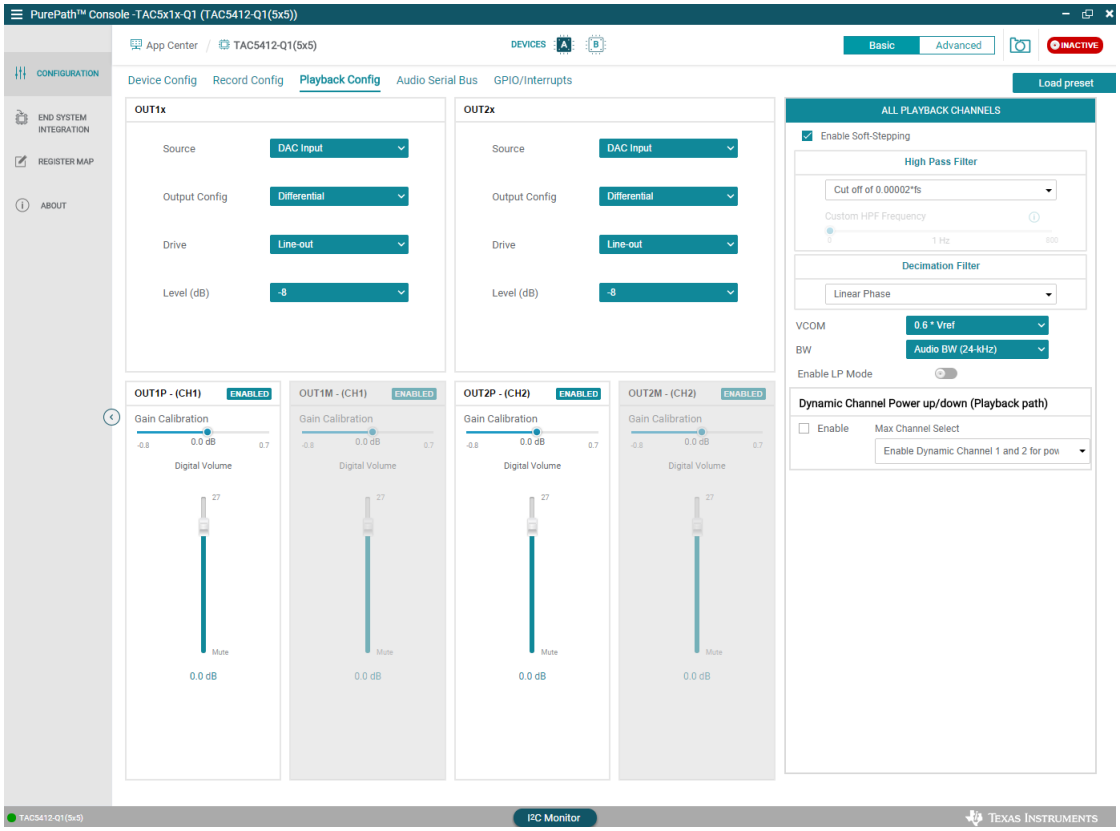

Figure 3-13. Playback Config

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3.3.2.4 Audio Serial Bus Tab

The TAx5x1x-Q1 family of devices features a very flexible audio serial bus. Allowing these devices to function seamlessly with various DSPs, SoCs, or other audio devices. The audio serial bus tab provides control to configure the EVM to the required format, mode, and the different channel/slot assignment for both transmit (ADC) and receive (DAC).

Besides the primary audio serial bus, the EVM supports a secondary audio serial bus when needed to interface with an external controller/device with the same flexibility.

3.3.2.4.1 Configuring Primary Audio Serial Bus

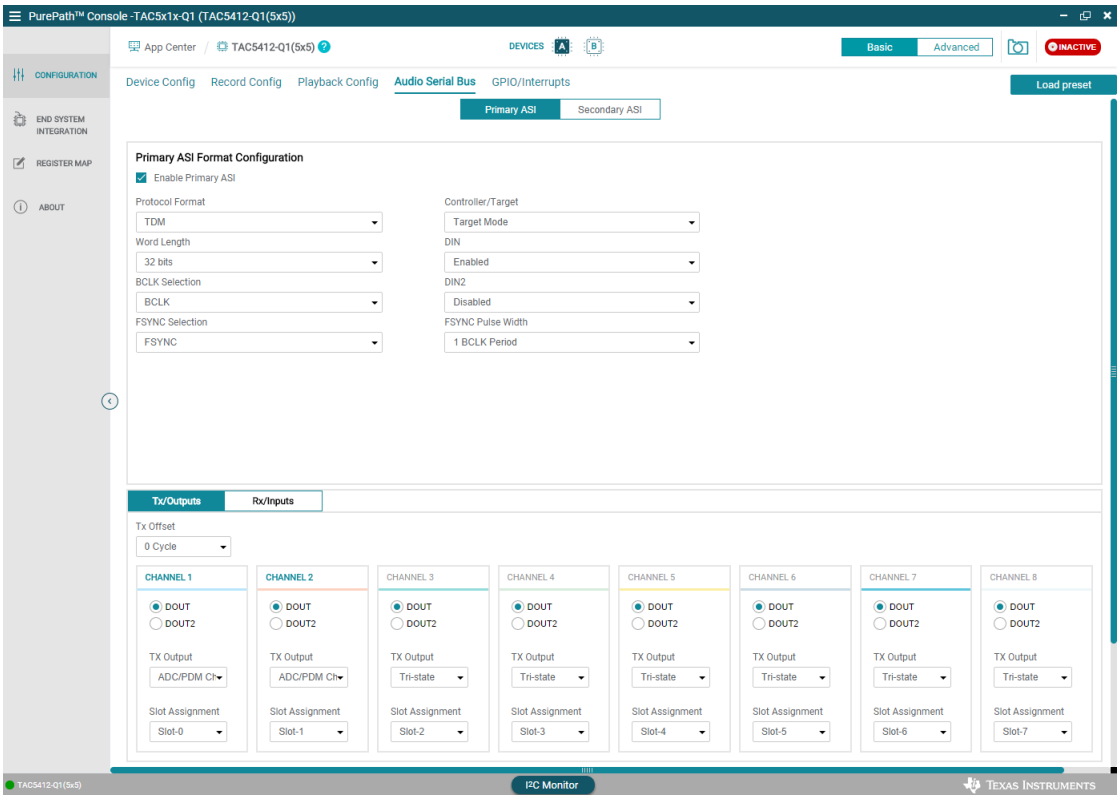

Figure 3-14. Primary Audio Serial Bus - Page 1

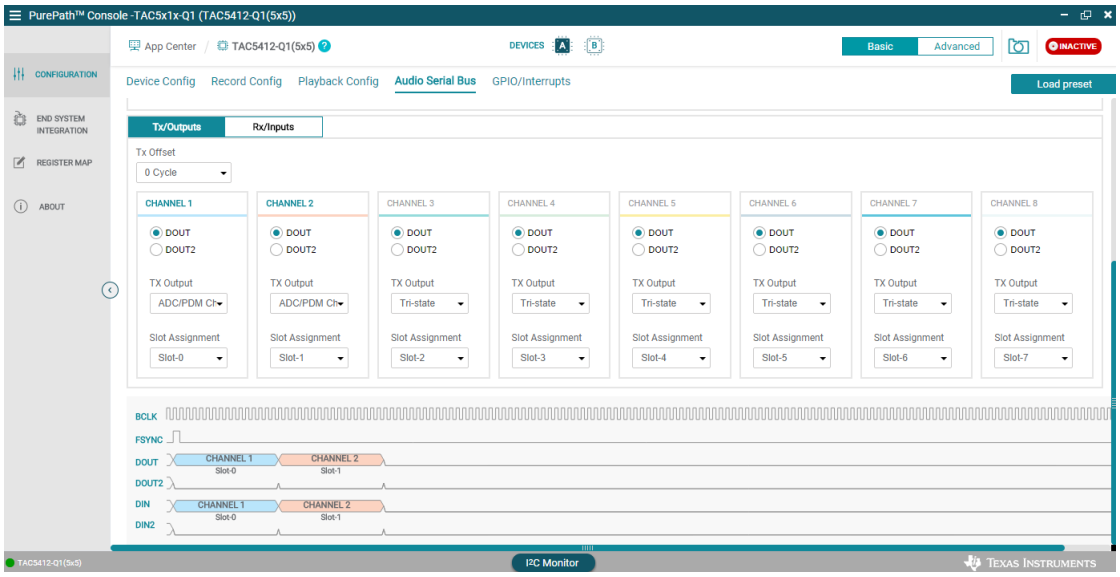

Figure 3-15. Primary Audio Serial Bus TX - Page 2

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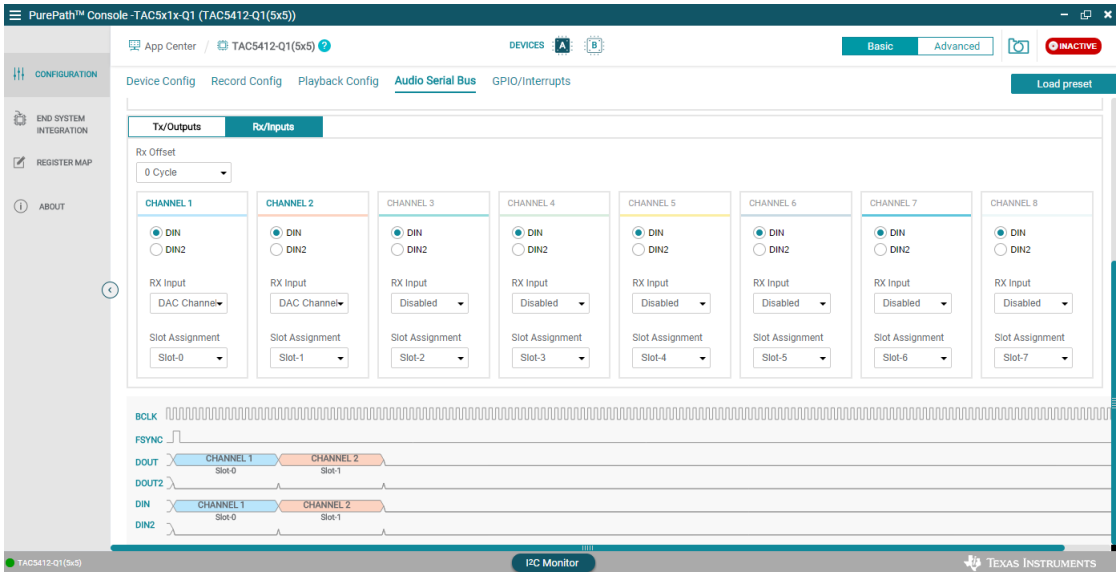

Figure 3-16. Primary Audio Serial Bus RX - Page 3

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3.3.2.4.2 Configuring Secondary Audio Serial Bus

A similar audio serial bus setting to the Primary interface is available under the Secondary ASI tab when a second audio serial bus is needed.

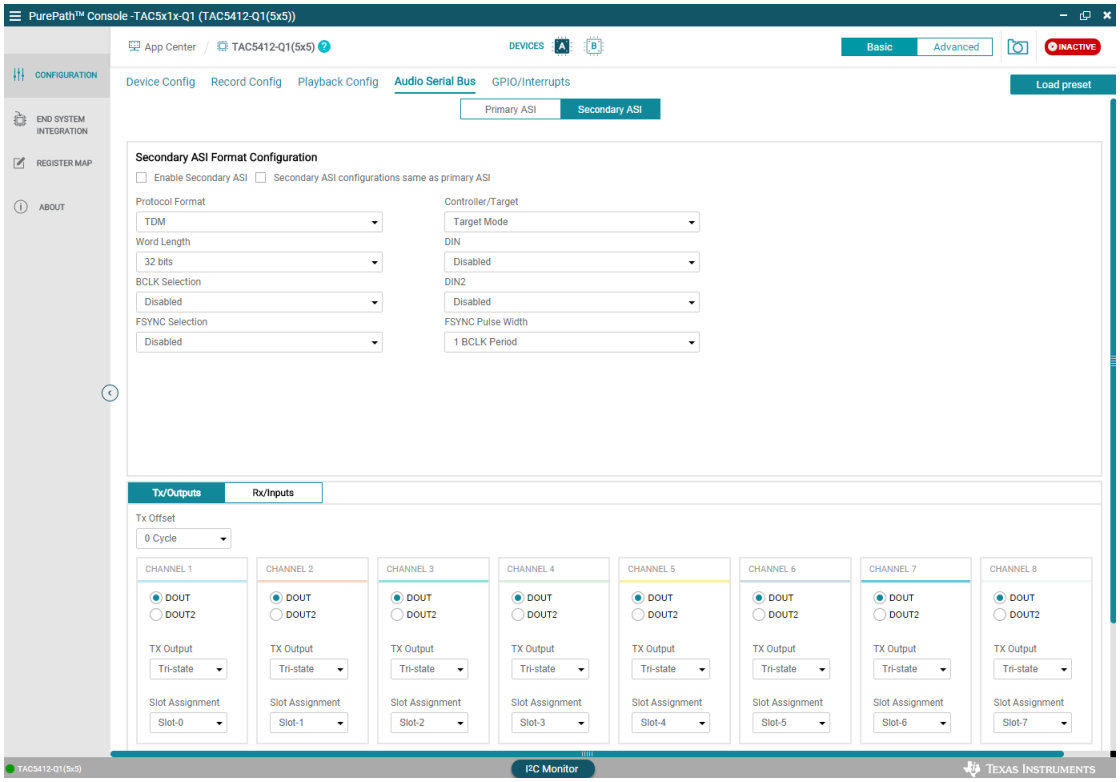

Figure 3-17. Secondary Audio Serial Bus Page 1

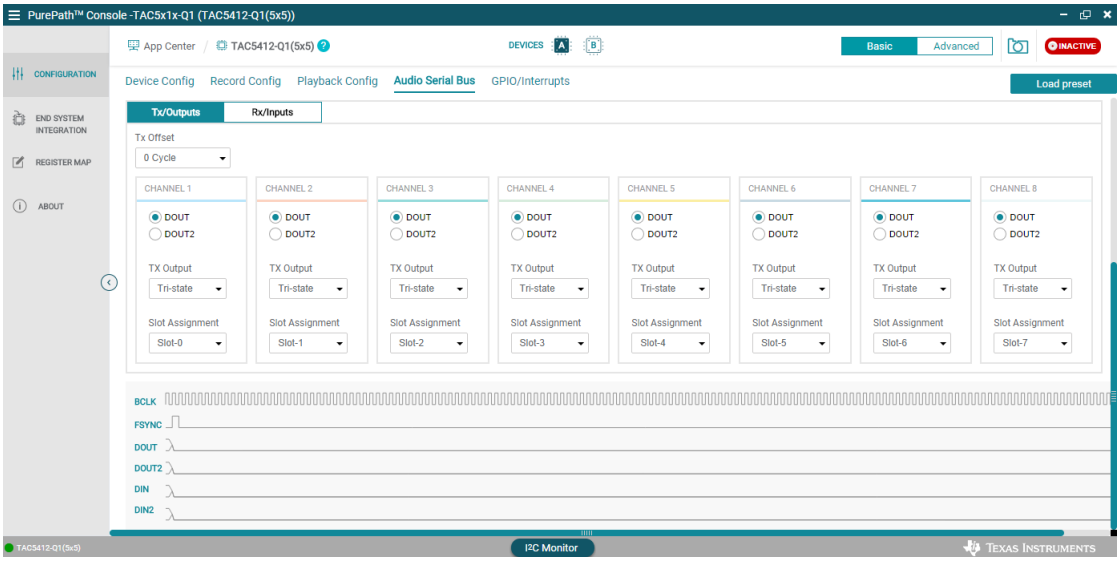

Figure 3-18. Secondary Audio Serial Bus TX - Page 2

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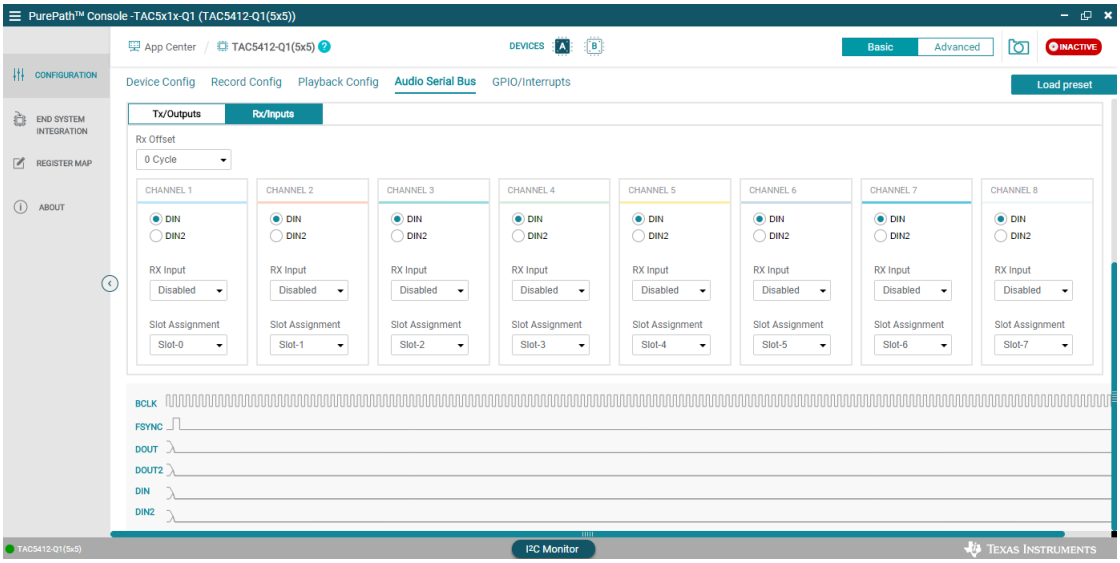

Figure 3-19. Secondary Audio Serial Bus RX - Page 3

3.3.2.4.3 Example Configuring I2S Interface

The TAx5x1x-Q1 features a highly flexible audio serial bus that can be configured to implement a wide range of data formats. The default format is TDM. However, the GUI can change the data format to I2S/LJ. This section shows a configuration example for a 2-channel I2S output to a USB audio at 16 bits and 48 kHz.

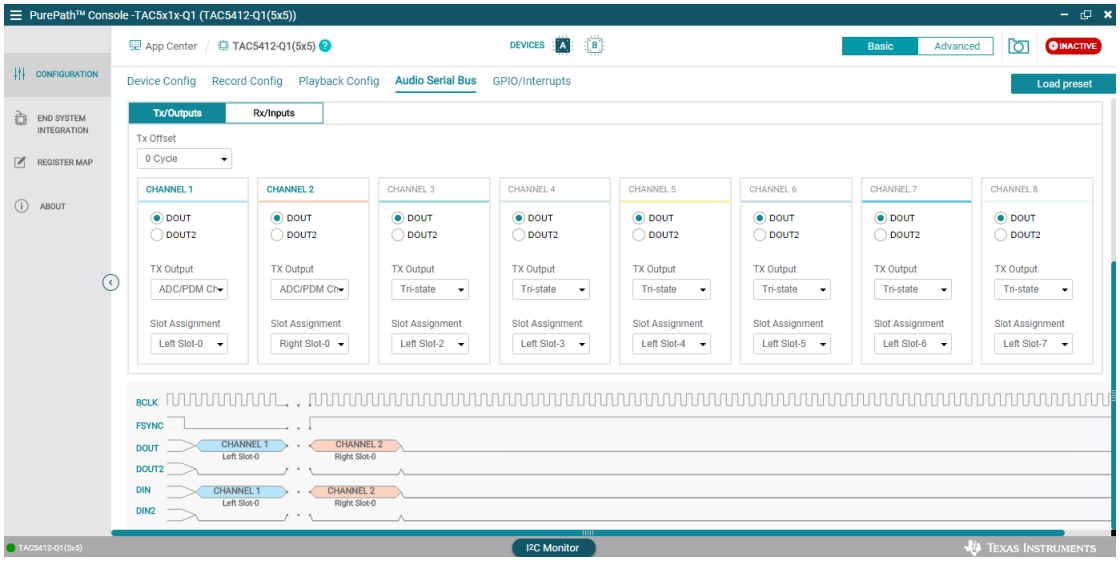

Figure 3-20. Configuring I2S Example

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3.3.2.5 GPIO/Interrupts Tab

As shown in the figure below, the GPIO function and interrupt behavior can be configured in this tab. There are two General Purpose Inputs (GPI1 and GPI2), one General Purpose Output (GPO1), and one General Purpose Input Output (GPIO1) in the TAx5x1x-Q1 devices. These general-purpose input/output drivers also provide several multiplexing functions, and the selection can also be configured in this tab. Depending on the selection, some controls are grayed out. On the right side is the Interrupt selection, which has the settings as well as flag update/status of the respective interrupt.

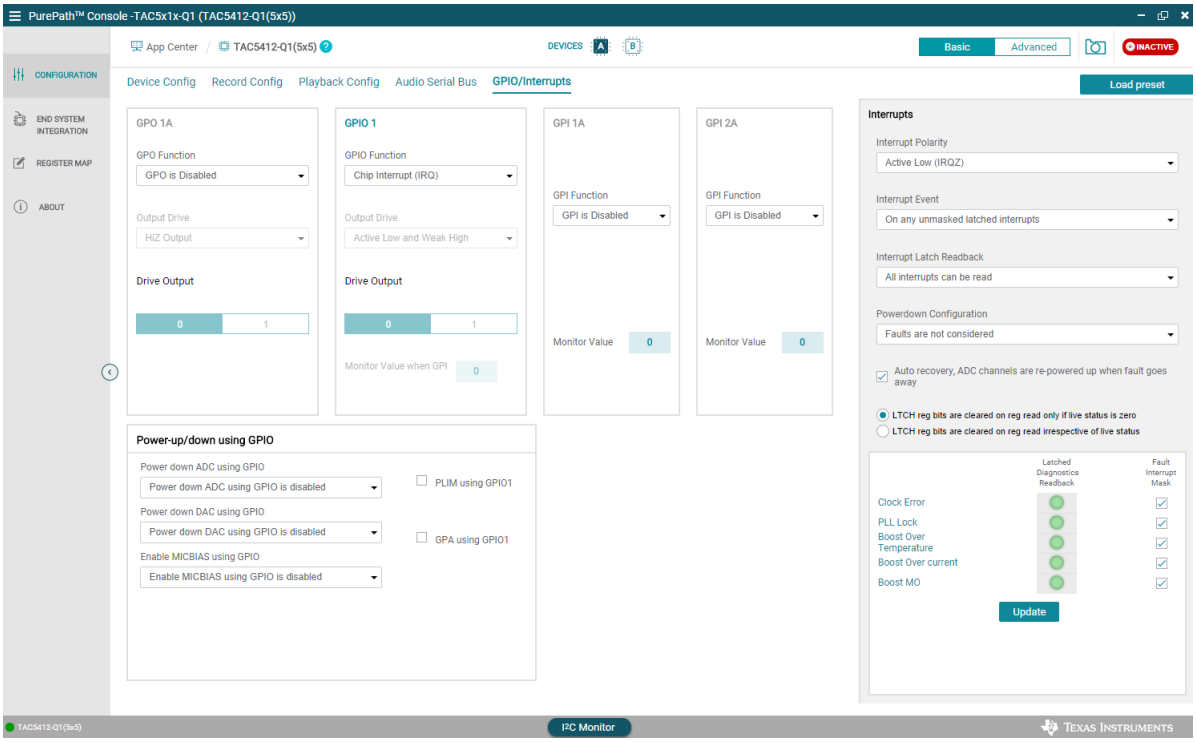

Figure 3-21. GPIO and Interrupts Tab

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3.3.2.6 Advanced Tabs

The following tabs are available in the Advanced feature. Click the *Advance* tab and a selection of other features are displayed. Select the feature to bring up the panel. Some of these features are not available in some device variants.

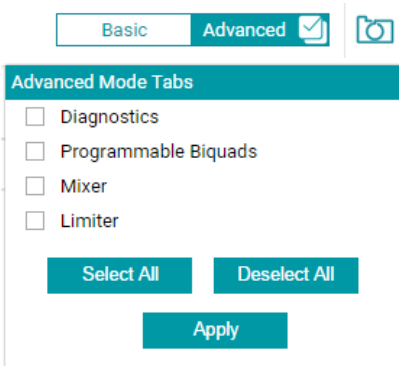

Figure 3-22. Advanced Feature

3.3.2.6.1 Diagnostic Tab

The diagnostics tab allows for the configuration and monitoring of the integrated diagnostics features of the TAx5x1x-Q1 devices. To enable diagnostic MICBIAS and PLL are required, so a message appears to allow user to turn them on. Click the *Turn On* button to enable diagnostic and the display is as shown below.

The latched fault status window also includes controls for mask interrupt. Any masked faults are displayed when a mask is enabled; however, these masks do not trigger an interrupt. Check the "Auto Update" button to automatically update the diagnostic status flag. Some diagnostic settings are available on the left hand side if needed.

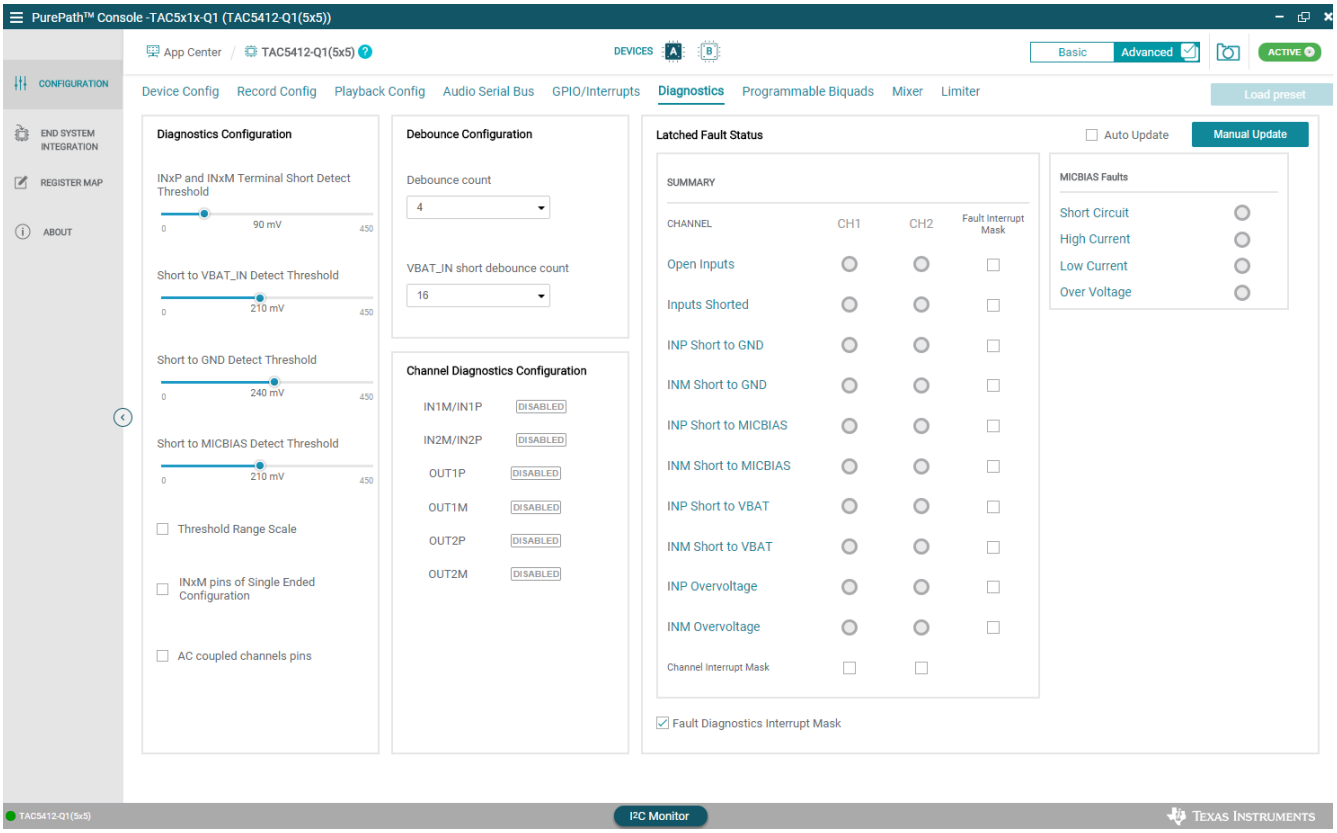

Figure 3-23. Diagnostic Tab

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3.3.2.6.2 Programmable Biquads Tab

Configuration of the biquad filters is made easy with the GUI in the programmable biquads tab. Biquad coefficients can be generated using the filter designers within PPC3 or biquad coefficients can be manually entered into the coefficients cells obtained from external filter tool. Each biquad can be configured individually, the gain and phase responses can then be shown for individual channels or all channels. Note that PPC3 uses the detected sampling rate from the audio serial bus tab to determine the biquad coefficients. The TAx5x1x-Q1 device must receive the desired sampling rate when the audio serial bus tab is opened, and the clock monitor must be updated by clicking the Read button. If no EVM is connected, PPC3 assumes sampling rate of 48 kHz for all biquad calculations.

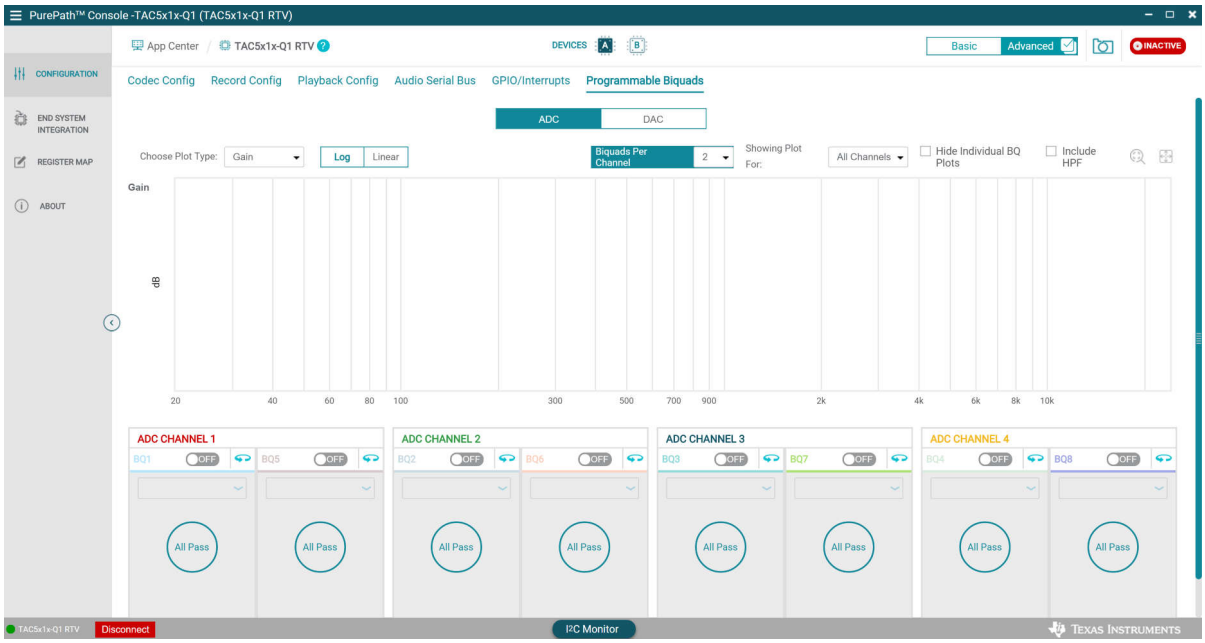

Figure 3-24. Programmable ADC Biquads Tab

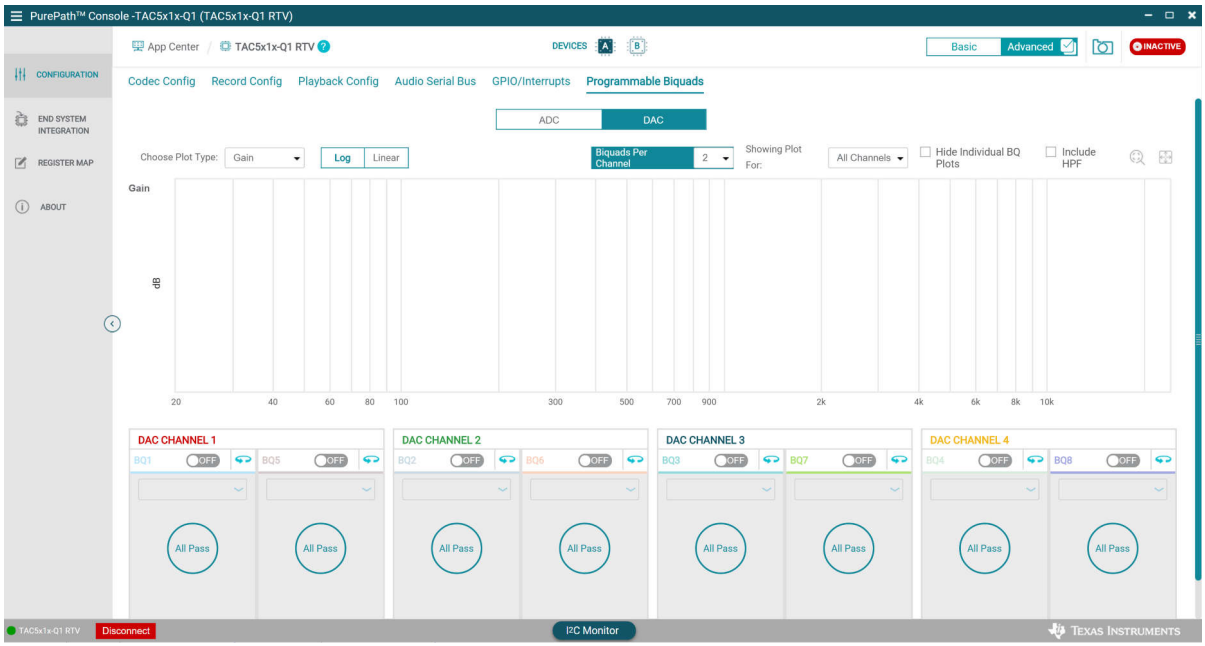

Figure 3-25. Programmable DAC Biquads Tab

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3.3.2.6.3 Mixer Tab

Some TAx5x1x devices support several mixing feature, settings are available in this tab. The ADC tab provides the mixing level/coefficient for each of the 4 ADC Mixers as well as the ADC Loopback. The level is in ratio, for example 0.5 represents half of the mixer full-scale range.

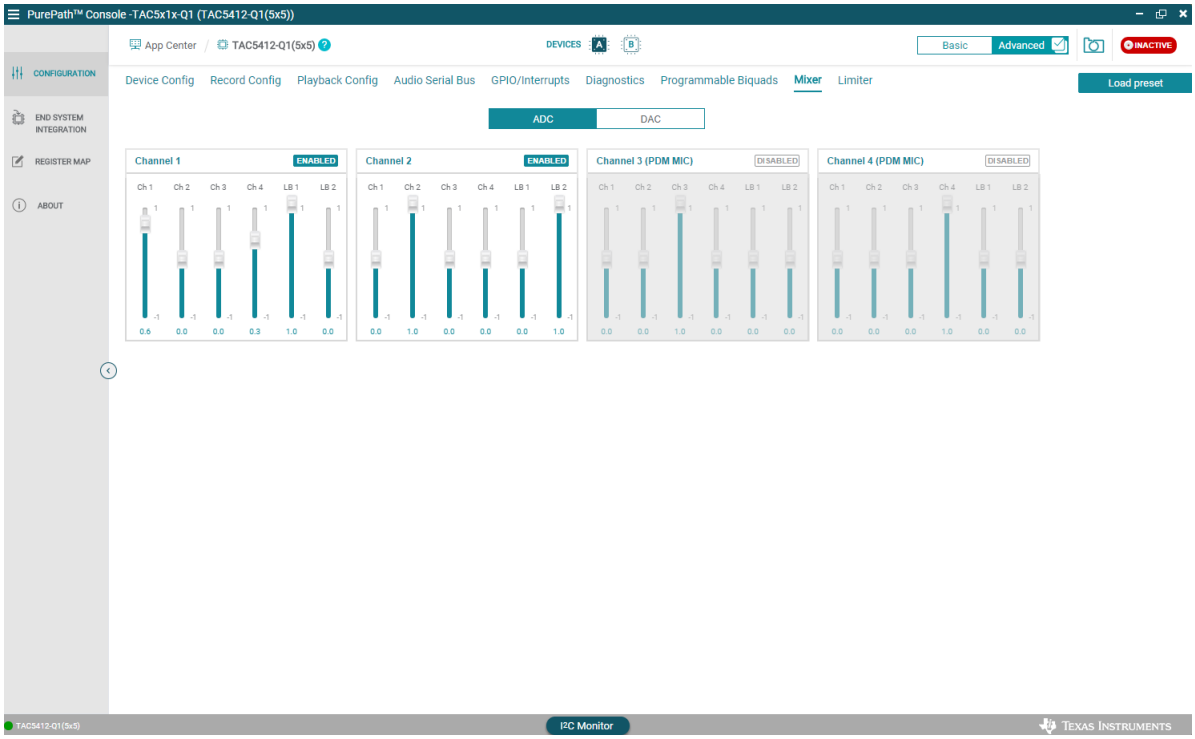

Figure 3-26. Mixer ADC Tab

In DAC tab, there are eight possible channels from main ASI and two possible channels from Auxiliary channels. The level is ratio of the mixer full-scale and user can enter in the cell provided. Besides the external inputs, there are beep and chirp generators that user can mix in DAC mixer as well.

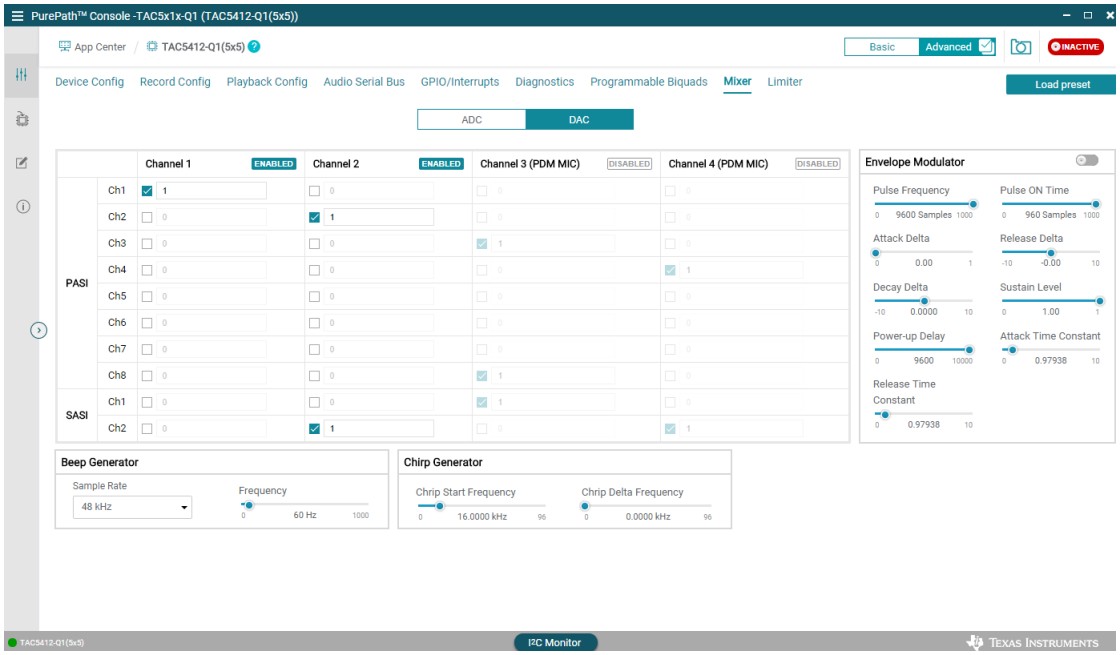

Figure 3-27. Mixer DAC Tab

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3.3.2.6.4 Limiter Tab

Various device limiters like brown out and temperature are available in this tab.

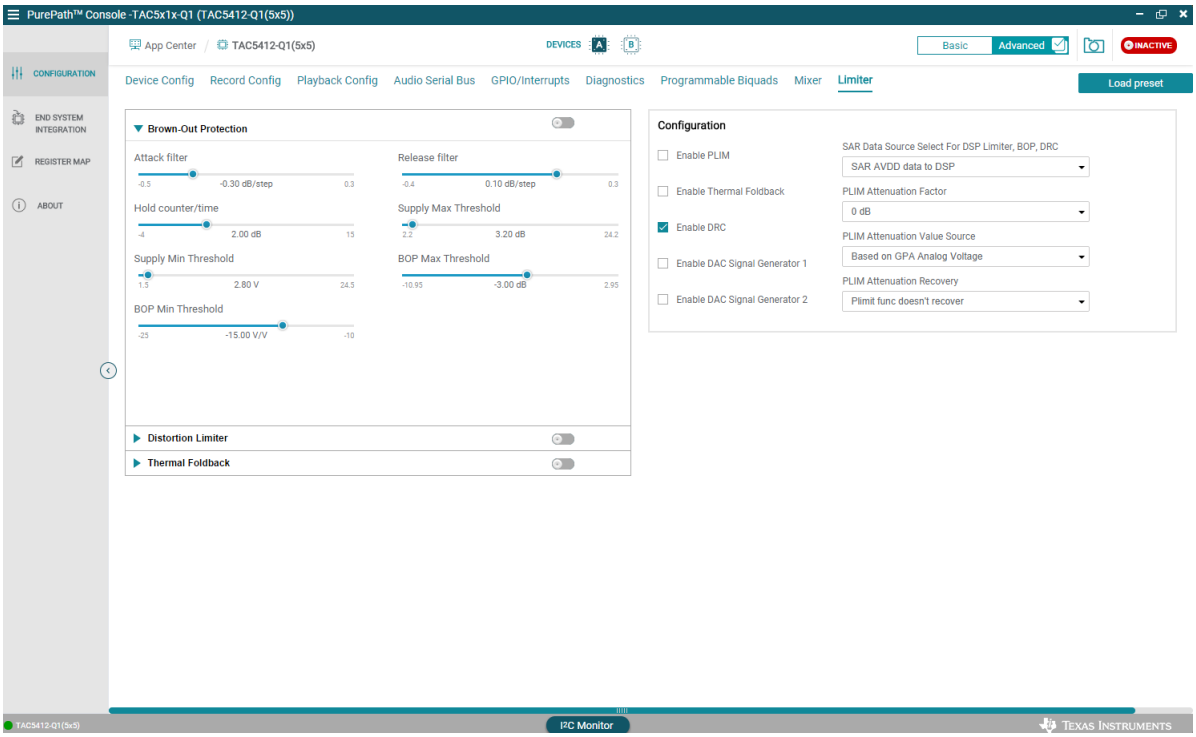

Figure 3-28. Limiter Tab

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3.3.3 End System Integration View

The End System Integration view provides methods for exporting the current configuration to a header (.h) or .cfg file. The header file can be used for quick integration with a simple microcontroller.

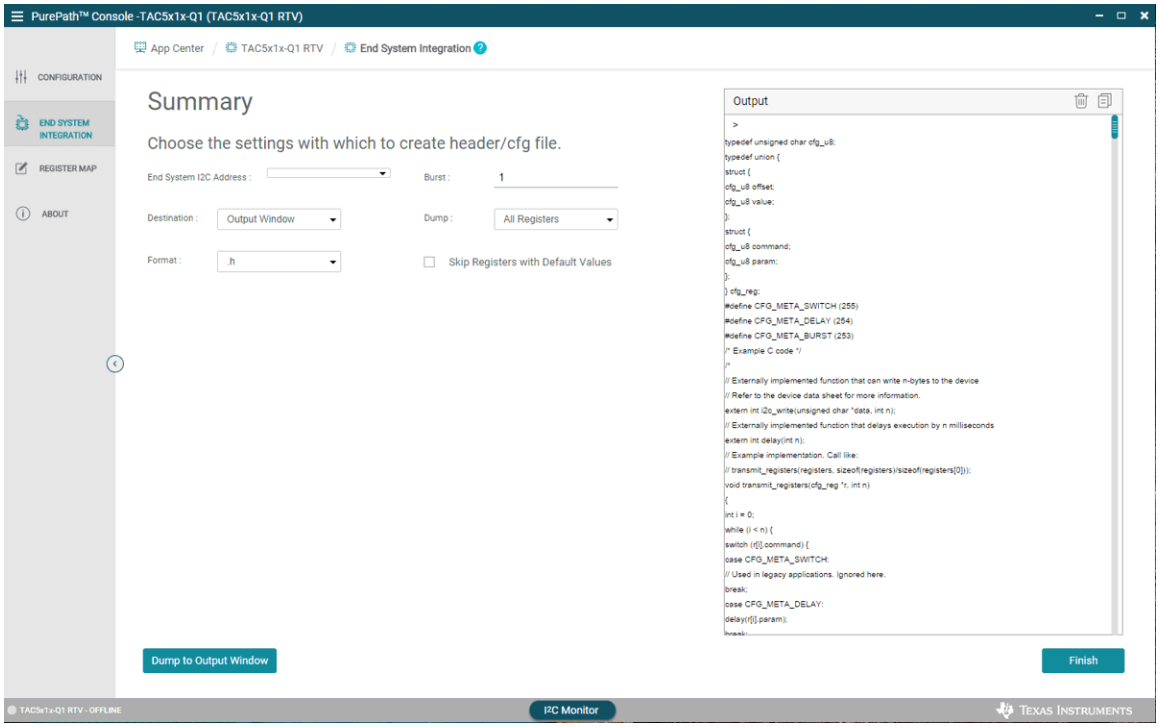

Figure 3-29. End System Configuration

3.3.4 Register Map View

The register map view provides a view of page 0, page 1, and page 3 of the register map.

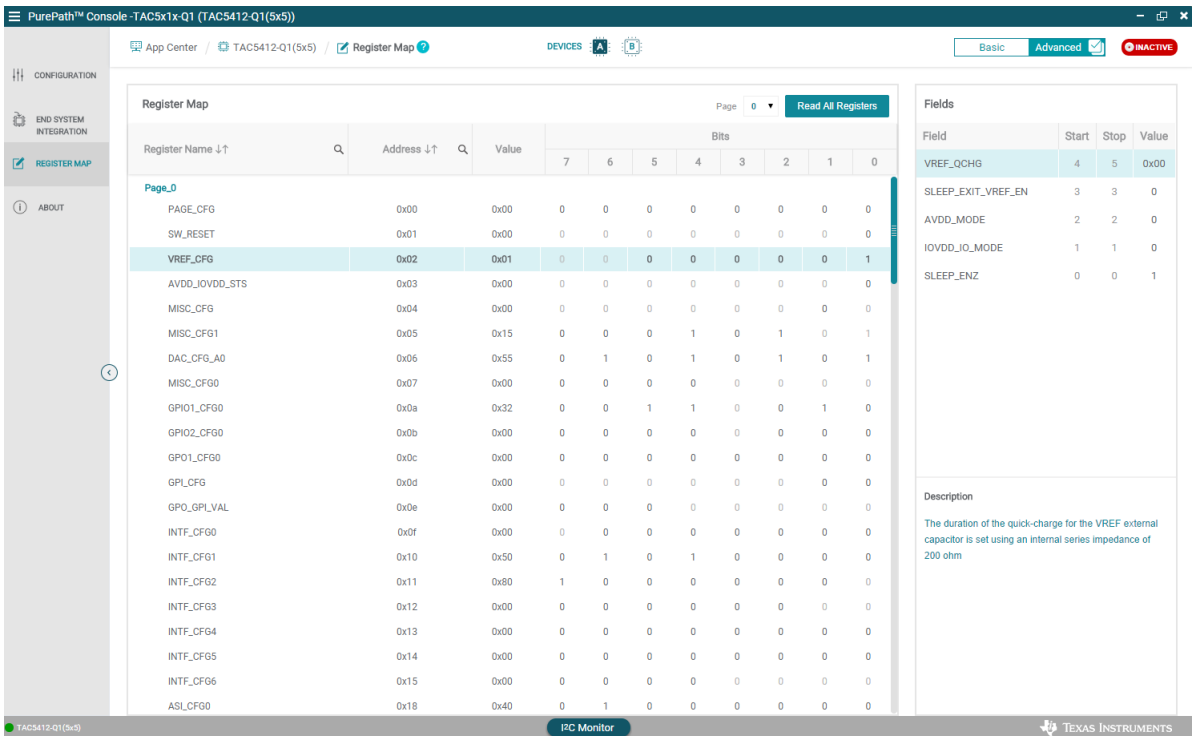

Figure 3-30. Register Map View

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3.3.5 Preset Configuration

There are several preset configurations that allow user to check the functionality of the device with the AC-MB Controller. Depending upon the device connected to the setup, the preset configurations that are available varies accordingly. Clicking the *Load Preset* button lists the preset configurations available for the device. Select and click *Load* to configure the device with the selected preset script and then activate the GUI.

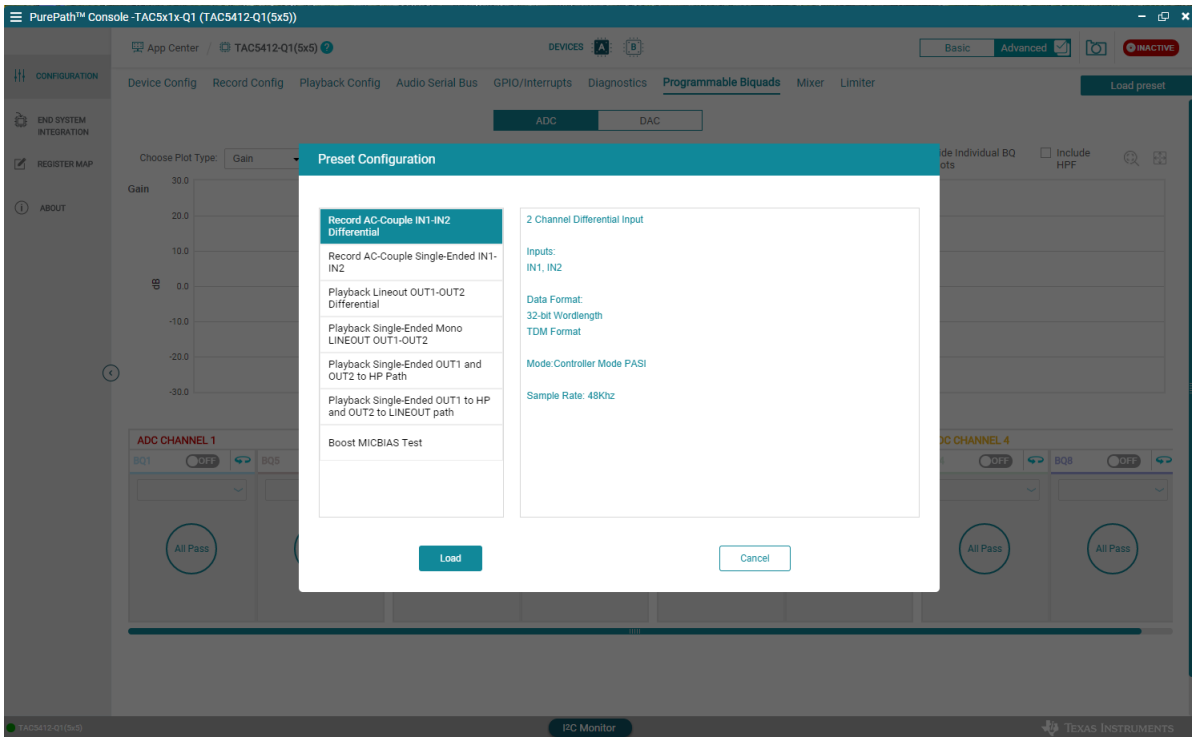

Figure 3-31. Preset Configuration

3.3.6 I2C Monitor View

The I2C Monitor tab allows users to load existing device configuration files or direct I2C transactions to the device registers. To access this window panel, click on the *I2C Monitor* button at the bottom of the GUI. The I2C monitor window opens as shown in the figure below. The LOG screen allows users to log or record any I2C transaction. This is useful when users wanted to record device register to use at later time, users can click on the green LED button once and the button turns to red for recording. To stop recording, just click the red LED button once and the button turns back to green.

To load an existing file or to manually write or read I2C transaction, click on the I/O button to open the input/ output window.

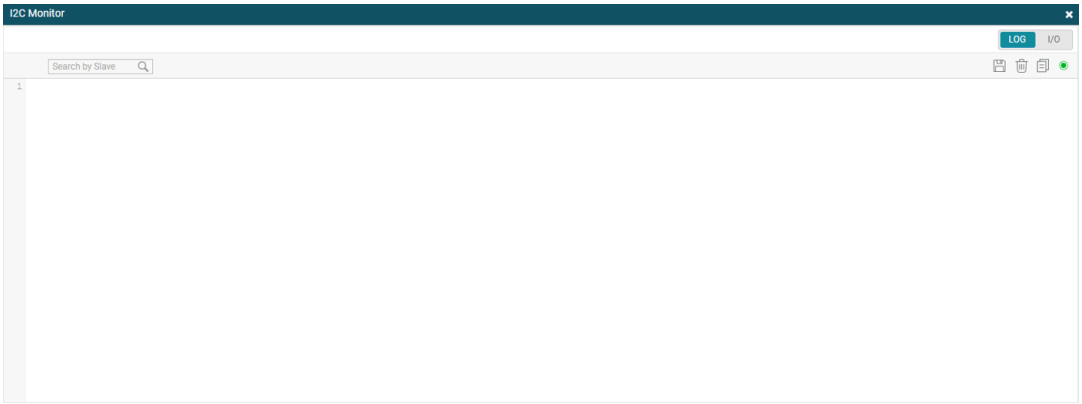

Figure 3-32. I2C Monitor Window

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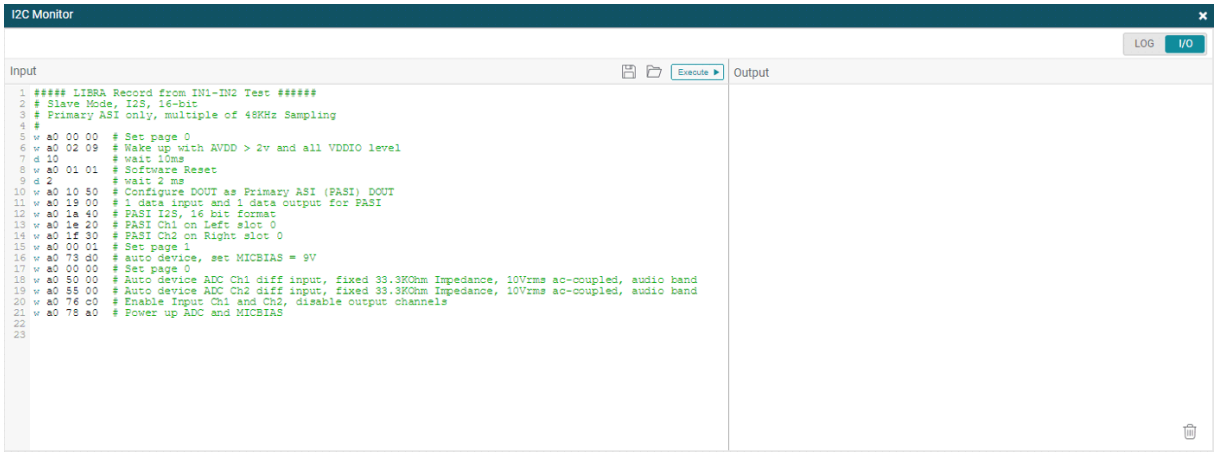

Figure 3-33. I2C Monitor I/O Window

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3.4 Configuration Examples

The following are several examples of configuring the device into the respective paths. These device configurations can be used with external host or instrument like Audio Precision. For testing with the AC_MB host of the EVM, use the GUI Preset Configuration. This is because the AC_MB host is configured to support only TDM and the polarity is different from these devices.

Users can copy the settings below and paste them into the I2C Monitor window to configure the device when used with external host/instrument.

- Target mode differential AC-couple recording with PASI

This configuration is for differential audio recording (ADC) with a 48 kHz sampling rate, TDM format, and 32-bit depth.

```
##### Record AC-Couple Differential IN1-IN2 path ######
# Target Mode, TDM, 32 bit
# Primary ASI only, multiple of 48 kHz Sampling
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50    # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 30    # PASI TDM, 32-bit format
w a0 1e 20    # PASI Ch1 on slot 0
w a0 1f 21    # PASI Ch2 on slot 1
w a0 00 01    # Set page 1
w a0 73 D0    # auto device, set MICBIAS = 9V
w a0 00 00    # Set page 0
w a0 50 00    # Auto device ADC Ch1 diff input, fixed 33.3KOhm, 10Vrms ac-coupled, audio band
w a0 55 00    # Auto device ADC Ch2 diff input, fixed 33.3KOhm, 10Vrms ac-coupled, audio band
w a0 76 c0    # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0    # Power up ADC and MICBIAS
```

- Target mode single-ended AC-couple recording with PASI

This configuration is for single-ended audio recording (ADC) with a 48 kHz sampling rate, I2S format, and 32-bit depth.

```
##### Record AC-Couple Single-Ended IN1-IN2 path ######
# Target Mode, I2S, 32 bit
# Primary ASI only, multiple of 48KHz Sampling
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50    # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 70    # PASI I2S, 32-bit format
w a0 1e 20    # PASI Ch1 on Left slot 0
w a0 1f 30    # PASI Ch2 on Right slot 0
w a0 00 01    # Set page 1
w a0 73 d0    # auto device, set MICBIAS = 9V
w a0 00 00    # Set page 0
w a0 50 40    # Auto device ADC Ch1 SE input, fixed 33.3KOhm, ac-coupled, audio band
w a0 55 40    # Auto device ADC Ch2 SE input, fixed 33.3KOhm, ac-coupled, audio band
w a0 76 c0    # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0    # Power up ADC and MICBIAS
```


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- Controller mode differential AC-couple recording with PASI

This configuration is for differential audio recording (ADC) with 48 kHz sampling rate, I2S format and 32-bit depth, and MCLK of 12.288 MHz.

```
##### Record AC-Couple Differential IN1-IN2 path ######
# Controller Mode, I2S, 32-bit, GPIO1 = CCLK from BCLK2 @ 12.288 MHz
# Primary ASI only, multiple of 48 kHz Sampling
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10    # configure GPIO1 as input
w a0 0f 20    # Set GPIO1=CCLK
w a0 10 50    # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 70    # PASI I2S, 32-bit format
w a0 1e 20    # PASI Ch1 on Left slot 0
w a0 1f 30    # PASI Ch2 on Right slot 0
w a0 32 50    # PASI Fs=48KHz with auto clock configuration
w a0 34 48    # PLL always enabled with fractional allowed and from fixed clk frequency
w a0 37 30    # Use MCLK=12.288 MHz, PASI in controller mode
w a0 38 80    # Use internal BCLK for FSYNC generation in controller mode
w a0 39 40    # Set controller mode BCLK/FSYNC ratio to 64 = h40
w a0 00 01    # Set page 1
w a0 73 d0    # auto device, set MICBIAS = 9V
w a0 00 00    # Set page 0
w a0 50 00    # Auto device ADC Ch1 diff input, fixed 33.3KOhm, 10Vrms ac-coupled, audio band
w a0 55 00    # Auto device ADC Ch2 diff input, fixed 33.3KOhm, 10Vrms ac-coupled, audio band
w a0 76 c0    # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0    # Power up ADC and MICBIAS
```

- Target mode digital mic recording with PASI

This configuration is for audio recording (ADC) from 2 digital microphones with a 48 kHz sampling rate, I2S format, and 32-bit depth.

```
##### Record from DMIC Test ######
# Target Mode, I2S, 32-bit
# Primary ASI only, multiple of 48 kHz Sampling 5 x 5-Q1
# PDMCLK=GPIO1, PDM Data=GPI1
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 41    # Configure GPIO1 as PDMCLK with drive active high and low
w a0 0d 02    # Configure GPI1 as input
w a0 10 50    # Configure DOUT as Primary ASI (PASI) DOUT
w a0 13 cc    # PDM ch 1 data latched on negative edge and ch 2 data latched on positive edge
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 70    # PASI I2S, 32-bit format
w a0 1e 20    # PASI Ch1 on Left slot 0
w a0 1f 30    # PASI Ch2 on Right slot 0
w a0 35 00    # PDM_CLK is 2.8224 MHz or 3.072 MHz
w a0 76 c0    # Enable input Ch1 and Ch2, disable output channels
w a0 78 80    # Power up ADC
```


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- Target mode differential AC-couple recording with Secondary Audio Serial Interface (SASI)

This configuration is for differential audio recording (ADC) with a 48 kHz sampling rate, TDM format, and 32-bit depth.

```
##### Record AC-Couple Differential IN1-IN2 path ######
# Target Mode, TDM, 32 bit
# Secondary ASI only, multiple of 48 kHz Sampling
# GPI2A=Secondary FSYNC, GPIO1=Secondary BCLK, GPO1A=Secondary DOUT, GPI1A=Secondary DIN for 5x5-Q1
#
w a0 00 00    # Sets page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10    # GPIO1 as input
w a0 0d 03    # GPI1 and GPI2 as input
w a0 0c 70    # GPO1 as Secondary DOUT
w a0 11 22    # Set GPI2A as Secondary FSYNC and GPIO1 as Secondary BCLK
w a0 12 60    # Set GPI1A as Secondary DIN
w a0 18 80    # Disable Primary ASI
w a0 34 44    # SASI BCLK is the input clock source
w a0 00 03    # Sets page 3
w a0 1e 20    # SASI Ch1 on slot 0
w a0 1f 21    # SASI Ch2 on slot 1
w a0 00 01    # Set page 1
w a0 73 d0    # auto device, set MICBIAS = 9V
w a0 00 00    # Sets page 0
w a0 50 00    # Auto device ADC Ch1 diff input, fixed 33.3KOhm, 10Vrms ac-coupled, audio band
w a0 55 00    # Auto device ADC Ch2 diff input, fixed 33.3KOhm, 10Vrms ac-coupled, audio band
w a0 76 C0    # Enable Input Ch1 and Ch2, disable output channels
w a0 78 A0    # Power up ADC and MICBIAS
```

- Target mode differential DC-couple recording with PASI

This configuration is for differential audio recording (ADC) with a 48 kHz sampling rate, I2S format, and 32-bit depth.

```
##### Record DC-Couple IN1-IN2 path ######
# Target Mode, I2S, 32 bit
# Primary ASI only, multiple of 48 kHz Sampling
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 10 50    # Configure DOUT as Primary ASI (PASI) DOUT
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 70    # PASI I2S, 32-bit format
w a0 1e 20    # PASI Ch1 on Left slot 0
w a0 1f 30    # PASI Ch2 on Right slot 0
w a0 00 01    # Set page 1
w a0 73 d0    # auto device, set MICBIAS = 9V
w a0 00 00    # Set page 0
w a0 50 04    # Auto device ADC Ch1 DIFF input, fixed 33.3KOhm, ac/dc-coupled, audio band
w a0 55 04    # Auto device ADC Ch2 DIFF input, fixed 33.3KOhm, ac/dc-coupled, audio band
w a0 76 c0    # Enable Input Ch1 and Ch2, disable output channels
w a0 78 a0    # Power up ADC and MICBIAS
```


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- Target mode playback to differential LINEOUT with PASI

This configuration is for differential audio playback (DAC) with a 48 kHz sampling rate, TDM format, and 32-bit depth.

```
##### Playback Differential LINEOUT Path ######
# Target Mode, TDM, 32 bit
# Primary ASI only, multiple of 48 kHz Sampling
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 11 80    # Enable PASI DIN
w a0 19 00    # 1 data inputs and 1 data outputs for PASI
w a0 1a 30    # PASI TDM, 32-bit format
w a0 28 20    # PASI DIN Ch1 on TDM slot 0
w a0 29 21    # PASI DIN Ch2 on TDM slot 1
w a0 64 20    # Configure OUT1P/M as differential from DAC1
w a0 65 20    # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20    # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20    # Configure OUT2P/M as differential from DAC2
w a0 6c 20    # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20    # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 0c    # Disable all input channels and enable output channel 1 and 2
w a0 78 40    # Power up all DAC channel
```

- Target mode playback to single-ended LINEOUT with PASI

This configuration is for single-ended mono audio playback (DAC) with a 48 kHz sampling rate, TDM format, and 32-bit depth.

```
##### Playback Single-Ended Mono LINEOUT Path ######
# Target Mode, TDM, 32 bit
# Primary ASI only, multiple of 48 kHz Sampling
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 11 80    # Enable PASI DIN
w a0 19 00    # 1 data inputs and 1 data outputs for PASI
w a0 1a 30    # PASI TDM, 32-bit format
w a0 28 20    # PASI DIN Ch1 on TDM slot 0
w a0 29 21    # PASI DIN Ch2 on TDM slot 1
w a0 64 28    # Configure OUT1P as mono single-ended from DAC1
w a0 65 20    # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20    # Configure 2Vrms Differential
w a0 6b 28    # Configure OUT2P as mono single-ended from DAC2
w a0 6c 20    # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20    # Configure 2Vrms Differential
w a0 76 0c    # Disable all input channels and enable output channel 1 and 2
w a0 78 40    # Power up all DAC channel
```


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- Target mode playback to differential LINEOUT with SASI

This configuration is for differential audio playback (DAC) with a 48 kHz sampling rate, TDM format, and 32-bit depth.

```
##### Playback Differential LINEOUT Path ######
# Target Mode, TDM, 32 bit
# Secondary ASI only, multiple of 48 kHz Sampling
# GPI2A = Secondary FSYNC, GPIO1 = Secondary BCLK, GPI1A = Secondary DIN, GPO1A=Secondary DOUT for
5x5-Q1
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 0a 10    # GPIO1 as input
w a0 0d 03    # GPI1 and GPI2 as input
w a0 0c 70    # GPO1 as Secondary DOUT
w a0 11 22    # Set GPI2A as Secondary FSYNC and GPIO1 as Secondary BCLK
w a0 12 60    # Set GPI1A as Secondary DIN
w a0 18 80    # Disable Primary ASI
w a0 34 44    # SASI BCLK is the input clock source
w a0 19 00    # 1 data input and 1 data output for SASI
w a0 00 03    # Set page 3
w a0 1a 30    # SASI TDM, 32 bit format
w a0 28 20    # SASI DIN Ch1 on TDM slot 0
w a0 29 21    # SASI DIN Ch2 on TDM slot 1
w a0 00 00    # Set page 0
w a0 64 20    # Configure OUT1P/M as differential from DAC1
w a0 65 20    # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20    # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20    # Configure OUT2P/M as differential from DAC2
w a0 6c 20    # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20    # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 0c    # Disable all input channels and enable output channel 1 and 2
w a0 78 40    # Power up all DAC channels
```

- Controller mode playback to differential LINEOUT with SASI

This configuration is for differential audio playback (DAC) with a 44.1 kHz sampling rate, TDM format 32-bit depth, and MCLK of 12.288 MHz.

```
##### Playback Differential LINEOUT Path ######
# Controller Mode MCLK = 12.288 MHz, TDM, 32-bit
# Secondary ASI only, multiple of 44.1 kHz Sampling
# GPIO1=Secondary FSYNC, GPI2A=CCLK Input, GPI1A=Secondary DIN, GPO1A=Secondary BCLK for 5 x 5 - Q1
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 0a a0    # GPIO1 as Secondary FSYNC output
w a0 0d 03    # GPI1 and GPI2 as input
w a0 0c 90    # GPO1A as Secondary BCLK output
w a0 0f 40    # GPI2A as CCLK input
w a0 11 14    # GPIO1 as Secondary FSYNC
w a0 12 60    # Set GPI1A as Secondary DIN
w a0 18 80    # Disable Primary ASI
w a0 32 00    # Auto clock configuration
w a0 33 50    # SASI Fs = 48 kHz (41895-49440) with Auto clock configuration
w a0 34 48    # PLL always enabled with fractional allowed and from fixed clk frequency
w a0 36 00    # auto detect the ratio
w a0 37 29    # Use MCLK=12.288 MHz, SASI in controller configuration with rate multiple of 44.1 kHz
w a0 3a 81    # Use internal BCLK for FSYNC generation for SASI, BCLK/FSYNC ratio=256
w a0 3b 00    # use BCLK/FSYNC ratio of 256 for SASI
w a0 00 03    # Set page 3
w a0 1a 30    # SASI TDM, 32 bit format
w a0 28 20    # SASI DIN Ch1 on TDM slot 0
w a0 29 21    # SASI DIN Ch2 on TDM slot 1
w a0 00 00    # Set page 0
w a0 64 20    # Configure OUT1P/M as differential from DAC1
w a0 65 20    # Configure OUT1P LINEOUT 0dB audio band
w a0 66 20    # Configure OUT1M LINEOUT 0dB 2Vrms Differential
w a0 6b 20    # Configure OUT2P/M as differential from DAC2
w a0 6c 20    # Configure OUT2P LINEOUT 0dB audio band
w a0 6d 20    # Configure OUT2M LINEOUT 0dB 2Vrms Differential
w a0 76 0c    # Disable all input channels and enable output channel 1 and 2
w a0 78 40    # Power up all DAC channels
```


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- Target mode playback to differential headphones with PASI

This configuration is for differential audio playback (DAC) with a 48 kHz sampling rate, I2S format, and 32-bit depth.

```
##### Playback Differential Headphone Path ######
# Target Mode, I2S, 32-bit
# Primary ASI only, multiple of 48 kHz Sampling
# Playback through Stereo OUT1P and OUT2P for Headphone
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 11 80    # Enable PASI DIN
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 70    # PASI I2S, 32 bit format
w a0 28 20    # PASI DIN Ch1 on Left slot 0
w a0 29 30    # PASI DIN Ch2 on Right slot 0
w a0 64 20    # Configure OUT1P/M as differential from DAC1
w a0 65 60    # Configure OUT1P as Headphone 0dB audio band
w a0 66 60    # Configure OUT1M as Headphone 0dB audio band
w a0 6b 20    # Configure OUT2P/M as differential from DAC2
w a0 6c 60    # Configure OUT2P as Headphone 0dB audio band
w a0 6d 60    # Configure OUT2M as Headphone 0dB audio band
w a0 76 0c    # Enable output channel 1 and 2 and disable all input channels
w a0 78 40    # Power up DAC channel
```

- Target mode playback to mono single-ended headphones with PASI

This configuration is for mono single-ended audio playback (DAC) with a 48 kHz sampling rate, I2S format, and 16-bit depth.

```
##### Playback Single-Ended Headphone Path ######
# Target Mode, I2S, 16 bit
# Primary ASI only, multiple of 48 kHz Sampling
# Playback through mono OUT1P and OUT2P for Headphone
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 11 80    # Enable PASI DIN
w a0 19 00    # 1 data input and 1 data output for PASI
w a0 1a 40    # PASI I2S, 16-bit format
w a0 28 20    # PASI DIN Ch1 on Left slot 0
w a0 29 30    # PASI DIN Ch2 on Right slot 0
w a0 64 28    # Configure OUT1P as mono single-ended from DAC1
w a0 65 60    # Configure OUT1P as Headphone 0dB audio band
w a0 66 60    # Configure 2Vrms Differential
w a0 6b 28    # Configure OUT2P as mono single-ended from DAC2
w a0 6c 60    # Configure OUT2P as Headphone 0dB audio band
w a0 6d 60    # Configure 2Vrms Differential
w a0 76 0c    # Enable output channel 1 and 2 and disable all input channels
w a0 78 40    # Power up DAC channel
```

- Diagnostic setting

This configuration enables input diagnostic testing; users read the fault detection status from B0_P1_R54 for Ch 1 and B0_P1_R55 for Ch 2.

```
##### Diagnostic Setting ######
#
w a0 00 00    # Set page 0
w a0 01 01    # Software Reset
w a0 02 09    # Wake up with AVDD > 2v and all VDDIO level
w a0 50 08    # Device set to DC mode
w a0 00 01    # Set page 1
w a0 73 d0    # Set MICBIAS = 9V
w a0 46 80    # Enable IN1P and IN1M Scan for diagnostic
w a0 47 00    # Input terminal short and VBAT_In short threshold 0mV
w a0 48 12    # short to GND and to MICBIAS threshold 60mV
w a0 4a b0    # 16 counts for debounce to filter out false fault detection
w a0 4b 40    # Enable moving average with 0.5 weightage
w a0 00 00    # Set page 0
w a0 76 c0    # Enable ADC channel 1 and channel 2
w a0 78 a0    # Power up ADC and MICBIAS
```


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4 Hardware Design Files

This section provides the schematics, layout examples, and bill of materials (BOM) for each TAC541x-Q1 EVM variant.

4.1 TAC5412-Q1 EVM Schematic

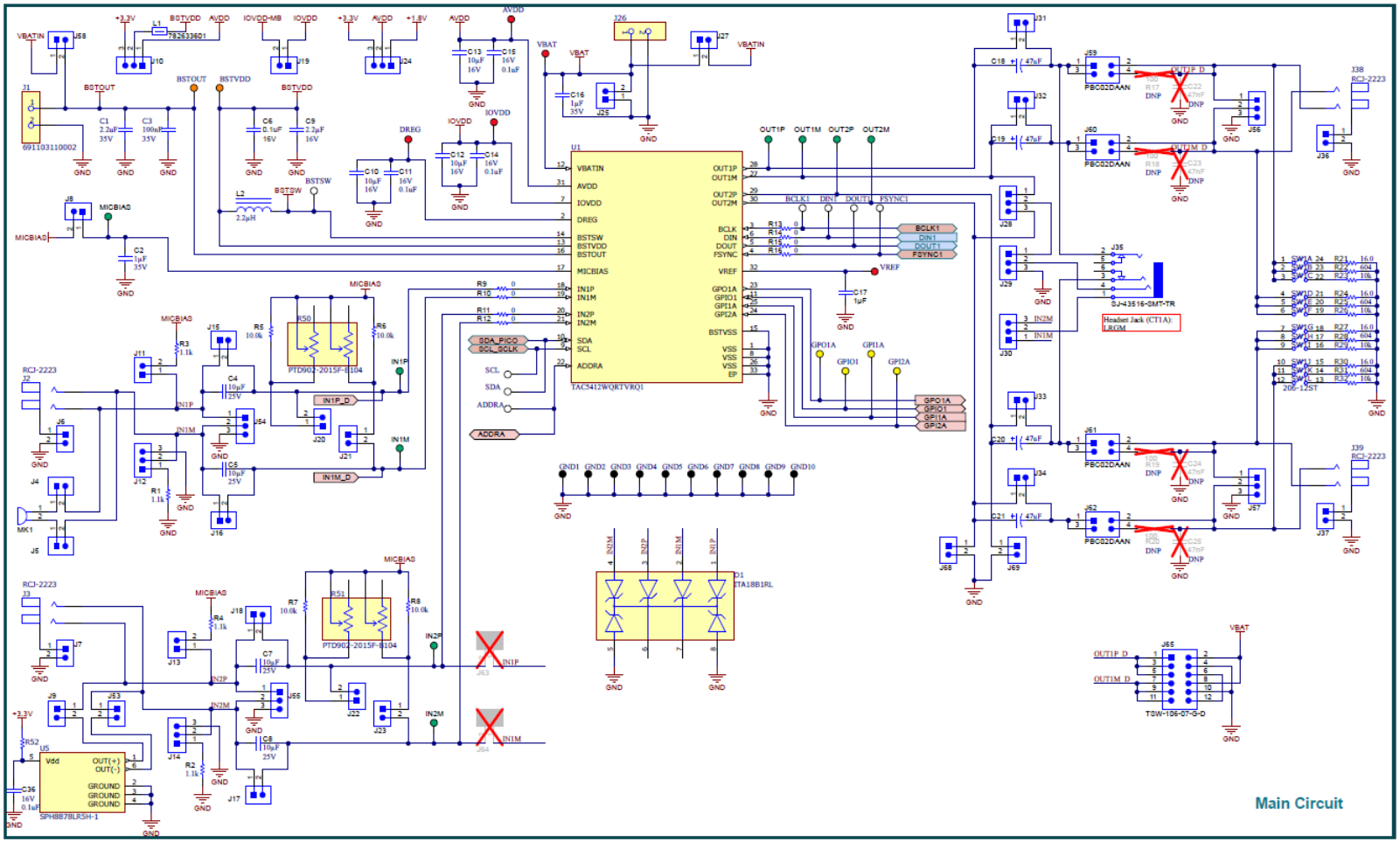

Figure 4-1. TAC5412-Q1 EVM Main DUT Schematic

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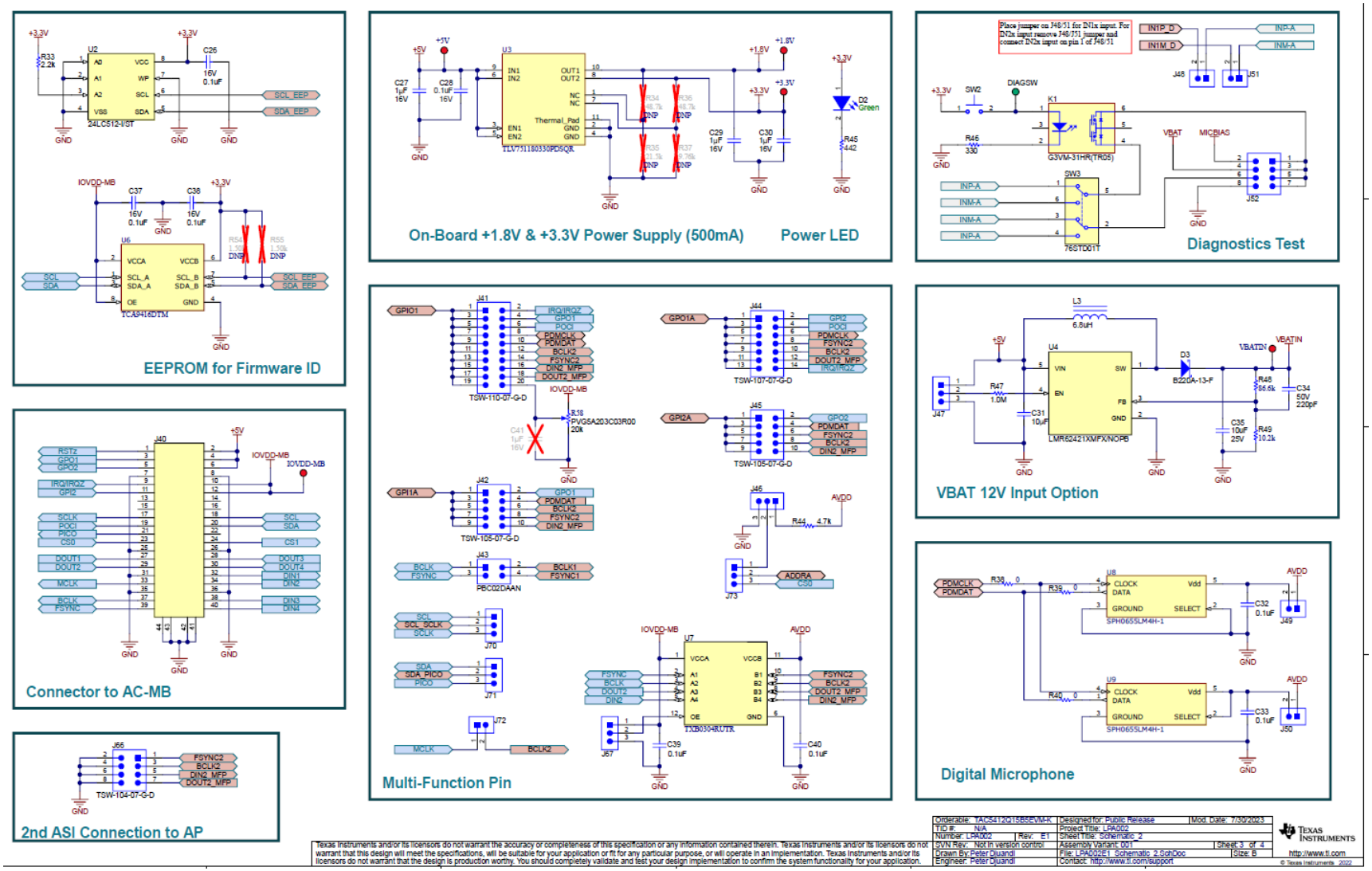

Figure 4-2. TAC5412-Q1 EVM Connectors and Supporting Circuitry Schematic

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4.2 TAC5411-Q1 EVM Schematic

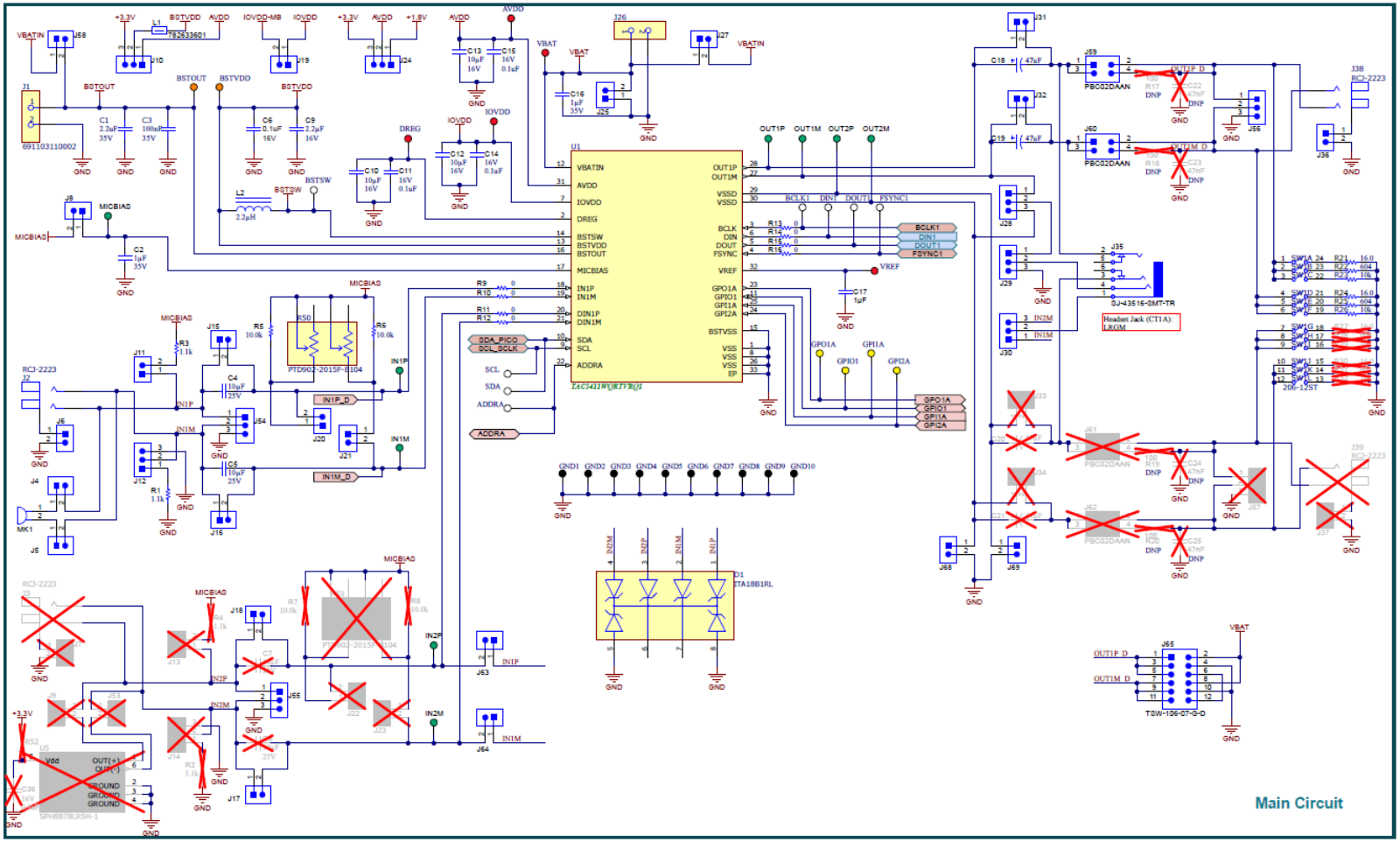

Figure 4-3. TAC5411-Q1 EVM Main DUT Schematic

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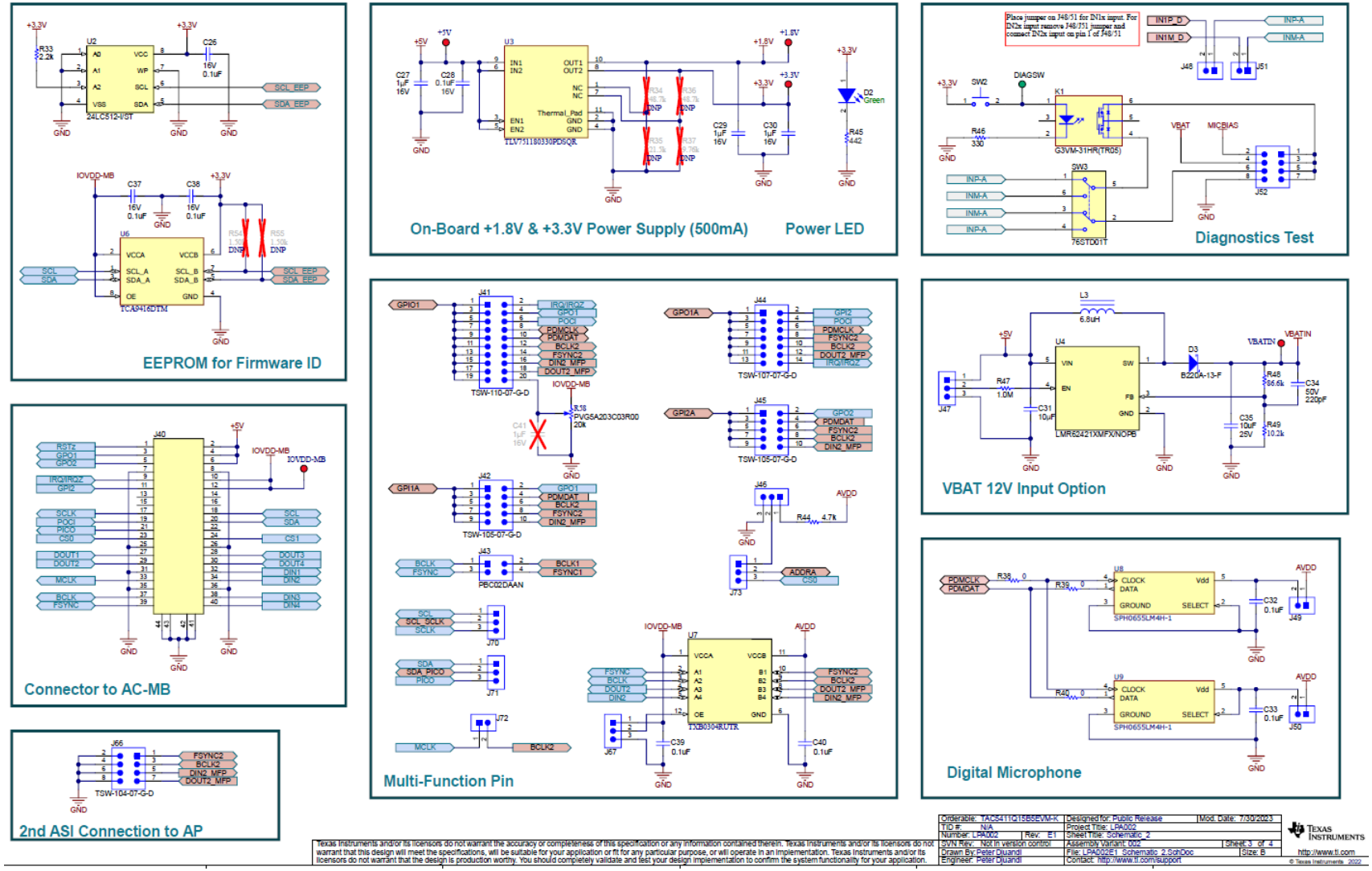

Figure 4-4. TAC5411-Q1 EVM Connectors and Supporting Circuitry Schematic

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4.3 TAC541x-Q1 EVM Board Layout

The board layout consists of the top and bottom silkscreen, the top and bottom layer routings, the power planes, the two inner layout routings, and the ground planes. The layout applies to both the TAC5412-Q1 and TAC5411-Q1 EVM.

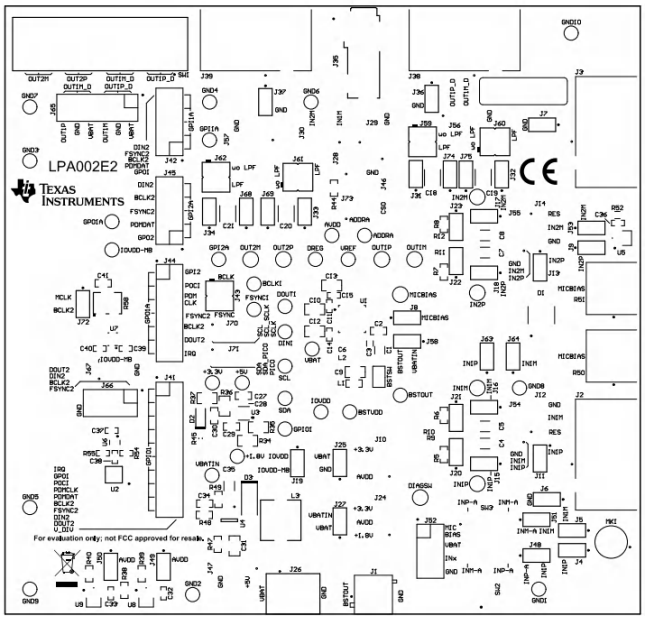

Figure 4-5. TAC541x-Q1 EVM Top Silkscreen

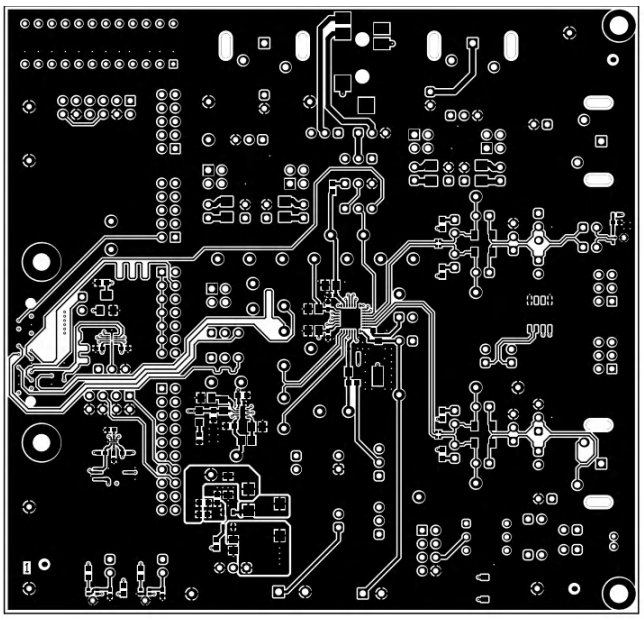

Figure 4-6. TAC541x-Q1 EVM Top Layer

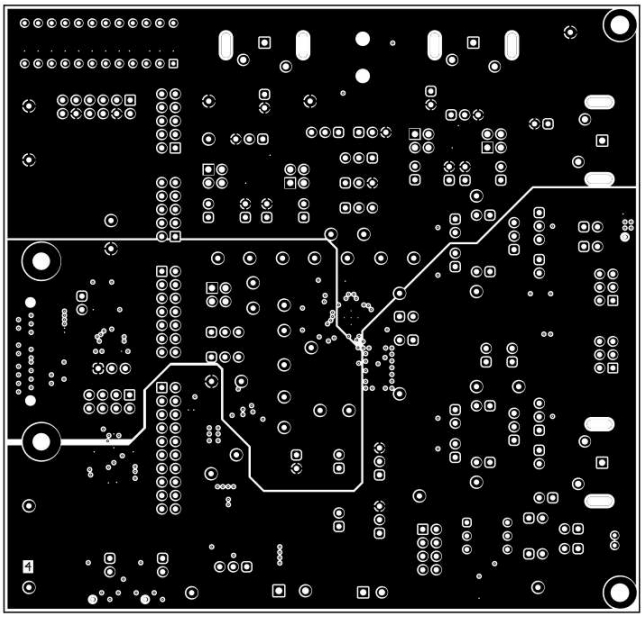

Figure 4-7. TAC541x-Q1 EVM Power Layer 1

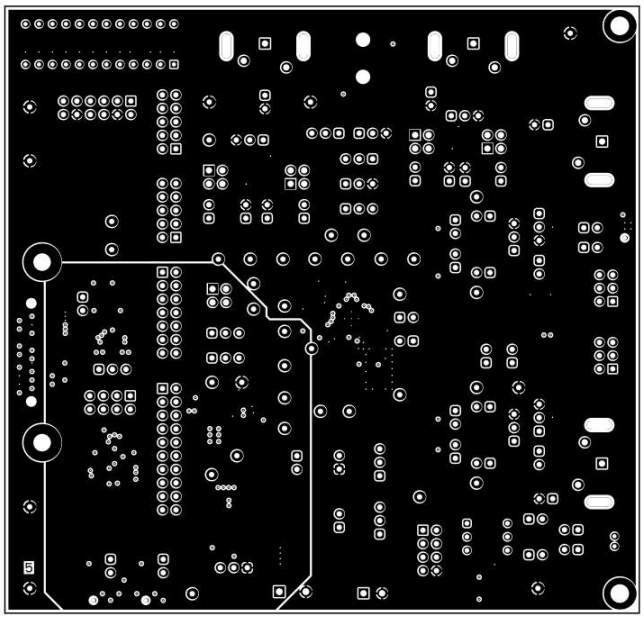

Figure 4-8. TAC541x-Q1 EVM Power Layer 2

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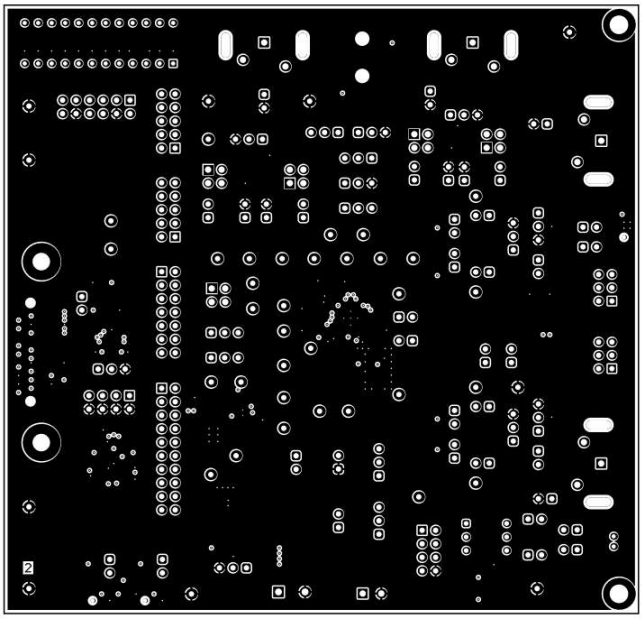

Figure 4-9. TAC541x-Q1 EVM Ground Layer 1

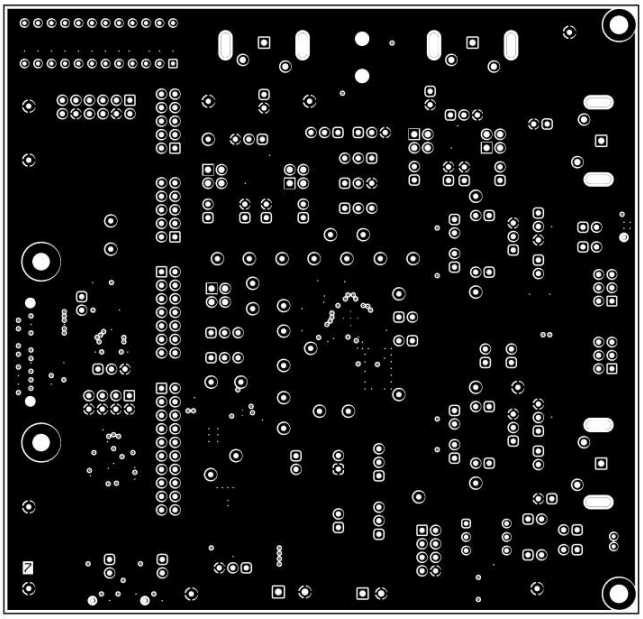

Figure 4-10. TAC541x-Q1 EVM Ground Layer 2

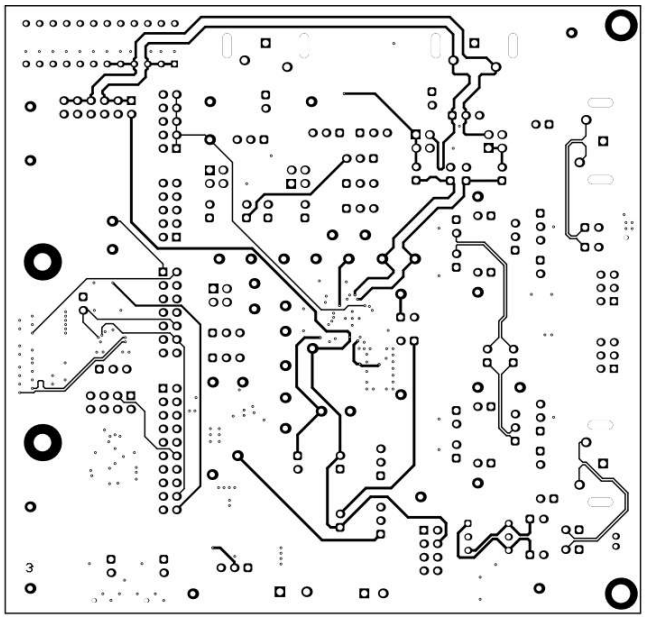

Figure 4-11. TAC541x-Q1 EVM Signal Layer 1

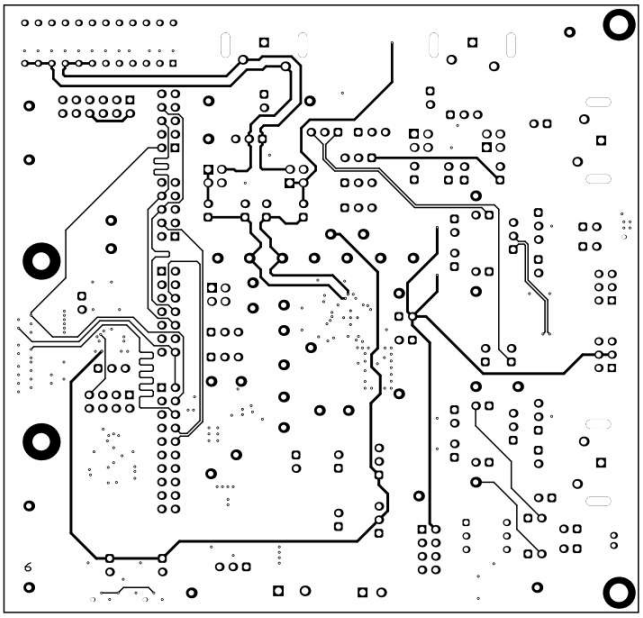

Figure 4-12. TAC541x-Q1 EVM Signal Layer 2

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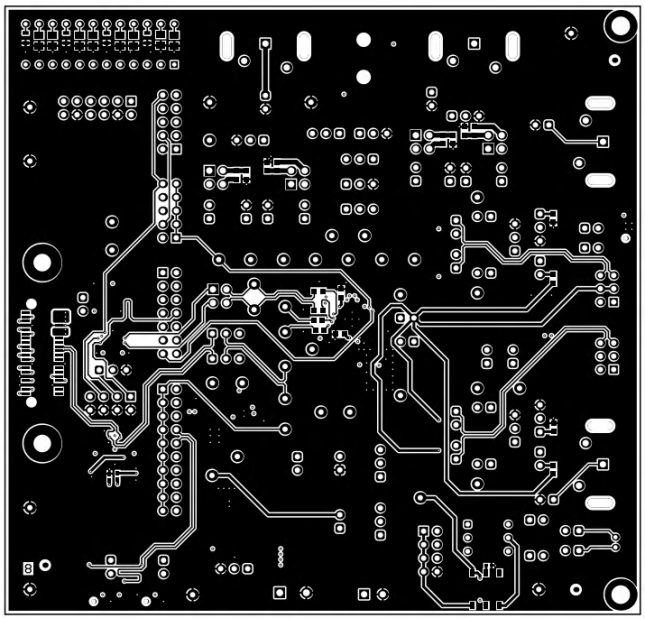

Figure 4-13. TAC541x-Q1 EVM Bottom Layer

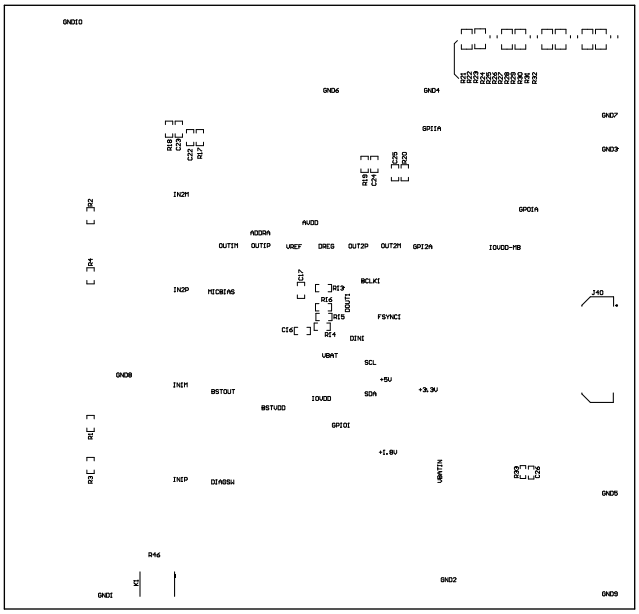

Figure 4-14. TAC541x-Q1 EVM Bottom Silkscreen

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4.4 Bill of Materials (BOM)

4.4.1 TAC5412-Q1 EVM Bill of Materials

Table 4-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LPA002	Any		
+1.8V, +3.3V, +5V, AVDD, DREG, IOVDD, IOVDD-MB, VBAT, VBATIN, VREF	10		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone Electronics		
ADDRA, BCLK1, DIN1, DOUT1, FSYNC1, SCL, SDA	7		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone Electronics		
BSTOUT, BSTVDD	2		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone Electronics		
BSTSW	1		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone Electronics		
C1	1	2.2µF	Capacitor Ceramic 2.2uF 35V X7R 10% 1206 T/R	1206	C3216X7R1V225K160AE	TDK		
C2, C16	2	1uF	CAP, CERM, 1uF, 35V, +/- 10%, X7R, 0603	0603	C1608X7R1V105K080AC	TDK		
C3	1	100nF	Cap Ceramic 100 nF 35 V X7R 10% Pad SMD 0402 +125°C Automotive T/R	0402	CGA2B3X7R1V104K050BB	TDK Corporation		
C4, C5, C7, C8	4	10uF	CAP, CERM, 10 µF, 25 V, +/- 5%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C106J3RACAUTO	Kemet		
C6, C11, C14, C15, C26, C28, C32, C33, C36, C37, C38, C39, C40	13	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	8.85012E+11	Wurth Elektronik		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C9	1	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0805	0805	C2012X7R1C225K125AB	TDK		
C10, C12, C13	3	10uF	CAP, CERM, 10 µF, 16 V,+/- 10%, X7R, 0805	0805	EMK212BB7106KG-T	Taiyo Yuden		
C17, C27, C29, C30	4	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik		
C18, C19, C20, C21	4	47uF	CAP, TA, 47 uF, 10 V, +/- 10%, 0.5 Ω, SMD	3528-21	TPSB476K010R0500	AVX		
C31	1	10uF	CAP, CERM, 10 µF, V,+/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata		
C34	1	220 pF	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C221J5GACTU	Kemet		
C35	1	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206	1206	GRM31CR71E106KA12L	MuRata		
D1	1		28 V Clamp 25 A (8/20 µs) Ipp Tvs Diode Surface Mount 8-SOIC	SOIC8	ITA18B1RL	STMicroelectronics		
D2	1	Green	LED, Green, SMD	LED_0805	LTST-C170KGKT	Lite-On		
D3	1	20 V	Diode, Schottky, 20 V, 2 A, SMA	SMA	B220A-13-F	Diodes Inc.		
DIAGSW, IN1M, IN1P, IN2M, IN2P, MICBIAS, OUT1M, OUT1P, OUT2M, OUT2P	10		Test Point, Miniature, Green, TH	Green Miniature Testpoint	5116	Keystone		
GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9, GND10	10		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone Electronics		
GPI1A, GPI2A, GPIO1, GPO1A	4		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone Electronics		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
H1, H2	2		Small nylon hex nut, 0.10 thick with a 0.250 outside diameter and a 4-40 threading	Hex Nut, 4-40 Thread, 250" Head Dia	9605	Keystone		
H3, H4	2		HEX STANDOFF 4-40 NYLON 3/4"	HEX STANDOFF 4-40 NYLON 3/4"	4804	Keystone		
J1	1			CONN_TERM_POS2	6.91103E+11	Wurth		
J2, J3, J38, J39	4		3.20 mm ID, 9.00 mm OD (RCA) Phono (RCA) Jack Mono Connector Solder	CONN_RCA_DUAL	RCJ-2223	CUI Devices		
J4, J5, J6, J7, J8, J9, J11, J13, J15, J16, J17, J18, J19, J20, J21, J22, J23, J25, J27, J31, J32, J33, J34, J36, J37, J48, J49, J50, J51, J53, J58, J68, J69, J72	34		Header, 100 mil, 2x1, Gold, TH	2 x 1 Header	TSW-102-07-G-S	Samtec		
J10, J12, J14, J24, J28, J29, J30, J46, J47, J54, J55, J56, J57, J67, J70, J71, J73	17		Header, 100 mil, 3x1, Gold, TH	3 x 1 Header	TSW-103-07-G-S	Samtec		
J26	1		TERM BLK 2POS SIDE ENTRY 5 MM PCB	HDR2	6.91138E+11	Würth Elektronik		
J35	1		AUDIO JACK 3.5 mm 4COND, SMT	AUDIO JACK 3.5 mm 4COND, SMT	SJ-43516-SMT-TR	CUI Inc.		
J40	1		Connector, Header, High Speed, 20 pairs, SMT	QTE-020-01-X-D-A	QTE-020-01-L-D-A	Samtec		
J41	1		Header, 100 mil, 10 x 2, Gold, TH	10 x 2 Header	TSW-110-07-G-D	Samtec		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J42, J45	2		Header, 100 mil, 5 x 2, Gold, TH	5 x 2 Header	TSW-105-07-G-D	Samtec		
J43, J59, J60, J61, J62	5		Header, 2.54 mm, 2 x 2, Gold, TH	Header, 2.54 mm, 2x2, TH	PBC02DAAN	Sullins Connector Solutions		
J44	1		Header, 100 mil, 7x2, Gold, TH	7 x 2 Header	TSW-107-07-G-D	Samtec		
J52, J66	2		Header, 100 mil, 4 x 2, Gold, TH	4 x 2 Header	TSW-104-07-G-D	Samtec		
J65	1		Header, 100 mil, 6 x 2, Gold, TH	6 x 2 Header	TSW-106-07-G-D	Samtec		
K1	1		Relay, SPST-NO (1 Form A), 4 A, SMD	6.3 x 4.4 mm	G3VM-31HR(TR05)	Omron Electronic Components		
L1	1	600 Ω	Ferrite Bead, 600 Ω @ 100 MHz, 1 A, 0603	0603	782633601	Wurth Elektronik		
L2	1	2.2 µH	Inductor, Shielded, Metal Composite, 2.2 µH, 2.2 A, 0.1 Ω, SMD	2 x 1.6 mm	LPWI201610H2R2T	Littelfuse		
L3	1	6.8 µH	Inductor, Shielded Drum Core, Ferrite, 6.8 µH, 2.91 A, 0.033 Ω, SMD	SMD	7447779006	Wurth Elektronik		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
MK1	1		Microphone, Condenser, Analog, Omnidirectional, -42DB, TH	6 mm DIA	POM-2242P-C33-R	PUI Audio		
R1, R2, R3, R4	4	1.1k	RES, 1.1 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K10JNEA	Vishay-Dale		
R5, R6, R7, R8	4	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603FT10K0	Stackpole Electronics Inc		
R9, R10, R11, R12	4	0	RES, 0, 5%, 0.05 W, 0201	0201	CRCW02010000Z0ED	Vishay-Dale		
R13, R14, R15, R16, R38, R39, R40	7	0	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	PMR03EZPJ000	Rohm		
R21, R24, R27, R30	4	16	RES, 16.0, 1%, 0.5 W, 0805	0805	ERJ-P06F16R0V	Panasonic		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R22, R25, R28, R31	4	604	RES, 604, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW0805604RFKEA	Vishay-Dale		
R23, R26, R29, R32	4		RES SMD 10 KΩ 5% 0.4 W 0805	0805	ESR10EZPJ103	Rohm Semiconductor		
R33	1	2.2k	RES, 2.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20JNED	Vishay-Dale		
R44	1	4.7k	RES, 4.7 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEYJ472V	Panasonic		
R45	1	442	RES, 442, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603442RFKEA	Vishay-Dale		
R46	1	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330RJNED	Vishay-Dale		
R47	1	1.0Meg	RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00JNEA	Vishay-Dale		
R48	1	86.6k	RES, 86.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060386K6FKEA	Vishay-Dale		
R49	1	10.2k	RES, 10.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K2FKEA	Vishay-Dale		
R50, R51	2	100 kΩ	Res POT Carbon Element 100 kΩ 20% 1/20 W/1/40 W PC Pins Thru-Hole	PTH_POT_9MM50_24MM65	PTD902-2015F-B104	Bourns		
R52	1	10k	10k ±5% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Moisture Resistant Thick Film	0402	RC0402JR-1310KL	Yageo		
R58	1	20k	Trimmer Potentiometer, 20 k ohm, 0.25 W, SMD	Trimmer, 4.8,3.9x5.1mm	PVG5A203C03R00	Bourns		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11, SH12, SH13, SH14, SH15, SH16, SH17, SH18, SH19, SH20, SH21, SH22, SH23, SH24, SH25, SH26, SH27, SH28, SH29, SH30, SH31, SH32, SH33, SH34, SH35, SH36, SH37, SH38, SH39, SH40, SH41, SH42, SH43, SH44, SH45, SH46, SH47, SH48, SH49, SH50, SH51, SH52, SH53, SH54, SH55, SH56, SH57, SH58, SH59, SH60	60	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
SW1	1		Dip Switch SPST 12 Position Through Hole Slide (Standard) Actuator 50 mA 24 VDC	DIP24	206-12ST	CTS		
SW2	1		Switch, Tactile, SPST-NO, 0.05 A, 12 V, SMT	Switch, 4.4x2x2.9 mm	TL1015AF160QG	E-Switch		
SW3	1		Switch, DPDT, 0.15 A, 30 VDC, TH	9.65x9.65mm	76STD01T	Grayhill		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U1	1		Libra SW Controlled High Voltage Stereo	WQFN32	TAC5412WQRTVRQ1	Texas Instruments		
U2	1		EEPROM, 512 KBIT, 400 KHZ, 8TSSOP	TSSOP-8	24LC512-I/ST	Microchip		
U3	1		500-mA, low-IQ, high-PSRR, dual-channel low-dropout (LDO) voltage regulator 10-WSON -40 to 125	WSON10	TLV751180330PDSQR	Texas Instruments		
U4	1		SIMPLE SWITCHER 2.7V to 5.5V, 2.1A Step-Up Regulator in SOT-23, DBV0005A (SOT-23-5)	DBV0005A	LMR62421XMFX/NOPB	Texas Instruments	LMR62421XMFE /NOPB	Texas Instruments
U5	1		7 Hz - 36 kHz Analog Microphone MEMS (Silicon) 2.3 V - 3.6 V Omnidirectional (-44 dB ± 0.5 dB SPL) Solder Pads	LGA	SPH8878LR5H-1	Knowles	SPH1878LR5H-C	Knowles
U6	1		TCA9416DTM X2SON8	X2SON8	TCA9416DTM	Texas Instruments		
U7	1		4-bit Bidirectional Auto-direction Sensing Translator with Fully Symmetric 0.9V to 3.6V Range, RUT0012A (UQFN-12)	RUT0012A	TXB0304RUTR	Texas Instruments		Texas Instruments
U8, U9	2		Digital, PDM Microphone MEMS (Silicon) Omnidirectional (-37 dB ± 1 dB @ 94 dB SPL) Solder Pads	SMT_MIC_2MM65_3MM50	SPH0655LM4H-1	Knowles		
C22, C23, C24, C25	0	0.047uF	CAP, CERM, 0.047 uF, 50 V, +/- 10%, X7R, 0603	0603	C1608X7R1H473K080AA	TDK		
C41	0	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J63, J64	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
R17, R18, R19, R20	0	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo		

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Table 4-1. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R34, R36	0	48.7k	RES, 48.7 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080548K7FKEA	Vishay-Dale		
R35	0	21.5k	RES, 21.5 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080521K5FKEA	Vishay-Dale		
R37	0	9.76k	RES, 9.76 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08059K76FKEA	Vishay-Dale		
R54, R55	0	1.50k	RES, 1.50 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT1K50	Stackpole Electronics Inc		

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4.4.2 TAC5411-Q1 EVM Bill of Materials

Table 4-2. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		LPA002	Any		
+1.8V, +3.3V, +5V, AVDD, DREG, IOVDD, IOVDD-MB, VBAT, VBATIN, VREF	10		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone Electronics		
ADDRA, BCLK1, DIN1, DOUT1, FSYNC1, SCL, SDA	7		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone Electronics		
BSTOUT, BSTVDD	2		Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone Electronics		
BSTSW	1		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone Electronics		
C1	1	2.2µF	Capacitor Ceramic 2.2 uF 35 V X7R 10% 1206 T/R	1206	C3216X7R1V225K160AE	TDK		
C2, C16	2	1uF	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, 0603	0603	C1608X7R1V105K080AC	TDK		
C3	1	100 nF	Cap Ceramic 100 nF 35 V X7R 10% Pad SMD 0402 +125°C Automotive T/R	0402	CGA2B3X7R1V104K050BB	TDK Corporation		
C4, C5	2	10uF	CAP, CERM, 10 µF, 25 V,+/- 5%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C106J3RACAUTO	Kemet		
C6, C11, C14, C15, C26, C28, C32, C33, C37, C38, C39, C40	12	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	8.85012E+11	Wurth Elektronik		
C9	1	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0805	0805	C2012X7R1C225K125AB	TDK		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C10, C12, C13	3	10uF	CAP, CERM, 10 µF, 16 V,+/- 10%, X7R, 0805	0805	EMK212BB7106KG-T	Taiyo Yuden		
C17, C27, C29, C30	4	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik		
C18, C19	2	47uF	CAP, TA, 47 uF, 10 V, +/- 10%, 0.5 ohm, SMD	3528-21	TPSB476K010R0500	AVX		
C31	1	10uF	CAP, CERM, 10 µF, V,+/- 10%, X7R, 0805	0805	GRM21BR71A106KA73L	MuRata		
C34	1	220 pF	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C221J5GACTU	Kemet		
C35	1	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7R, 1206	1206	GRM31CR71E106KA12L	MuRata		
D1	1		28-V Clamp 25-A (8/20µs) Ipp Tvs Diode Surface Mount 8-SOIC	SOIC8	ITA18B1RL	STMicroelectronics		
D2	1	Green	LED, Green, SMD	LED_0805	LTST-C170KGKT	Lite-On		
D3	1	20 V	Diode, Schottky, 20 V, 2 A, SMA	SMA	B220A-13-F	Diodes Inc.		
DIAGSW, IN1M, IN1P, IN2M, IN2P, MICBIAS, OUT1M, OUT1P, OUT2M, OUT2P	10		Test Point, Miniature, Green, TH	Green Miniature Testpoint	5116	Keystone		
GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, GND9, GND10	10		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone Electronics		
GPI1A, GPI2A, GPIO1, GPO1A	4		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone Electronics		
H1, H2	2		Small nylon hex nut, 0.10 thick with a 0.250 outside diameter and a 4-40 threading	Hex Nut,4-40 Thread, 250" Head Dia	9605	Keystone		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
H3, H4	2		HEX STANDOFF 4-40 NYLON 3/4"	HEX STANDOFF 4-40 NYLON 3/4"	4804	Keystone		
J1	1			CONN_TERM_POS 2	6.91103E+11	Wurth		
J2, J38	2		3.20mm ID, 9.00mm OD (RCA) Phono (RCA) Jack Mono Connector Solder	CONN_RCA_DUAL	RCJ-2223	CUI Devices		
J4, J5, J6, J8, J11, J15, J16, J17, J18, J19, J20, J21, J25, J27, J31, J32, J36, J48, J49, J50, J51, J58, J63, J64, J68, J69, J72	27		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
J10, J12, J24, J28, J29, J30, J46, J47, J54, J55, J56, J67, J70, J71, J73	15		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
J26	1		TERM BLK 2POS SIDE ENTRY 5-MM PCB	HDR2	6.91138E+11	Würth Elektronik		
J35	1		AUDIO JACK 3.5mm 4COND, SMT	AUDIO JACK 3.5mm 4COND, SMT	SJ-43516-SMT-TR	CUI Inc.		
J40	1		Connector, Header, High Speed, 20 pairs, SMT	QTE-020-01-X-D-A	QTE-020-01-L-D-A	Samtec		
J41	1		Header, 100mil, 10x2, Gold, TH	10x2 Header	TSW-110-07-G-D	Samtec		
J42, J45	2		Header, 100mil, 5x2, Gold, TH	5x2 Header	TSW-105-07-G-D	Samtec		
J43, J59, J60	3		Header, 2.54mm, 2x2, Gold, TH	Header, 2.54mm, 2x2, TH	PBC02DAAN	Sullins Connector Solutions		
J44	1		Header, 100mil, 7x2, Gold, TH	7x2 Header	TSW-107-07-G-D	Samtec		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J52, J66	2		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec		
J65	1		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec		
K1	1		Relay, SPST-NO (1 Form A), 4 A, SMD	6.3x4.4mm	G3VM-31HR(TR05)	Omron Electronic Components		
L1	1	600 ohm	Ferrite Bead, 600 ohm @ 100 MHz, 1 A, 0603	0603	782633601	Wurth Elektronik		
L2	1	2.2uH	Inductor, Shielded, Metal Composite, 2.2 µH, 2.2 A, 0.1 ohm, SMD	2x1.6mm	LPWI201610H2R2T	Littelfuse		
L3	1	6.8uH	Inductor, Shielded Drum Core, Ferrite, 6.8 uH, 2.91 A, 0.033 ohm, SMD	SMD	7447779006	Wurth Elektronik		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
MK1	1		Microphone, Condenser, Analog, Omnidirectional, -42DB, TH	6-mm DIA	POM-2242P-C33-R	PUI Audio		
R1, R3	2	1.1k	RES, 1.1 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K10JNEA	Vishay-Dale		
R5, R6	2	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603FT10K0	Stackpole Electronics Inc		
R9, R10, R11, R12	4	0	RES, 0, 5%, 0.05 W, 0201	0201	CRCW02010000Z0ED	Vishay-Dale		
R13, R14, R15, R16, R38, R39, R40	7	0	RES, 0, 0%, 0.25 W, AEC-Q200 Grade 0, 0603	0603	PMR03EZPJ000	Rohm		
R21, R24	2	16	RES, 16.0, 1%, 0.5 W, 0805	0805	ERJ-P06F16R0V	Panasonic		
R22, R25	2	604	RES, 604, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW0805604RFKEA	Vishay-Dale		
R23, R26	2		RES SMD 10K OHM 5% 0.4W 0805	0805	ESR10EZPJ103	Rohm Semiconductor		
R33	1	2.2k	RES, 2.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20JNED	Vishay-Dale		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R44	1	4.7k	RES, 4.7 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEYJ472V	Panasonic		
R45	1	442	RES, 442, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603442RFKEA	Vishay-Dale		
R46	1	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330RJNED	Vishay-Dale		
R47	1	1.0Meg	RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00JNEA	Vishay-Dale		
R48	1	86.6k	RES, 86.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060386K6FKEA	Vishay-Dale		
R49	1	10.2k	RES, 10.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K2FKEA	Vishay-Dale		
R50	1	100 kΩ	Res POT Carbon Element 100kOhm 20% 1/20W/1/40W PC Pins Thru-Hole	PTH_POT_9MM50_24MM65	PTD902-2015F-B104	Bourns		
R58	1	20k	Trimmer Potentiometer, 20 k ohm, 0.25 W, SMD	Trimmer, 4.8,3.9x5.1mm	PVG5A203C03R00	Bourns		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH1, SH2, SH3, SH4, SH5, SH6, SH7, SH8, SH9, SH10, SH11, SH12, SH13, SH14, SH15, SH16, SH26, SH27, SH28, SH29, SH30, SH31, SH32, SH33, SH41, SH42, SH43, SH44, SH45, SH46, SH47, SH48, SH49, SH50, SH51, SH52, SH53, SH54, SH55, SH56, SH57, SH58, SH59, SH60	44	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
SW1	1		Dip Switch SPST 12 Position Through Hole Slide (Standard) Actuator 50-mA 24-VDC	DIP24	206-12ST	CTS		
SW2	1		Switch, Tactile, SPST-NO, 0.05A, 12-V, SMT	Switch, 4.4x2x2.9 mm	TL1015AF160QG	E-Switch		
SW3	1		Switch, DPDT, 0.15 A, 30 VDC, TH	9.65x9.65mm	76STD01T	Grayhill		
U1	1		Libra SW Controlled High Voltage Mono	WQFN32	TAC5411WQRTVRQ1	Texas Instruments		
U2	1		EEPROM, 512-KBIT, 400-KHZ, 8TSSOP	TSSOP-8	24LC512-I/ST	Microchip		
U3	1		500-mA, low-IQ, high-PSRR, dual-channel low-dropout (LDO) voltage regulator 10-WSON -40 to 125	WSON10	TLV751180330PDSQR	Texas Instruments		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
U4	1		SIMPLE SWITCHER 2.7V to 5.5V, 2.1A Step-Up Regulator in SOT-23, DBV0005A (SOT-23-5)	DBV0005A	LMR62421XMFX/NOPB	Texas Instruments	LMR62421XMFE /NOPB	Texas Instruments
U6	1		TCA9416DTM X2SON8	X2SON8	TCA9416DTM	Texas Instruments		
U7	1		4-bit Bidirectional Auto-direction Sensing Translator with Fully Symmetric 0.9V to 3.6V Range, RUT0012A (UQFN-12)	RUT0012A	TXB0304RUTR	Texas Instruments		Texas Instruments
U8, U9	2		Digital, PDM Microphone MEMS (Silicon) Omnidirectional (-37 dB ±1 dB @ 94 dB SPL) Solder Pads	SMT_MIC_2MM65_ 3MM50	SPH0655LM4H-1	Knowles		
C7, C8	0	10uF	CAP, CERM, 10 µF, 25 V,+/- 5%, X7R, AEC-Q200 Grade 1, 1206	1206	C1206C106J3RACAUTO	Kemet		
C20, C21	0	47uF	CAP, TA, 47 uF, 10 V, +/- 10%, 0.5 ohm, SMD	3528-21	TPSB476K010R0500	AVX		
C22, C23, C24, C25	0	0.047uF	CAP, CERM, 0.047 uF, 50 V, +/- 10%, X7R, 0603	0603	C1608X7R1H473K080AA	TDK		
C36	0	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	8.85012E+11	Wurth Elektronik		
C41	0	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	8.85012E+11	Wurth Elektronik		
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J3, J39	0		3.20mm ID, 9.00mm OD (RCA) Phono (RCA) Jack Mono Connector Solder	CONN_RCA_DUAL	RCJ-2223	CUI Devices		
J7, J9, J13, J22, J23, J33, J34, J37, J53	0		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
J14, J57	0		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
J61, J62	0		Header, 2.54mm, 2x2, Gold, TH	Header, 2.54mm, 2x2, TH	PBC02DAAN	Sullins Connector Solutions		
R2, R4	0	1.1k	RES, 1.1 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K10JNEA	Vishay-Dale		
R7, R8	0	10.0k	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603FT10K0	Stackpole Electronics Inc		
R17, R18, R19, R20	0	100	RES, 100, 1%, 0.1 W, 0603	0603	RC0603FR-07100RL	Yageo		
R27, R30	0	16	RES, 16.0, 1%, 0.5 W, 0805	0805	ERJ-P06F16R0V	Panasonic		
R28, R31	0	604	RES, 604, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW0805604RFKEA	Vishay-Dale		
R29, R32	0		RES SMD 10K OHM 5% 0.4W 0805	0805	ESR10EZPJ103	Rohm Semiconductor		
R34, R36	0	48.7k	RES, 48.7 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080548K7FKEA	Vishay-Dale		
R35	0	21.5k	RES, 21.5 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080521K5FKEA	Vishay-Dale		
R37	0	9.76k	RES, 9.76 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08059K76FKEA	Vishay-Dale		
R51	0	100 kΩ	Res POT Carbon Element 100kOhm 20% 1/20W/1/40W PC Pins Thru-Hole	PTH_POT_9MM50_24MM65	PTD902-2015F-B104	Bourns		
R52	0	10k	10k ±5% 0.063W, 1/16W Chip Resistor 0402 (1005 Metric) Moisture Resistant Thick Film	0402	RC0402JR-1310KL	Yageo		
R54, R55	0	1.50k	RES, 1.50 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT1K50	Stackpole Electronics Inc		

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Table 4-2. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
SH17, SH18, SH19, SH20, SH21, SH22, SH23, SH24, SH25, SH34, SH35, SH36, SH37, SH38, SH39, SH40	0	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
U5	0		7 Hz - 36 kHz Analog Microphone MEMS (Silicon) 2.3 V - 3.6 V Omnidirectional (-44dB ± 0.5dB SPL) Solder Pads	LGA	SPH8878LR5H-1	Knowles	SPH1878LR5H-C	Knowles

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5 Additional Information

5.1 Trademarks

PurePath™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

5.2 Cable References

The following cables can be used for evaluation with external audio instruments like Audio Precision:

- BNC Male to RCA Male Cable
- RCA Speaker Cable with Banana Plugs

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (January 2024)	Page
• Updated images in *Software* section	19

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STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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