

# **ESP430CE1, ESP430CE1A, ESP430CE1B Peripheral Modules**

This document describes the ESP430CE1, ESP430CE1A, and ESP430CE1B modules. These modules incorporate the SD16, hardware multiplier, and ESP430 embedded processor engine for use in single-phase energy metering applications.

- The ESP430CE1 is implemented in the MSP430FE42x devices.
- The ESP430CE1A is implemented in the MSP430FE42xA devices.
- The ESP430CE1B is implemented in the MSP430FE42x2 devices.

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**NOTE:** The ESP430CE1B does not support current  $I_2$ .

The ESP430CE1B is functionally similar to the ESP430CE1A, except that ESP430CE1B supports only one current channel. Therefore, any references in this document to current  $I_2$  or tamper detection and their associated flags do not apply to the ESP430CE1B.

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## 1 ESP430CE1, ESP430CE1A, and ESP430CE1B Introduction

The ESP430CE1, ESP430CE1A, and ESP430CE1B modules perform energy metering calculations independent of the CPU. The modules include the SD16 module, hardware multiplier module, and the ESP430 embedded signal processor.

Features of the ESP430CE1, ESP430CE1A, and ESP430CE1B include:

- Complete analog and digital functionality for single-phase metering [2-wire and 3-wire (not available on ESP430CE1B) applications]
- Tamper detection functionality (not available on ESP430CE1B)
- Built-in calibration features and flexible user-configurable system setup
- Integrated analog front end (AFE) for voltage and current sampling
- Independently configurable analog input gain and oversampling ratio
- Software selectable internal or external voltage reference
- Built-in temperature sensor
- Integrated processing for metering calculations including active, apparent and reactive energies, power factor, line frequency, and so on.
- Direct interface to hardware multiplier module

[Figure 1](#) shows the block diagram of the ESP430CE1 and ESP430CE1A module. [Figure 2](#) shows the block diagram of the ESP430CE1B module.

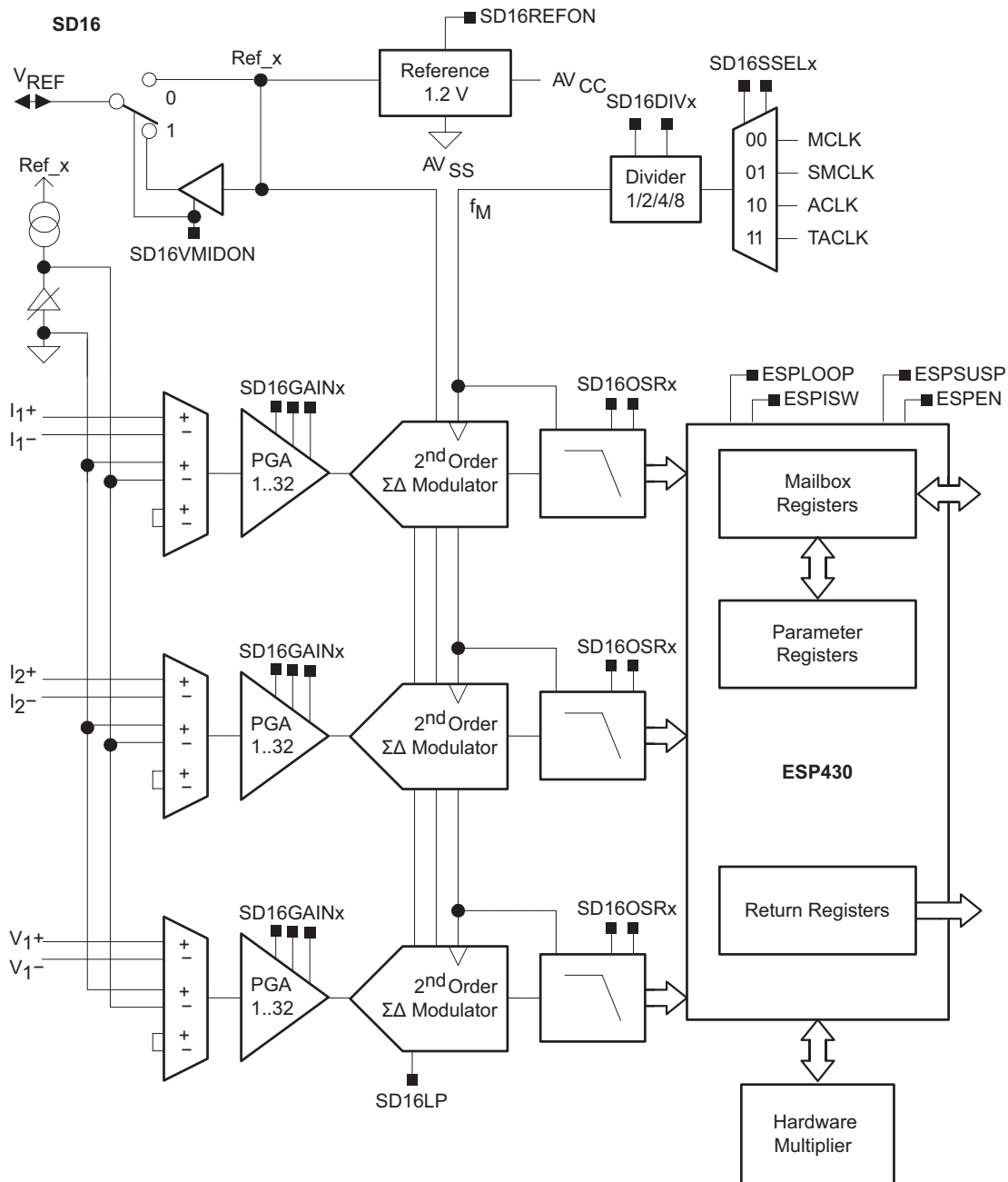


Figure 1. ESP430CE1 and ESP430CE1A Block Diagram

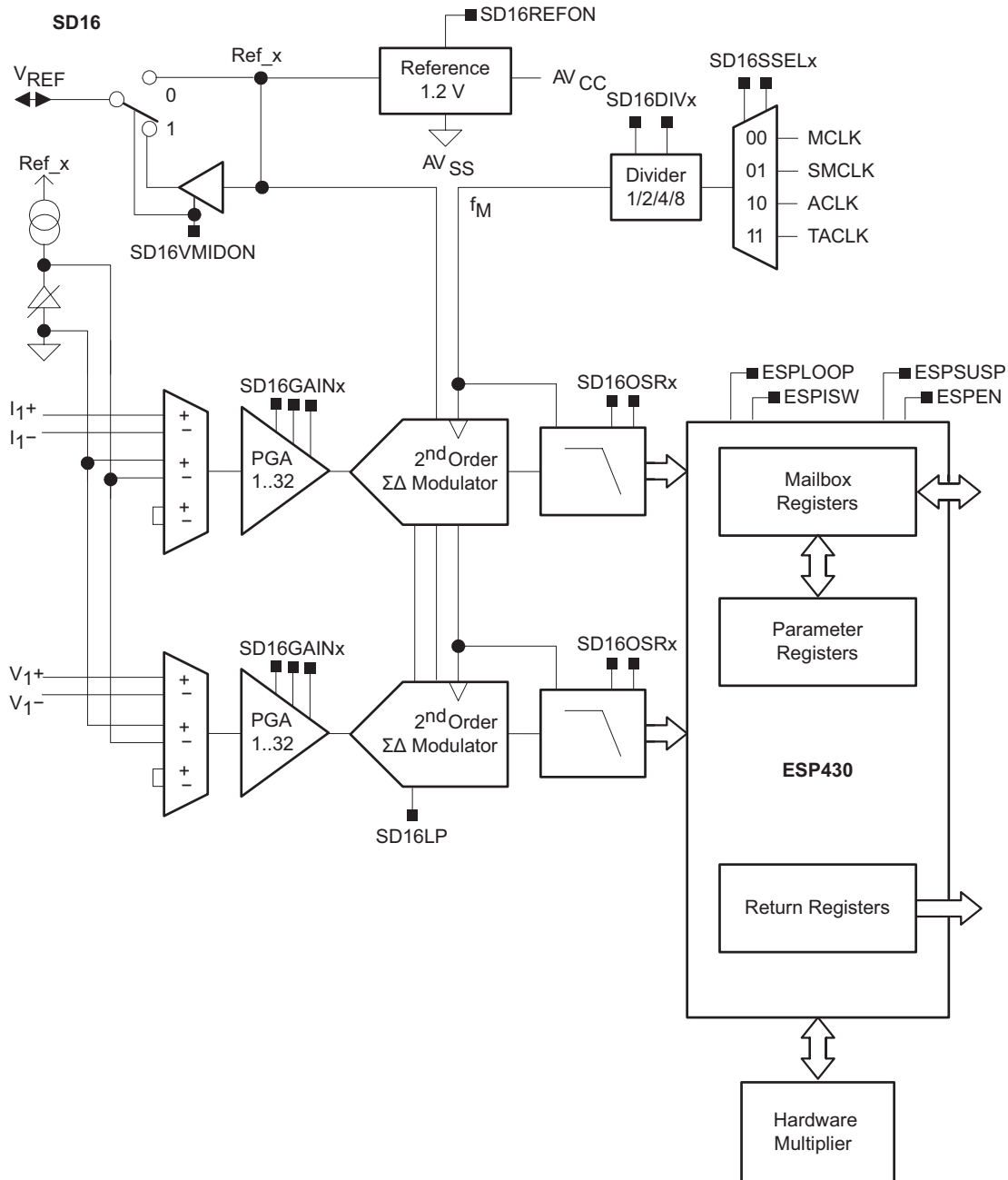


Figure 2. ESP430CE1B Block Diagram

The following are the key differences and improvements in the ESP430CE1A and ESP430CE1B in comparison to the ESP430CE1:

- Spikes on voltage  $V_1$  can disturb the measurement of the mains period leading to incorrect results that use this information. A programmable  $V_1$  filter can be used to eliminate such spikes. See [Section 2.11](#) for details.
- The reactive energy algorithm is improved and the result is signed. See [Section 2.13.5](#) for details.
- The apparent energy algorithm is improved and calculated using reactive and active energy.
- The three ADC offsets  $N_{V1SC}$ ,  $N_{I1SC}$ , and  $N_{I2SC}$  to measure  $V_1$ ,  $I_1$ , and  $I_2$ , respectively, are initialized with zero instead of measuring them with the ADC inputs shorted. See [Section 2.8.1](#) for details.
- The ADC values for the  $I_1$  and  $I_2$  samples are saturated to 7FFFh (maximum positive value) and 8000h (maximum negative value) during sample preparation (saturation).
- A watchdog function observes the zero crossing of  $V_1$ . If zero crossings are missing (for example, due to a defective resistor divider) the watchdog expires and triggers the DC removal calculations associated with a zero crossing.
- The RMS values of  $I_1$  and  $I_2$  are calculated independently of each other and are represented as 32-bit values (format +15.16).
- The RMS values of  $I_1$  and  $I_2$  are calculated using apparent power and the RMS value of  $V_1$ . See [Section 2.13.13](#) for details.
- If voltage  $V_1$  is disconnected and a supply voltage is still provided to the ESP430CE1A and ESP430CE1B, the RMS values of  $I_1$  and  $I_2$  are calculated using the root mean square of the measured current samples. This allows the CPU to calculate an energy value with a nominal voltage value for  $V_1$ .
- The calculated dc offsets for  $I_1$ ,  $I_2$ , and  $V_1$  are not cleared when the ESP430CE1A and ESP430CE1B comes out of Idle mode.
- The influence of the voltage ADC to the two current ADCs can be eliminated by a selectable hardware-specific value at address CORRCOMP. If it is zero, no common mode correction is used. Additionally, the flag I2CMRR in register ESP430\_CTRL0 can switch off the correction for current path  $I_2$ . See [Section 2.12](#) for details.
- Interrupts are generated for both positive and negative energies and are indicated by the flag ILNEGFG.

## 2 ESP430CE1, ESP430CE1A, and ESP430CE1B Operation

The ESP430CE1, ESP430CE1A, and ESP430CE1B module is configured with user software. The setup and operation of the ESP430CE1, ESP430CE1A, and ESP430CE1B are discussed in the following sections.

### 2.1 ESP430 Operation and Access

The ESP430 controls the analog sampling of the module and performs the metering calculations in parallel to CPU activity. This includes dedicated access to the SD16 and hardware multiplier modules when the ESP430 is enabled. In this case, the CPU cannot control or access the SD16 or the hardware multiplier.

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**NOTE:** Suspending the ESP430

The ESP430 can be suspended by setting ESPSUSP in ESPCTL. After ESPSUSP = 1, wait 9 MCLK cycles before the CPU accesses the SD16 or hardware multiplier modules.

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ESP430 setup, control, and access are provided by accessing data and control registers. These registers fall into three categories: control and mailbox registers, parameter registers, and return registers.

Figure 3 shows the communication links connecting each category with the ESP430 and CPU.

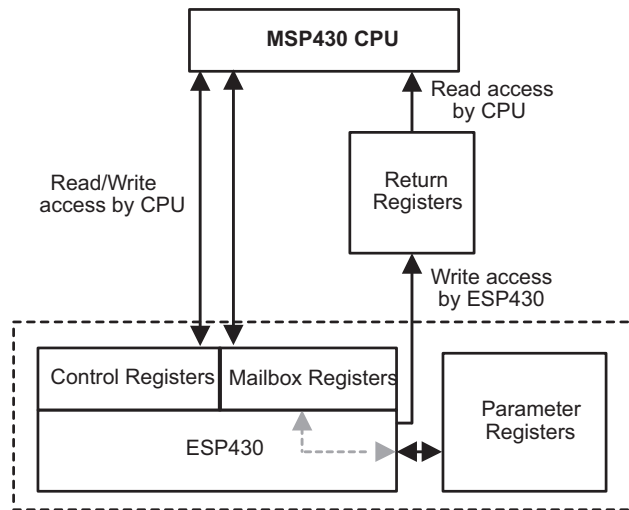


Figure 3. Module Control and Value Access Registers

The CPU controls the operation of the ESP430, which in turn controls the analog sampling and data processing of the metering analog front-end. The ESP430 also performs all parameter calculations such as active energy, apparent energy, power factor, and so on. Operation of the ESP430 is performed using the ESPCTL register.

## 2.2 ESP430 Modes of Operation

Figure 4 shows the ESP430 operating modes.

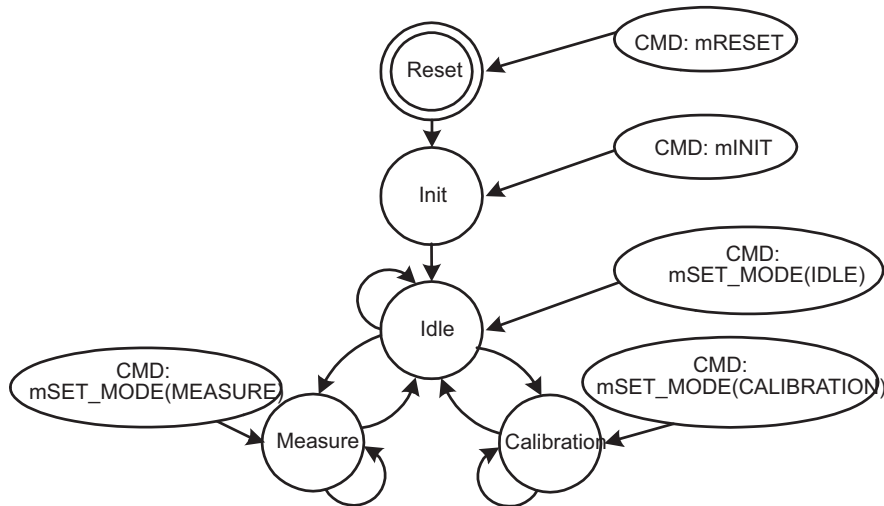


Figure 4. ESP430 Operational State Diagram

Modes are entered through commands sent by the CPU. These commands are transmitted to the ESP430 using the mailbox communication architecture. Table 1 defines these modes.

**Table 1. ESP430 Operational Mode Summary**

Mode	Command	Function
RESET	mRESET	ESP430CE1 module is reset: <ul style="list-style-type: none"> <li>Parameter registers are initialized.</li> <li>Return registers are cleared.</li> </ul> Upon completion, INIT mode is entered.
INIT	mINIT	Internal offset calibration of the AFE is performed. Offset of each SD16 channel is measured and stored using the shunted ADC input. Upon completion, the IDLE mode is entered.
IDLE	mSET_MODE (IDLE)	Operation of the ESP430 is halted. The following actions are performed in IDLE mode before halt: <ul style="list-style-type: none"> <li>Status bits in ESP430_STAT0 are cleared.</li> <li>SD16 conversions are stopped.</li> <li>ESP430 data processing is stopped.</li> </ul> IDLE mode is exited by CPU-issued command. ESP430CE1: the RAM is cleared completely. ESP430CE1A and ESP430CE1B: the RAM is cleared with the exception of the dc offset registers for $I_1$ , $I_2$ , and $V_1$ . This allows fast return to full accuracy of the ADCs.
MEASURE	mSET_MODE (MEASURE)	SD16 conversions active; all metering calculations are performed continuously and written to the return registers.
CALIBRATION	mSET_MODE (CALIBRATION)	Calibration of analog front-end and all meter parameters active. Used during production for the purpose of calibrating meter-specific performance and constants. Upon completion, IDLE mode is entered.

### 2.3 ESP430CE1, ESP430CE1A, and ESP430CE1B Mailbox Communication

The CPU communicates with the ESP430 via the mailbox register architecture. Incoming (ESP430 to CPU) and outgoing (CPU to ESP430) mailboxes are used to control the operation of the ESP430 and for access to parameter registers. Three groups of mailbox commands are implemented:

- Control Commands: Request defined action of the ESP430 (Outgoing) (see [Section 2.3.1](#))
- Parameter Commands: Modify parameter register values (Outgoing) (see [Section 2.3.3](#))
- Return Commands: Acknowledge or Notification by the ESP430 (Incoming) (see [Section 2.3.4](#))

A total of four 16-bit registers support incoming messages (MBIN0, MBIN1) and outgoing messages (MBOUT0, MBOUT1). The use of each mailbox register is described in the following sections.

#### 2.3.1 Control Commands

Mailbox control commands are sent by the CPU and define actions to be performed by the ESP430. [Table 2](#) lists the available control commands.

**Table 2. Mailbox Control Commands**

Control Command	MBOUT0 Value		MBOUT1 Value	Description
	ESP430CE1	ESP430CE1A, ESP430CE1B		
mRESET	0001h	0001h	N/A	ESP430 enters RESET mode. No acknowledge is returned to the CPU.
mSET_MODE	0003h	0003h	0:IDLE 2:CALIBRATION 4:MEASURE 6:RESET 8:INIT	ESP430 enters the specified mode. No acknowledge is returned to the CPU. RESET and INIT can also be entered by using commands mRESET and mINIT, respectively.
mCLR_EVENT	0005h	0005h	16-bit value specifying event flags to be cleared	Flags are cleared in ESP430_STAT0.
mINIT	0007h	0007h	N/A	ESP430 enters INIT mode. No acknowledge is returned to the CPU.



**Table 2. Mailbox Control Commands (continued)**

Control Command	MBOU0 Value		MBOU1 Value	Description
	ESP430CE1	ESP430CE1A, ESP430CE1B		
mTEMP	0009h	0009h	N/A	Request integrated temperature measurement. ESP430 returns mTEMPRDY in MBIN0 and conversion result in MBIN1.
mSWVERSION	000Bh	000Bh	N/A	Request ESP430 firmware version. ESP430 returns mSWRDY in MBIN0 and version value in MBIN1. The ESP430 expects the CPU to accept an immediate mail return after the mSWVERSION command is issued.
mREAD_PARAM	000Dh	000Dh	Address value of parameter register to be read. See <a href="#">Table 3</a> for a complete list of parameter registers and their address values.	Read parameter register. ESP430 returns mPARAMRDY in MBIN0 and the parameter register value in MBIN1. The ESP430 expects the CPU to accept an immediate mail return after the mREAD_PARAM command is issued.
ml2 <sup>(1)</sup>	000Fh	000Fh	N/A	Single measurement on I <sub>2</sub> channel
ml2_CONT <sup>(1)</sup>	N/A	0011h	N/A	Continuous measurement on I <sub>2</sub> channel
mLOAD_PC	0011h	0013h	Start address of called subroutine	
mSET_RES_SC	N/A	0015h	N/A	For test purposes only

<sup>(1)</sup> Not present in the ESP430CE1B

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**NOTE:** Clearing ESP430\_STAT0 Event Flags with mCLR\_EVENT

Not all flags can be reset by the CPU due to independent activity by the ESP430. These flags include I2GT11FG, ZXLDLFG, ZXTRFG, and ACTIVEFG. See the description of the individual flags for details.

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### 2.3.2 Temperature Measurement and the ESP430

A temperature measurement is triggered with the mTEMP command sent to the ESP430. With the next zero crossing of the signal on V<sub>1</sub>, an internal temperature measurement is performed. Upon completion, the mTEMPRDY command is returned in MBIN0 along with the 16-bit result in MBIN1. The temperature is calculated using the following equation.

$$T [^{\circ}\text{C}] = (\text{MBIN1}) \times \frac{V_{\text{REF}} [\text{V}] \times 1000}{65535 \times T_{\text{C}} [\text{mV/K}]} - \frac{V_{\text{OFFSET}} [\text{mV}]}{T_{\text{C}} [\text{mV/K}]} - 273 [^{\circ}\text{C}] \quad (1)$$

The parameters T<sub>C</sub> and V<sub>OFFSET</sub> refer to the temperature sensor. See the device-specific data sheet for more information.

### 2.3.3 Parameter Commands

The parameter commands are used by the CPU to access the ESP430 parameter registers. See [Section 2.8](#) for detailed description of each parameter register value. [Table 3](#) lists each parameter command. In each instance, MBOU1 contains the data value to be written to the specified parameter register and is not shown.

**Table 3. Mailbox Parameter Commands**

Parameter Command	Target Register	MBOUT0 Value Register Pointer
mSET_CTRL0	ESP430_CTRL0	0200h
mSET_CTRL1 <sup>(1)</sup>	ESP430_CTRL1	0202h
mSET_EVENT	EVENT	0204h
mSET_PHASECORR1	PHASECORR1	0206h
mSET_PHASECORR2 <sup>(2)</sup>	PHASECORR2	0208h
mSET_V1OFFSET	V1OFFSET	020Ah
mSET_I1OFFSET	I1OFFSET	020Ch
mSET_I2OFFSET <sup>(2)</sup>	I2OFFSET	020Eh
mSET_ADAPT11	ADAPT11	0210h
mSET_ADAPT12 <sup>(2)</sup>	ADAPT12	0212h
mSET_GAINCORR1	GAINCORR1	0214h
mSET_POFFSET1_LO	POFFSET1_LO	0216h
mSET_POFFSET1_HI	POFFSET1_HI	0218h
mSET_GAINCORR2 <sup>(2)</sup>	GAINCORR2	021Ah
mSET_POFFSET2_LO <sup>(2)</sup>	POFFSET2_LO	021Ch
mSET_POFFSET2_HI <sup>(2)</sup>	POFFSET2_HI	021Eh
mSET_INTRPTLEVL_LO	INTRPTLEVL_LO	0220h
mSET_INTRPTLEVL_HI	INTRPTLEVL_HI	0222h
mSET_CALCYCLCNT	CALCYCLCNT	0224h
mSET_STARTCURR_FRAC	STARTCURR_FRAC	0226h
mSET_STARTCURR_INT	STARTCURR_INT	0228h
mSET_NOMFREQ	NOMFREQ	022Ah
mSET_VDROPCYCLS	VDROPCYCLS	022Ch
mSET_RATIOTAMP <sup>(2)</sup>	RATIOTAMP	022Eh
mSET_ITAMP <sup>(2)</sup>	ITAMP	0230h
mSET_VDROPDLEVEL	VDROPDLEVEL	0232h
mSET_VPEAKLEVEL	VPEAKLEVEL	0234h
mSET_IPEAKLEVEL	IPEAKLEVEL	0236h
mSET_DCREMPER	DCREMPER	0238h
mSET_DELTAV1MAX <sup>(1)</sup>	DELTAV1MAX	023Ah
mSET_CORRCOMP <sup>(1)</sup>	CORRCOMP	023Ch
mSET_FADCU <sup>(1)</sup>	FADCU	023Eh

<sup>(1)</sup> A parameter command overwrites any existing value in the register with the new value passed in MBOUT1. The ESP430 returns the command mPARAM\_SET in MBIN0 and the requested parameter register pointer value in MBIN1 after the register is updated. Present only in the ESP430CE1A.

<sup>(2)</sup> Not present in the ESP430CE1B

### 2.3.4 Return Commands

The mailbox return commands notify the CPU that the ESP430 has completed an action or that an event has occurred. [Table 4](#) lists the ESP430 return commands. See [Section 2.3.1](#) and [Section 2.3.3](#) for more information.

**Table 4. Mailbox Return Commands**

Return Command	MBIN0 Value	MBIN1 Value	Description
mPARAM_SET	0009h	16-bit parameter register pointer value (see <a href="#">Table 3</a> )	Acknowledge a parameter register was modified and notify CPU
mPARAMRDY	0007h	16-bit parameter register data value	Acknowledge a parameter register was queried and return value to CPU
mSWRDY	0005h	ESP430 revision number	Acknowledge revision was queried and return revision number to CPU
mTEMPRDY	0003h	16-bit temperature conversion result. Acknowledge a temperature measurement was requested and return result to CPU.	
mEVENT	0001h	16-bit ESP430_STAT0 value (see <a href="#">Section 3.9</a> )	Notify CPU that an enabled event has occurred and return ESP430_STAT0 value to the CPU

## 2.4 Sampling Rate

The AFE sampling rate is the modulator input frequency divided by the oversampling ratio:  $f_{\text{ADC}} = f_{\text{M}}/\text{SD16OSRx}$ . If not otherwise noted, the sampling rate of  $f_{\text{ADC}} = 1.048576 \text{ MHz} / 256 = 4096 \text{ Hz}$  is assumed.

**NOTE:** SD16OSRx Settings

The SD16OSRx settings for each SD16 channel must be identically configured for proper ESP430 operation. Failure to assign the same oversampling rate to all SD16 channels causes erroneous ESP430 calculation results.

The number of samples for a complete ESP430 calculation sequence is 4096 and is independent of  $f_{\text{ADC}}$ . The measurement time for a complete measurement sequence is based on  $f_{\text{ADC}}$ . The sampling period is divided into 256 units to get the timebase unit for the ESP430.

$$\text{ESP430 timebase unit} = \frac{1}{f_{\text{ADC}} \times 256} \quad (2)$$

All timings are expressed with this unit, and some common values are given in [Table 5](#).

**Table 5. ESP430 Timebase and ADC Repetition Frequencies**

$f_{\text{ADC}}$	ESP430 Timebase Unit	Measurement Time	Minimum MCLK Frequency	
			ESP430CE1	ESP430CE1A, ESP430CE1B
4096 Hz	953.674 ns ( $2^{-20}$ s)	1.0 s	4.194 MHz	8.389 MHz
2048 Hz	1.907348 $\mu$ s ( $2^{-19}$ s)	2.0 s	2.097 MHz	4.194 MHz
1024 Hz	3.814697 $\mu$ s ( $2^{-18}$ s)	4.0 s	1.049 MHz	2.097 MHz

The minimum MCLK frequency for the ESP430 is dependent upon the desired ESP430 functions to be performed and  $f_{\text{ADC}}$ . [Table 6](#) shows the minimum MCLK frequency for ESP430 function combinations.

**Table 6. Minimum MCLK Frequency (SD16OSRx = 256)**

Enabled Functions	Minimum SD16DIVx	MCLK Minimum Frequency (per ADC sampling rate, $f_{ADC}$ )					
		ESP430CE1			ESP430CE1A, ESP430CE1B		
		1024 Hz	2048 Hz	4096 Hz	1024 Hz	2048 Hz	4096 Hz
Measure $I_1$	10b: /4 <sup>(1)</sup>	1.049 MHz	2.097 MHz	4.194 MHz	2.097 MHz	4.194 MHz	8.389 MHz
Measure $I_1$ and $I_2$ <sup>(2)</sup>	10b: /4 <sup>(1)</sup>	1.049 MHz	2.097 MHz	4.194 MHz	2.097 MHz	4.194 MHz	8.389 MHz
Measure $I_1$ and $I_2$ <sup>(2)</sup> , Enable DC removal function	10b: /4 <sup>(1)</sup>	1.049 MHz	2.097 MHz	4.194 MHz	2.097 MHz	4.194 MHz	8.389 MHz
Measure $I_1$ and $I_2$ <sup>(2)</sup> , Correct for DC-tolerant CTs	11b: /8	2.097 MHz	4.194 MHz	8.389 MHz	2.097 MHz	4.194 MHz	8.389 MHz
$V_1$ filter enabled		N/A	N/A	N/A	2.097 MHz	4.194 MHz	8.389 MHz
All functions enabled	11b:/8	2.097 MHz	4.194 MHz	8.389 MHz	2.097 MHz	4.194 MHz	8.389 MHz

<sup>(1)</sup> For ESP430CE1A and ESP430CE1B, divider SD16DIVx is 11b: /8.

<sup>(2)</sup> Not applicable for the ESP430CE1B

For reduced power consumption of the ESP430CE1,  $f_{ADC}$  can be reduced. This change affects the meter-specific constants, which must be modified accordingly. With a lower  $f_{ADC}$ , the MCLK frequency can be reduced with all functions remaining enabled.

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**NOTE:** SD16 Clock Source and Low Power Modes

When the CPU enters low-power modes, the clock source to the SD16 must not be disabled during ESP430 operation. Turning off the SD16 clock source halts ADC conversions, and ESP430 operation halts. User software must account for this operation when low-power modes are used

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## 2.5 Reasons for False Measurements

If the ESP430CE1, ESP430CE1A, and ESP430CE1B shows false measurements, the following causes are possible:

- The external hardware is erroneous (open and wrong connections, failures).
- The MCLK frequency of the ESP430CE1, ESP430CE1A, and ESP430CE1B is too low. See previous tables for the minimum MCLK frequencies.
- The ADC clock  $f_{ADC}$  that is in use is too high for the MCLK frequency.
- The measured values for  $V_1$ ,  $I_1$ , and  $I_2$  are  $> 7FFFh$  (+32767) or  $< 8000h$  (-32768). The ADC delivers the saturated values 7FFFh or 8000h. A hardware check is necessary.
- The values for (ADAPT11) or (ADAPT12) are too high. The multiplication with the ADC values for  $V_1$ ,  $I_1$ , and  $I_2$  deliver the saturated values 7FFFh or 8000h.
- The V1FILTER is enabled with a value too low for (DELTAV1MAX). Too many approximated  $V_1$  samples are used for the calculations.

## 2.6 ESP430 Energy Measurement Configurations

The ESP430 can operate in two different energy measurement configurations (see [Table 7](#)).

**Table 7. Measurement Configuration Summary**

Configuration	Description
Energy Measurement using $I_1$ only (2-wire or 3-wire <sup>(1)</sup> meter architecture)	Line voltage and current using $V_1$ and $I_1$ are measured. $I_2$ not used externally and is reserved for temperature measurement. Limited tamper-detection capability is available: <ul style="list-style-type: none"> <li>• Disconnection of the mains voltage</li> <li>• Reversed meter connections<sup>(1)</sup></li> </ul> $I2GT11FG$ and $TAMPFG$ always = 0
Energy Plus Tamper Detection <sup>(1)</sup> Measurement using $I_1$ and $I_2$ (2-wire meter architecture only)	Line voltage and current using $V_1$ and $I_1$ are measured. $I_2$ is used to measure neutral current enabling full tamper-detect capability: <ul style="list-style-type: none"> <li>• Disconnection of the mains voltage</li> <li>• Reversed meter connections</li> <li>• Earthing of the load</li> </ul> Temperature measurement is performed by $I_x$ channel and is automatically selected by the ESP430.

<sup>(1)</sup> Not applicable for the ESP430CE1B

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**NOTE:** Tamper Detection and ADAPT<sub>x</sub> Parameter Registers

When the energy plus tamper-detection configuration is used, it is necessary to adapt the meter constants  $C_{z1}$  and  $C_{z2}$  using parameter registers ADAPT1 and ADAPT2. See the specific parameter register descriptions for more information.

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### 2.6.1 Disconnection of the Mains Voltage

This condition occurs when voltage connections of the electricity meter are removed. With a coil around the current path providing a supply voltage to the MSP430, basic meter functionality can continue. The CPU must sample the current channel using the SD16 directly and perform the required calculations to continue accumulating energy. The missing voltage value can be replaced by the highest specified mains voltage for the system. The ESP430 should be disabled to minimize current consumption.

### 2.6.2 Reversed Meter Connections

This condition occurs when either the voltage or the current connections of the electricity meter – but not both – are reversed. It is indicated when ACTENERGY1 contains a negative energy value. The CPU must define the treatment of negative active energy values calculated by the ESP430 and take appropriate action when negative active energy is encountered. The treatment of negative active energy by the ESP430 is defined by NE1 and NE0 in ESP430\_CTRL0 and is defined in [Table 8](#).

**Table 8. ESP430 Treatment of Negative Active Energy**

NE1	NE0	ESP430 Action
0	0	Energy not summed, active energy is set to zero, NEGENFG = 1
0	1	Absolute active energy is summed, NEGENFG = 1
1	0	Negative active energy is summed, NEGENFG = 1 return register POWERFCT is negative.
1	1	Reserved. Defaults to NE1 = 1, NE0 = 0.

### 2.6.3 Earthing of the Load

This condition occurs when the load is not connected to the neutral return but to an earth ground connection. This is potentially the case when  $I_1$  has a significantly larger value than  $I_2$  (or vice-versa) and depends on the electricity meter circuitry. The CPU must use the provided energy values and take appropriate action.

### 2.6.4 Comparison of Two Currents (Not Applicable for the ESP430CE1B)

Fundamental operation of the complete tamper-detection features of the ESP430 requires a comparison of currents on both  $I_1$  and  $I_2$ . The ESP430 measures the meter current at  $I_1$  and  $I_2$  when both channels are used, and the larger of the two RMS values is used for all calculations.

I2GTI1FG in return register ESP430\_STAT0 indicates the channel measuring the greater current:

- I2GTI1FG = 0:  $I_1 \geq I_2$ . Current  $I_1$  is used
- I2GTI1FG = 1:  $I_1 < I_2$ . Current  $I_2$  is used

TAMPFG in return register ESP430\_STAT0 indicates if tampering (defined by parameter register RATIOTAMP) occurred during the last measurement period (4096 samples). RATIOTAMP defines the percentage difference between both  $I_x$  channels allowed before a possible tampering condition is indicated (0% to 100%:  $1.0 \leq (\text{RATIOTAMP}) \times 2^{-14} < 2.0$ ).

TAMPFG = 0: No tampering detected

- I2GTI1FG = 0:  $I_1 < I_2 \times (\text{RATIOTAMP}) \times 2^{-14}$
- I2GTI1FG = 1:  $I_2 < I_1 \times (\text{RATIOTAMP}) \times 2^{-14}$

TAMPFG = 1: Possible tampering condition

- I2GTI1FG = 0:  $I_1 \geq I_2 \times (\text{RATIOTAMP}) \times 2^{-14}$
- I2GTI1FG = 1:  $I_2 \geq I_1 \times (\text{RATIOTAMP}) \times 2^{-14}$

The tampering check threshold for each channel is defined by the ITAMP parameter register. If the RMS values of  $I_1$  and  $I_2$  are lower than the tamper threshold current provided, the tampering check calculations are not performed and TAMPFG = 0.

### 2.7 Meter Constants and the ESP430

The ESP430 processes AFE conversion data and calculates the return register results. With user software, the CPU calculates meter-specific values for voltage, current, energy, power, and so on, from the relative values provided by the ESP430. To calculate the meter-specific values from the relative values provided by the ESP430, meter constants must be defined.

The meter constant  $C_z$  is given by:

$$C_z = \frac{f_{\text{ADC}}}{k_v \times k_i \times 4096} \left[ \frac{\text{steps}^2}{\text{Ws}} \right] \quad (3)$$

When  $f_{\text{ADC}} = 4096$  Hz this simplifies to:

$$C_z = \frac{1}{k_v \times k_i \times 1\text{sec}} \left[ \frac{\text{steps}^2}{\text{Ws}} \right] \quad (4)$$

The variables  $k_v$  and  $k_i$  represent the meter-specific constants used by the CPU to calculate actual voltages and currents from the values of the return registers. Different constants can exist for each current path and are differentiated by a 1 or 2 for  $I_1$  and  $I_2$ , respectively, where appropriate. Return value equations used by the ESP430 and meter-specific relationships used by the CPU are described in the following sections.

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**NOTE:** Equations and ESP430 Registers

Throughout this document, equation variables enclosed in “( )” refer to values contained in ESP430 Parameter or return registers.

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## 2.8 ESP430CE1 Parameter Register Description

The parameter registers contain information provided by the CPU that controls how the ESP430 processes the current and voltage sample data.

The parameter registers are located within the ESP430 and are accessed using the mailbox communication registers. The following section describes each parameter register.

### 2.8.1 ESP430\_CTRL0: ESP430 Control Register 0

The ESP430\_CTRL0 register controls the calculation functionality of the ESP430 and is described in [Table 9](#).

**Table 9. ESP430\_CTRL0 Summary**

Name	Bit Function
CURR_I2 <sup>(1)</sup>	<p>CURR_I2 enables the external use of analog channel I<sub>2</sub>.</p> <ul style="list-style-type: none"> <li>CURR_I2 = 0: I<sub>2</sub> is disabled and not used externally.</li> <li>CURR_I2 = 1: I<sub>2</sub> accepts a connection to a current transformer (CT), DC-tolerant CT or shunt sensor for tamper detection operation.</li> </ul>
CURR_I1	<p>CURR_I1 enables the external use of analog channel I<sub>1</sub>.</p> <ul style="list-style-type: none"> <li>CURR_I1 = 0: I<sub>1</sub> accepts a connection to a CT, DC-tolerant CT or shunt sensor for measurement of the line current.</li> <li>CURR_I1 = 1: Reserved</li> </ul>
MB	<p>MB defines the operation ILREACHEDFG indicating that an interrupt level has been reached specified in the INTRPTLEVL parameter register.</p> <ul style="list-style-type: none"> <li>MB = 0: ILREACHEDFG is set after a defined accumulated energy level has been reached specified by INTRPTLEVL. The value in INTRPTLEVL is subtracted from the ESP430 energy sum and accumulation of energy continues.</li> <li>MB = 1: ILREACHEDFG is set after a defined number of measurements has been completed specified by INTRPTLEVL. The ESP430 internal measurement counter is cleared and counting resumes from 0.</li> </ul>
NE0	NE <sub>x</sub> bits define the ESP430 handling of a negative active energy result. Refer to <a href="#">Table 8</a> for
NE1	additional information.
DCREM_V1	<p>DCREM<sub>xx</sub> enables the ESP430 DC removal functionality for measurements made on the respective AFE channel: V<sub>1</sub>, I<sub>1</sub>, or I<sub>2</sub>.</p> <ul style="list-style-type: none"> <li>DCREM<sub>xx</sub> = 0: the removal function is disabled. ADC conversion values are corrected using the offset correction value obtained for the specific AFE channel during the INIT mode of the ESP430 startup operation.</li> <li>DCREM<sub>xx</sub> = 1: the removal function is enabled. ADC conversion values are corrected using the DC removal function.</li> </ul>
DCREM_I1	
DCREM_I2 <sup>(1)</sup>	
V1FILTER	The V1FILTER bit (bit 8) switches the spike filter function for the voltage V <sub>1</sub> . Implemented with the ESP430CE1A and ESP430CE1B only.
I2CMRR <sup>(1)</sup>	The CMRR enable bit (bit 9) switches the common mode rejection function for the current I <sub>2</sub> . Implemented with the ESP430CE1A only.

<sup>(1)</sup> Not present in the ESP430CE1B

---

#### NOTE: Enabling DC Removal for Multiple AFE Channels

It is not necessary to enable dc removal for all channels, and removal must be enabled only for the voltage path or the current path. When both I<sub>1</sub> and I<sub>2</sub> are used, and dc removal is required in the current path, the dc removal function can be enabled for both current channels as required by the measurement configuration.

---



### 2.8.2 DC Removal Bit for $V_1$ – DCREM\_V1

The DCREM\_V1 bit (bit 5) switches the dc removal function for the voltage  $V_1$ . For a description of dc removal, see [Section 2.8.24](#).

#### ESP430CE1

DCREM\_V1 = 0: The dc removal function for  $V_1$  is switched off, the ADC offset  $N_{V1SC}$  measured with shorted ADC inputs for  $V_1$  is used instead.

DCREM\_V1 = 1: The dc removal function for  $V_1$  is switched on.

#### ESP430CE1A and ESP430CE1B

DCREM\_V1 = 0: The dc removal function for  $V_1$  is switched off, an ADC offset 0 is used instead.

DCREM\_V1 = 1: The dc removal function for  $V_1$  is switched on.

### 2.8.3 DC Removal Bit for $I_1$ – DCREM\_I1

The DCREM\_I1 bit (bit 6) switches the dc removal function for the current  $I_1$ .

#### ESP430CE1

DCREM\_I1 = 0: The dc removal function for  $I_1$  is switched off, the ADC offset  $N_{I1SC}$  measured with shorted ADC inputs for  $I_1$  is used instead.

DCREM\_I1 = 1: The dc removal function for  $I_1$  is switched on. If a Rogowski coil is used (CURR\_I1 = 1), the dc removal for the  $\Delta i/\Delta t$  integrator is enabled, too.

#### ESP430CE1A and ESP430CE1B

DCREM\_I1 = 0: The dc removal function for  $I_1$  is switched off, an ADC offset 0 is used instead.

DCREM\_I1 = 1: The dc removal function for  $I_1$  is switched on.

### 2.8.4 DC Removal Bit for $I_2$ – DCREM\_I2

The DCREM\_I2 bit (bit 7) switches the dc removal function for the current  $I_2$ .

#### ESP430CE1

DCREM\_I2 = 0: The dc removal function for  $I_2$  is switched off, the ADC offset  $N_{I2SC}$  measured with shorted ADC inputs for  $I_2$  is used instead.

DCREM\_I2 = 1: The dc removal function for  $I_2$  is switched on.

#### ESP430CE1A

DCREM\_I2 = 0: The dc removal function for  $I_2$  is switched off, an ADC offset 0 is used instead.

DCREM\_I2 = 1: The dc removal function for  $I_2$  is switched on.

#### ESP430CE1B

Not present

### 2.8.5 Spike Filter Enable Bit for $V_1$ – V1FILTER

The V1FILTER bit (bit 8) switches the spike filter function for the voltage  $V_1$ . Implemented with the ESP430CE1A and ESP430CE1B only.

V1FILTER = 0: No filter function. The  $V_1$  input samples are not checked.

V1FILTER = 1: The spike filter function for  $V_1$  is enabled. The absolute value of the difference  $|N_{V1n} - N_{V1n-1}|$  is compared to the value contained in word DELTAV1MAX. If the absolute value of this difference is smaller, the original  $V_1$  sample is used. If the difference is larger or equal, a linear approximation of the two previous  $V_1$  values ( $N_{V1n-1}$ ,  $N_{V1n-2}$ ) is used instead for  $N_{V1n}$ . See [Section 2.11](#) for details.



## 2.8.6 CMRR Enable Bit for $I_2$ – I2CMRR

The CMRR Enable bit (bit 9) switches the common mode rejection function for the current  $I_2$ . Implemented with the ESP430CE1A only.

I2CMRR = 0: No common-mode rejection function for  $I_2$ . This allows the use of current sensors with relatively high output voltages like current transformers.

I2CMRR = 1: The common-mode rejection function for  $I_2$  is enabled, if the value in parameter register CORRCOMP > 0. See [Section 2.12](#) for details.

## 2.8.7 EVENT: Event Message Enable Control Register

The message enable bits in EVENT enable a mEVENT mailbox message return command to be sent by the ESP430 to the CPU when the corresponding event occurs. An event is the setting of a previously cleared bit in the ESP430\_STAT0 register. A static level of a flag in ESP430\_STAT0 or resetting of a flag not previously cleared does not generate an event. The event flags in ESP430\_STAT0 are set independently of the message enable settings.

## 2.8.8 PHASECORRx: $I_x$ Phase Correction

PHASECORRx defines the phase correction for  $I_x$  where  $x = 1$  or  $2$  for channels  $I_1$  and  $I_2$ , respectively. The value specified is used for phase error correction of a simple or DC tolerant current transformer on  $I_x$ . If this value is nonzero, the correction calculations are made during the measurement process. If a shunt is used on  $I_x$ , set PHASECORRx = 0.

- PHASECORRx > 0:  $I_x$  leads  $V_1$  (capacitive characteristic of DC tolerant CTs)
- PHASECORRx < 0:  $I_x$  lags  $V_1$  (inductive characteristic of simple CTs)

Format	Signed integer	±15.0
Range	0x8000 to 0x7FFF	–31.25 ms to +31.2490 ms ( $f_{\text{MAINS}} = 50 \text{ Hz}$ , $f_{\text{ADC}} = 4096 \text{ Hz}$ )
Normal Range	–2° to +8°: 0xFF8C to 0x01D2 ( $f_{\text{MAINS}} = 50 \text{ Hz}$ , $f_{\text{ADC}} = 4096 \text{ Hz}$ )	–111 μs to +444 μs ( $f_{\text{MAINS}} = 50 \text{ Hz}$ , $f_{\text{ADC}} = 4096 \text{ Hz}$ )
Resolution	ESP430 timebase unit	2 to 20 s ( $f_{\text{ADC}} = 4096 \text{ Hz}$ )
Initialization	0x00	

### Formulas

$$(\text{PHASECORRx}) = \frac{\varphi_{\text{CT}}}{360^\circ \times f_{\text{MAINS}(\text{nom})}} \times \frac{1}{\text{ESP430 Timebase Unit}} \quad (5)$$

### Example

The phase error,  $\varphi_{\text{CT}}$ , of a DC tolerant current transformer on  $I_1$  is specified to be +4.2° at 50 Hz;  $f_{\text{ADC}} = 4096 \text{ Hz}$ . The rounded value calculated for PHASECORR1 is:

$$(\text{PHASECORR1}) = \frac{4.2^\circ}{360^\circ \times 50\text{Hz}} \times \frac{1}{2^{-20}} = 244.667 \approx 0xF5 \quad (6)$$

### Example

A simple current transformer on  $I_1$  has an inductive phase error of –1° at 50 Hz;  $f_{\text{ADC}} = 4096 \text{ Hz}$ . The rounded value in PHASECORR1 is:

$$(\text{PHASECORR1}) = \frac{-1.0^\circ}{360^\circ \times 50\text{Hz}} \times \frac{1}{2^{-20}} = -58.254 \approx 0xFFC6 \quad (7)$$

### 2.8.9 V1OFFSET: V<sub>1</sub> Offset Correction

V1OFFSET defines the ADC offset correction for V<sub>1</sub>. The value specified is added to the ADC result to measure 0 when 0 V is applied externally.

Format	Signed integer	±15.0
Range	0x8000 to 0x7FFF	-32768 to +32767
Normal Range	0xFE00 to 0x0200	±512
Resolution	1 step	
Initialization	0x00	

#### Formulas

$$(\text{WAVEFSV1}) = N_{V1\text{ADC}} - N_{V1\text{SC}} + (\text{V1OFFSET}) \quad (8)$$

Where:

$N_{V1\text{ADC}}$  = Conversion value from SD16

$N_{V1\text{SC}}$  = ESP430-corrected offset value

$N_{V1\text{SC}}$  represents two different values dependent on DCREM\_V1:

DCREM\_V1 = 0:  $N_{V1\text{SC}}$  is the offset measured during the INIT mode of the ESP430 startup (internally shorted ADC input result).

DCREM\_V1 = 1:  $N_{V1\text{SC}}$  is the offset resulting from the ESP430 DC removal calculation for V<sub>1</sub>. V1OFFSET is not used and should be set to 0.

### 2.8.10 IxOFFSET: I<sub>x</sub> Offset Correction

IxOFFSET defines the ADC offset correction for I<sub>x</sub> where x = 1 or 2 for channels I<sub>1</sub> and I<sub>2</sub>, respectively. The value specified is added to the ADC result to measure when 0A is applied to the shunt or CT externally for the respective I<sub>x</sub> channel.

Format	Signed integer	±15.0
Range	0x8000 to 0x7FFF	-32768 to +32767
Normal Range	0xFE00 to 0x0200	±512
Resolution	1 step	
Initialization	0x00	

#### Formulas

$$(\text{WAVEFSIx}) = (N_{Ix\text{ADC}} - N_{Ix\text{SC}} + (\text{IxOFFSET})) \times (\text{ADAPTIx}) \times 2^{-14} \quad (9)$$

Where:

$N_{Ix\text{ADC}}$  = Conversion value from SD16

$N_{Ix\text{SC}}$  = ESP430-corrected offset value

$N_{Ix\text{SC}}$  represents two different values dependent on DCREM\_Ix:

DCREM\_Ix = 0:  $N_{Ix\text{SC}}$  is the offset measured during the INIT mode of the ESP430 startup (internally shorted ADC input result).

DCREM\_Ix = 1:  $N_{Ix\text{SC}}$  is the offset resulting from the ESP430 DC removal calculation for I<sub>x</sub>. IxOFFSET is not used and should be set to 0.

### 2.8.11 ADAPT<sub>I<sub>x</sub></sub>: I<sub>x</sub> Adaptation Current

ADAPT<sub>I<sub>x</sub></sub> defines the multiplication factor for the adaptation of the I<sub>x</sub> ADC result. This parameter is used to provide equal current constants k<sub>11</sub> and k<sub>12</sub> (and therefore equal meter constants C<sub>Z1</sub> and C<sub>Z2</sub>) for the currents I<sub>1</sub> and I<sub>2</sub> despite possible hardware implementation differences. To assure that the meter constants can be adapted, I<sub>1</sub> and I<sub>2</sub> should be matched as close as possible using the AFE gain settings.

Format	unsigned Integer.Fraction	+1.14
Range	0x00 to 0x7FFF	0.0 to 1.999938965
Normal Range	0x2000 to 0x7FFF	0.5 to 1.999938965
Resolution	61.035x10 <sup>-6</sup>	2 <sup>-14</sup>
Initialization	0x4000	1.000

#### Formulas

$$(\text{ADAPT}_{I_x}) = \frac{k_{I_x}}{k_{I_{\text{com}}}} \times 2^{14} \quad (10)$$

Where:

k<sub>I<sub>x</sub></sub> = I<sub>x</sub> meter constant

k<sub>I<sub>com</sub></sub> = Common meter constant

#### Example

The I<sub>1</sub> meter constant should be modified to k<sub>I<sub>com</sub></sub> = 2.5x10<sup>-3</sup> from the actual meter constant k<sub>11</sub> = 2.21946x10<sup>-3</sup>. The rounded value required in ADAPT<sub>I1</sub> is:

$$\begin{aligned}
 (\text{ADAPT}_{I1}) &= \frac{k_{I1}}{k_{I_{\text{com}}}} \times 2^{14} = \frac{2.21946 \times 10^{-3}}{2.5 \times 10^{-3}} \times 2^{14} = 0.887784 \times 2^{14} = \\
 &= 14,545.45306 \approx 0x38D1 \quad (11)
 \end{aligned}$$

---

#### NOTE: ADAPT<sub>I<sub>x</sub></sub> Minimum Values

The I<sub>1</sub> ADC result WAVEFS1 is corrected with the offset correction value I1OFFSET, the offset value N<sub>I<sub>1</sub>ISC</sub>, which depends on DCREM\_I1, and the value in ADAPT<sub>I1</sub>. It is recommended that ADAPT<sub>I1</sub> × 2<sup>-14</sup> ≥ 1. Results less than 1 can degrade calculation accuracy. This also applies to ADAPT<sub>I2</sub>.

---

### 2.8.12 GAINCORRx: I<sub>x</sub> Gain Correction

GAINCORRx defines the slope for the correction of the product WAVEFSV1 × WAVEFSIx, where x = 1 or 2 for channel I<sub>1</sub> or I<sub>2</sub>, respectively. Before internally summing the new value, the product of the new voltage and current samples is corrected with GAINCORRx and POFFSETx. See [Section 2.14](#) for more information.

Format	Unsigned Integer.Fraction	1.14
Range	0x00 to 0x7FFF	0.0 to 1.999938965
Normal Range	0x3999 to 0x4666	1 ±10%
Resolution	61.035x10 <sup>-6</sup>	2 <sup>-14</sup>
Initialization	0x4000	1

#### Formulas

$$(\text{GAINCORRx}) = \text{slope} \times 2^{14} = \frac{n_{\text{Hlcalc}} - n_{\text{LOcalc}}}{n_{\text{Hlmeas}} - n_{\text{LOmeas}}} \times 2^{14} \quad (12)$$

Where:

$n_{\text{Hlcalc}}$  = Calculated result at the high current calibration point [steps<sup>2</sup>]

$n_{\text{Hlmeas}}$  = Measured result at the high current calibration point [steps<sup>2</sup>]

$n_{\text{LOcalc}}$  = Calculated result at the low current calibration point [steps<sup>2</sup>]

$n_{\text{LOmeas}}$  = Measured result at the low current calibration point [steps<sup>2</sup>]

$n_{\text{LOcalc}}$  and  $n_{\text{LOmeas}}$  are both zero for a single point calibration.

#### Example

Calibration resulted in a necessary gain correction of 1.0145 (slope). The value in GAINCORR1 is:

$$(\text{GAINCORR1}) = 1.0145 \times 2^{14} = 16621.568 = 0x40EE \quad (13)$$

### 2.8.13 POFFSETx: I<sub>x</sub> Power Offset Correction

POFFSETx (POFFSETx = POFFSETx\_HI, POFFSETx\_LO = 32-bit value) defines the offset for the correction of the product WAVEFSV1 × WAVEFSIx, where x = 1 or 2 for channels I<sub>1</sub> and I<sub>2</sub>, respectively. Before internally summing the new value, the product of the new voltage and current samples is corrected with GAINCORRx and POFFSETx. See [Section 2.14](#) for more information.

Format	Signed integer	±31.0
Range	0x80000000 to 0x7FFFFFFF	-2.14748E+9 to +2.14748E+9
Normal Range	0xFF000000 to 0x1000000	±224
Resolution	1 step <sup>2</sup>	

#### Formulas

$$P_{ix} = \frac{(\text{WAVEFSIx}) \times (\text{WAVEFSV1}) \times (\text{GAINCORRx})}{2^{14}} + (\text{POFFSETx}) \quad (14)$$

Where:

$P_{ix}$  = Corrected internal ESP430 power calculation for channel I<sub>x</sub>

#### NOTE: POFFSETx Value Format

POFFSETx values are expressed in the internal number format used by the ESP430. These values are 4096 times larger than the calculated energy contained in addresses ACTENERGY1 and ACTENERGY2. This is due to the adaptation of the energy to the meter constants  $C_{z1}$  and  $C_{z2}$ .

## 2.8.14 INTRPTLEVL: Energy Overflow Interrupt Level

INTRPTLEVL (INTRPTLEVL = INTRPTLEVL\_HI, INTRPTLEVL\_LO = 32 bits) defines the trigger threshold for setting ILREACHEDFG in ESP430\_STAT0. MB controls how the ESP430 uses INTRPTLEVL.

- MB = 0: ILREACHEDFG = 1 when the ESP430 accumulated energy count reaches the value in INTRPTLEVL. INTRPTLEVL is subtracted from the ESP430 accumulated energy count and accumulation resumes. ILREACHEDFG is set with the repetition frequency  $f_{IL}$ .
- MB = 1: ILREACHEDFG = 1 when the number of ESP430 measurement cycles performed reaches the value in INTRPTLEVL. The 32-bit measurement count contained in NMBMEAS is cleared, and measurement counting restarts at 0.

Format	Unsigned integer	+32.0
Range	0x00 to 0xFFFFFFFF	0 to +4.294967E+9
Resolution	MB = 0: 1 step <sup>2</sup> MB = 1: 1 measurement	
Initialization	0x80000000	2.147483E+9

### Formulas

Interrupt level frequency:

$$f_{IL} = P \text{ [W]} \times \text{Interrupt Rate [1/Ws]} = \frac{P \times 4096 \times C_Z}{(\text{INTRPTLEVL})}$$

$$\text{Energy per pulse [Ws]} = \frac{1}{\text{Interrupt Rate}} = \frac{(\text{INTRPTLEVL})}{4096 \times C_Z}$$

$$f_{IL(\min)} = \frac{P \times 4096 \times C_Z}{0xFFFFFFFF}$$

$$f_{IL(\max)} = f_{ADC} \rightarrow (\text{INTRPTLEVL})_{\min} > \frac{P_{\max} \times 4096 \times C_Z}{f_{ADC}}$$

$$\text{Error}_{f_{IL(\max)}} = \frac{1}{(\text{INTRPTLEVL})_{\min}} = \frac{f_{ADC}}{P_{\max} \times 4096 \times C_Z} \quad (15)$$

### Example

ILREACHEDFG is to be set with a mean repetition frequency of  $f_{IL} = 2$  kHz for a power  $P = 3$  kW. The  $I_1$  meter constant of the meter is  $C_{Z1} = 29322.81$  steps<sup>2</sup>/Ws:

$$\begin{aligned} (\text{INTRPTLEVL}) &= \frac{3 \text{ [kW]} \times 4096 \times 29,322.81 \text{ [steps}^2\text{/Ws]}}{2 \text{ [kHz]}} = \\ &= 180,159,344.6 \approx 0x0ABD,0370 \end{aligned} \quad (16)$$

### Example

ILREACHEDFG is to be set after 8192 measurements. The value in INTRPTLEVL is 0x2000 (INTRPTLEVL\_LO = 0x2000, INTRPTLEVL\_HI = 0x0). ILREACHEDFG is set every 2 s if  $f_{ADC} = 4096$  Hz.

### ESP430CE1A and ESP430CE1B

Works for both positive and negative energies and is indicated by the flag ILNEGFG.

---

**NOTE:** Return Register Updates

When the interrupt level is reached, only ILREACHEDFG is set; the update of the return registers is not affected.

---

### 2.8.15 CALCYCLCNT: Calibration Cycle Count

CALCYCLCNT defines the number of mains frequency periods used for calibration when the ESP430CE1 is set to Calibration Mode.

Format	Unsigned integer	+16.0
Range	0x00 to 0xFFFF	0 to 65535
Normal Range	0x01 to 0x200	1 to 512
Resolution	1 mains period	
Initialization	0x64	100 mains periods

#### Example

The calibration cycle count required is determined to be 40 mains cycles. The value stored in CALCYCLCNT is 0x0028.

### 2.8.16 STARTCURR: Energy Measurement Start Current

#### ESP430CE1

STARTCURR (STARTCURR = STARTCURR\_INT.STARTCURR\_FRAC = 32 bits) defines the current threshold at which energy accumulation is performed when the ESP430 is not in calibration mode. If the measured current's RMS value is below the threshold defined by STARTCURR, no energy is accumulated.

When both I channels are used, the greater current value of  $I_1$  and  $I_2$  is used and is indicated by I2GT11FG. In this configuration, when one  $I_x$  value is above the STARTCURR threshold, energies for both channels are accumulated.

Format	Unsigned Integer.Fraction	+15.16
Range	0x0.0 to 0x07FFF.FFFF	0.0 to +32767.9999
Normal Range	0x00 to 0x666.C000	0 to 5.0%
Resolution	±0.25 steps are used for the comparison	
Initialization	0x17.2A90	0.1% × 0x7FFF × 0.707

#### Formulas

$$(\text{STARTCURR}) = \frac{I_{\text{START}}}{k_{\text{Icom}}} \times 2^{16} \quad (17)$$

#### Example

The required start current for an electricity meter is 40 mA. The value for STARTCURR is:

$$\begin{aligned} (\text{STARTCURR}) &= \frac{40 \text{ [mA]}}{2.21946 \times 10^{-3} \text{ [A/step]}} \times 2^{16} = \\ &= 1,181,116.127 = 0x0012,05BC \end{aligned} \quad (18)$$

---

#### NOTE: STARTCURR Comparison

The 16-bit value in STARTCURR\_INT and the two MSBs in STARTCURR\_FRAC are used for the  $I_x$  comparison. The remaining LSBs are ignored.

---

### ESP430CE1A and ESP430CE1B

The value in STARTCURR defines the current value for the start of the energy counting if the Operation Mode is not set to Calibration. Below this value all calculated energies (active energy, reactive energy and apparent energy) provided for the CPU are zero. The RMS value of the measured current I is used. For a better resolution the fractional part is also defined. For the comparison the (IRMS) value is used: the flag I2GT11FG defines if the result for I1RMS or I2RMS was stored there. I2GT11FG is not present in the ESP430CE1B.

Format	Unsigned Integer.Fraction	+15.16
Range	0x0.0 to 0x07FFF.FFFF	0.0 to +32767.9999
Normal Range	0x00 to 0x666.5999	0 to 5.0%
Resolution	All 32 bits are used for the comparison	
Initialization	0x17.45A1	0.1% × 0x7FFF × 0.707

#### Formulas

$$(\text{IRMS}) = \frac{\sqrt{(\text{ACTENERGY1})^2 + (\text{REACTENERGY})^2}}{(\text{VRMS})} \text{ [steps]} \quad \text{if I2GT11FG} = 0$$

$$(\text{IRMS}) = \frac{\sqrt{(\text{ACTENERGY2})^2 + (\text{REACTENERGY})^2}}{(\text{VRMS})} \text{ [steps]} \quad \text{if I2GT11FG} = 1$$

$$(\text{STARTCURR}) = \frac{I_{\text{START}}}{k_{\text{Icom}}} \times 2^{16} \quad (19)$$

Example 1: See previous example for ESP430CE1.

Example 2: The required start current for an electricity meter is 40 mA. The value for STARTCURR is:

$$\begin{aligned} (\text{STARTCURR}) &= \frac{I_{\text{START}}}{k_{\text{I1}}} \times 2^{16} = \frac{40 \text{ [mA]}}{2.21946 \times 10^{-3} \text{ [A/step]}} \times 2^{16} = \\ &= 1,181,116.127 = 0x0012,05BC \end{aligned} \quad (20)$$

The value for STARTCURR is 0x05BC (to LSBs at address STARTCURR) and 0x0012 (to MSBs at address STARTCURR + 2). All 16 bits (0x05BC) at the address STARTCURR are used for the comparison.

#### 2.8.17 NOMFREQ: Nominal Mains Frequency

NOMFREQ defines the expected nominal line, or mains, frequency. The mains frequency is required for ESP430 phase correction of DC tolerant current transformers using PHASECORRx.

Format	Unsigned Integer	+8.0
Range	0x00 to 0x0FF	0 to +255
Normal Range	0x28 to 0x46	40 to 70 Hz
Resolution	1 Hz	
Initialization	0x32	50 Hz

#### Example

The expected mains frequency is 60 Hz corresponding to NOMFREQ = 0x3C.

### 2.8.18 VDROPCYCLS: Voltage Drop Detection Cycles

VDROPCYCLS defines the maximum number of contiguous mains voltage cycles having an absolute peak value less than the threshold defined by VDROPLEVEL. If the number of low voltage mains voltage cycles reaches the VDROPCYCLS, VDROPPFG in ESP430\_STAT0 is set. VDROPPFG is reset when the absolute peak level of the voltage is greater than the value in VDROPLEVEL.

Format	Unsigned Integer	+8.0
Range	0x00 to 0xFF	0 to +255 mains periods
Normal Range	Full range	
Resolution	1 mains period	
Initialization	0x05	5 mains periods

#### Formulas

If  $|(WAVESFSV1)| \geq (VDROPLEVEL)$  :  $VDROPPFG = 0$ ,  $vdrop_{cnt} = 0$

If  $|(WAVESFSV1)| < (VDROPLEVEL)$  :  $vdrop_{cnt} = vdrop_{cnt} + 1$

If  $vdrop_{cnt} \geq (VDROPCYCLS)$  :  $VDROPPFG = 1$



## 2.8.19 RATIOTAMP: Tampering Current Ratio

This feature is not available in the ESP430CE1B.

RATIOTAMP defines the threshold for the ratio of the internal ESP430 currents  $I_{1RMS}$  and  $I_{2RMS}$  used to indicate potential meter tampering. This feature is valid for the Energy Plus Tamper Detection configuration only. Both RMS currents are calculated and the greater of the two is stored in IRMS. TAMPFG in ESP430\_STAT0 is set according to the comparison and depends on I2GTI1FG:

TAMPFG = 0: (no tampering) when:

- I2GTI1FG = 0:  $I_{1RMS} < I_{2RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$
- I2GTI1FG = 1:  $I_{2RMS} < I_{1RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$

TAMPFG = 1: (potential tampering occurred) when:

- I2GTI1FG = 0:  $I_{1RMS} \geq I_{2RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$
- I2GTI1FG = 1:  $I_{2RMS} \geq I_{1RMS} \times (\text{RATIOTAMP}) \times 2^{-14}$

When hardware implementations for  $I_1$  and  $I_2$  vary, adaptation for the two channels can be required to get equivalent results under equivalent excitation. Refer to the ADAPTI1 and ADAPTI2 sections for more information.

Format	Unsigned Integer.Fraction	+1.14
Range	0x4000 to 0x7FFF	1.0 to +1.999938965
Normal Range	Full range	
Resolution	$61.035 \times 10^{-6}$	$2^{-14}$
Initialization	0x4000	1.000

### Formulas

$$(\text{RATIOTAMP}) = \left( \frac{I_{HI}}{I_{LO}} \right)_{MAX} \times 2^{14} \quad (21)$$

Where:

$I_{HI}$  = Larger RMS value of  $I_{1RMS}$  and  $I_{2RMS}$

$I_{LO}$  = Smaller RMS value of  $I_{1RMS}$  and  $I_{2RMS}$

### Example

When  $I_x$  RMS currents differ by more than 5%, potential tampering has occurred. RATIOTAMP is:

$$(\text{RATIOTAMP}) = \left( \frac{1.05}{1.00} \right) \times 2^{14} = 17,203.2 \approx 0x4333 \quad (22)$$

---

#### NOTE: $I_x$ RMS Results and TAMPFG

When IRMS is less than the threshold set in ITAMP, TAMPFG = 0 and is not set, regardless of the measured RMS ratio for  $I_1$  and  $I_2$ .

---

### 2.8.20 ITAMP: Tampering Current Threshold (Not Available in the ESP430CE1B)

ITAMP defines the RMS current threshold for  $I_1$  and  $I_2$  enabling the ESP430 to perform a tampering check using RATIOAMP. This feature is valid for the Energy Plus Tamper Detection configuration only.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32767
Normal Range	Full range	
Resolution	1 step	
Initialization	0x2E	0.2% × 0x7FFF × 0.707

#### Formulas

$$(\text{ITAMP}) = \frac{I_{\text{TAMP}}}{k_{\text{Icom}}} \quad (23)$$

Where:

$I_{\text{TAMP}}$  = Current threshold for tamper check

$k_{\text{Icom}}$  = Common meter constant

#### Example

No tampering check to be made below 2% of the specified 40-A maximum RMS current for the meter.

$k_{\text{Icom}} = 0.0025$  A/step.  $I_{\text{TAMP}}$  is:

$$(\text{ITAMP}) = \frac{40 \times 0.02}{0.0025} = 320.0 = 0x140 \quad (24)$$

### 2.8.21 VDROPLEVEL: Voltage Drop Detection Threshold Level

VDROPLEVEL defines the minimum absolute peak value of the mains voltage  $V_1$  expected during a normal mains period. If VDROPLEVEL is not reached, an internal ESP430 counter increments. When this counter reaches the value in VDROPCYCLS, VDROPPFG = 1.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32767
Normal Range	Full range	
Resolution	1 step	

#### Formulas

$$(\text{VDROPLEVEL}) = \frac{|V_{1\text{PEAK}}|}{k_{V1}} = \frac{|V_1| \times \sqrt{2}}{k_{V1}} \quad (\text{for sinusoidal voltage}) \quad (25)$$

#### Example

VDROPPFG should be set when  $V_1$  falls below 75% of the nominal voltage of 230 V for 6 or more mains periods,  $k_{V1} = 15.365513 \times 10^{-3}$ . VDROPCYCLS = 0x6, VDROPLEVEL is:

$$(\text{VDROPLEVEL}) = \frac{|230 \times 0.75| \times \sqrt{2}}{15.365513 \times 10^{-3}} = 15,876.58 \approx 0x3E05 \quad (26)$$

---

**NOTE:** VDROPPFG and V1RMS

When V1RMS is less than  $0.088 \times \text{VDROPLEVEL}$ , VDROPPFG is set independent of the internal ESP430 counter used for VDROPLEVEL.

---

### 2.8.22 VPEAKLEVEL: Voltage Peak Level

VPEAKLEVEL defines the maximum value for  $V_1$ . If the absolute value of the measured voltage is greater than VPEAKLEVEL, V1PEAKFG = 1, otherwise V1PEAKFG = 0. To filter out single spikes on the line, three contiguous measurements must exceed VPEAKLEVEL.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32767
Normal Range	Full range	
Resolution	1 step	
Initialization	0x7FFF	Maximum voltage value

#### Formulas

$$(VPEAKLEVEL) = \frac{|V_{1MAX}|}{k_{V1}} \quad (27)$$

Where:

$V_{1MAX}$  = Maximum  $V_1$  peak voltage

#### Example

$V_{1MAX}$  is specified to be  $\pm 398V$ ;  $k_{V1} = 15 \times 10^{-3}$ . VPEAKLEVEL is:

$$(VPEAKLEVEL) = \frac{|V_{1MAX}|}{k_{V1}} = \frac{398[V]}{15 \times 10^{-3} [V/step]} \approx 0x67A5 \quad (28)$$

V1PEAKFG = 1 if three contiguous, voltage samples greater than 0x67A5 or less than 0x985B are measured (0x985B = -0x67A5), else V1PEAKFG = 0.

### 2.8.23 IPEAKLEVEL: Current Peak Level

IPEAKLEVEL defines the maximum value for  $I_1$  and  $I_2$ . If the absolute value of each measured current is greater than IPEAKLEVEL, IxPEAKFG = 1, otherwise IxPEAKFG = 0, where  $x = 1$  or  $2$  for  $I_1$  or  $I_2$ , respectively. To filter out single spikes on the line, three contiguous measurements must exceed IPEAKLEVEL.

Format	Unsigned Integer	+15.0
Range	0x00 to 0x07FFF	0.0 to +32767
Normal Range	Full range	
Resolution	1 step	
Initialization	0x7FFF	Maximum current value

#### Formulas

$$(IPEAKLEVEL) = \frac{|I_{max}|}{k_{Icom}} \quad (29)$$

#### Example

I1PEAKFG = 1 when a current sample greater than  $42 A \times 1.414$  (peak value for 42 A) is measured on  $I_1$ ,  $k_{Icom1} = 0.0025 A/step$ . IPEAKLEVEL is:

$$(IPEAKLEVEL) = \frac{42 \times \sqrt{2}}{2.5 \times 10^{-3} [A/step]} = 23,758.79 \approx 0x5CCE \quad (30)$$

## 2.8.24 DCREMPER: DC Removal Period Count

DCREMPER defines the number of mains periods used for one iteration of the DC removal algorithm. Larger values in DCREMPER can improve noise suppression and result in longer calculation settling times. When the DC removal function is disabled, DCREMPER is not used.

If the dc removal function is not on (with bits DCREM\_V1, DCREM\_I1, DCREM\_I2):

ESP430CE1: The offset measured with shorted ADC inputs during the initialization (or with the INIT Control Command) is used.

ESP430CE1A: The value 0 is used.

Format	Unsigned Integer	+6.0
Range	0x00 to 0x032	0 to +50 (due to 32-bit sum buffer capacity)
Resolution	1 mains period	
Initialization	0x05	5 mains periods

## 2.8.25 DC Removal Function Description

If the AFE voltage and current samples contain offsets or DC components, the measured energy  $W$  is:

$$\begin{aligned}
 W &= \frac{1}{f_{\text{ADC}}} \times \sum_{t=0}^{t=\infty} (v_n + v_{\text{dc}}) \times (i_n + i_{\text{dc}}) = \\
 &= \frac{1}{f_{\text{ADC}}} \times \sum_{t=0}^{t=\infty} (v_n \times i_n + v_n \times i_{\text{dc}} + i_n \times v_{\text{dc}} + i_{\text{dc}} \times v_{\text{dc}})
 \end{aligned} \tag{31}$$

Where:

$v_{\text{dc}}$  = DC part of a voltage sample [V]

$i_{\text{dc}}$  = DC part of a current sample [A]

$v_n$  = voltage sample [V]

$i_n$  = current sample [A]

---

**NOTE:** With the ESP430CE1A, a watchdog is implemented for a missing voltage  $V_1$  (see [Section 2.9.2](#)).

---

The terms  $(v_n \times i_{\text{dc}})$  and  $(i_n \times v_{\text{dc}})$  in the previous equation equal zero when summed over one full mains period (the integral of a sine wave from 0 to  $2\pi = 0$ ). However, the term  $(i_{\text{dc}} \times v_{\text{dc}})$  is added erroneously to the energy summation with each sample result. If one of the two offsets can be set to zero, the error term is eliminated.

With the DC removal function enabled, it is possible to eliminate the DC component for the  $V_1$  voltage path or the current paths,  $I_1$  and  $I_2$ . DCREMPER defines the number of mains periods used for the calculation of the DC removal values.

## 2.9 Detection of Zero Crossing

### 2.9.1 Zero Crossing Checks

Zero crossing of the voltage  $V_1$  is detected by the change of the sign of  $V_1$  after two samples with the same sign:

- Leading edge: a positive  $V_1$  sample follows two negative ones.
- Trailing edge: a negative  $V_1$  sample follows two positive ones.

#### ESP430CE1A and ESP430CE1B

To get secure results with noise and spikes on the voltage  $V_1$ , two limits are given for the change of  $V_1$ :

- The two  $V_1$  samples before and after the sign change must have minimum distances of 502 ADC steps. This avoids noise induced, false zero crossings.
- V1FILTER enabled: Spikes of  $V_1$  are checked against the value (DELTA V1MAX) in the parameter registers. The voltage sample differences  $|\Delta N_{v1}|$  must be smaller than (DELTA V1MAX), otherwise a linear approximation is used for the actual  $V_1$  sample  $v1n$ .

The V1FILTER avoids false zero crossings by large spikes.

If V1FILTER = 0:

No  $V_1$  check is made. Sample  $v1n$  is used as it is.

If V1FILTER = 1:

If  $|N_{v1n} - N_{v1n-1}| < (\text{DELTA V1MAX})$ , sample  $v1n$  is used as it is.

Else:  $N_{v1n} = (N_{v1n-1} - N_{v1n-2}) + N_{v1n-1} = 2N_{v1n-1} - 2N_{v1n-2}$ , a linear approximation for sample  $v1$  is used.

If the V1FILTER is used, the value for (DELTA V1MAX) must be set by the CPU to the maximum  $dv1/dt$  value for the used ADC range, multiplied with a security factor  $k_{\text{safety}}$  (for example, 1.2):

$$(\text{DELTA V1MAX}) = 2\pi \times f_{\text{mains max}} \times \frac{N_{\text{ADC max}}}{f_{\text{ADC}}} \times k_{\text{safety}} \quad (32)$$

#### Example

The V1FILTER is used with a used ADC range of 90%, a maximum mains frequency of 51 Hz, an ADC frequency of 4096 Hz and a safety factor of 1.1. The value in DELTA V1MAX is:

$$(\text{DELTA V1MAX}) = 2\pi \times 51 \times \frac{0.9 \times 7FFFh}{4096} \times 1.1 = 2538 \quad (33)$$

### 2.9.2 Zero Crossing Watchdog (ESP430CE1A and ESP430CE1B)

With  $V_1$  disconnected, no zero crossings occur and no mains period measurements are made. To allow the important dc removal calculations without  $V_1$ , a watchdog is implemented for the zero crossing detection. This Zero Crossing Watchdog is reset with each detected valid zero crossing of  $V_1$  and incremented with the sample frequency  $f_{\text{ADC}}$ . If the watchdog reaches the fixed value:

$$\text{ZCWD} = \frac{f_{\text{ADC max}}}{f_{\text{mains min}}} + k_{\text{ZCWD}} = \frac{4096}{40} + 40 \approx 142 \quad (34)$$

The dc removal calculations are processed with the accumulated values and the watchdog is reset.

The maximum repetition frequency  $f_{\text{DCRm max}}$  of the dc removal function due to the Zero Crossing Watchdog is:

$$f_{\text{DCRm max}} = \frac{f_{\text{ADC}}}{(\text{DCREMPER}) \times \text{ZCWD}} + 1 \text{ [Hz]} \quad (35)$$

With the initial value of 5 for (DCREMPER) and  $f_{\text{ADC}} = 4096$  Hz this leads to:

$$f_{\text{DCRm max}} = \frac{4096}{5 \times 142} + 1 \approx 6 \text{ [Hz]} \quad (36)$$

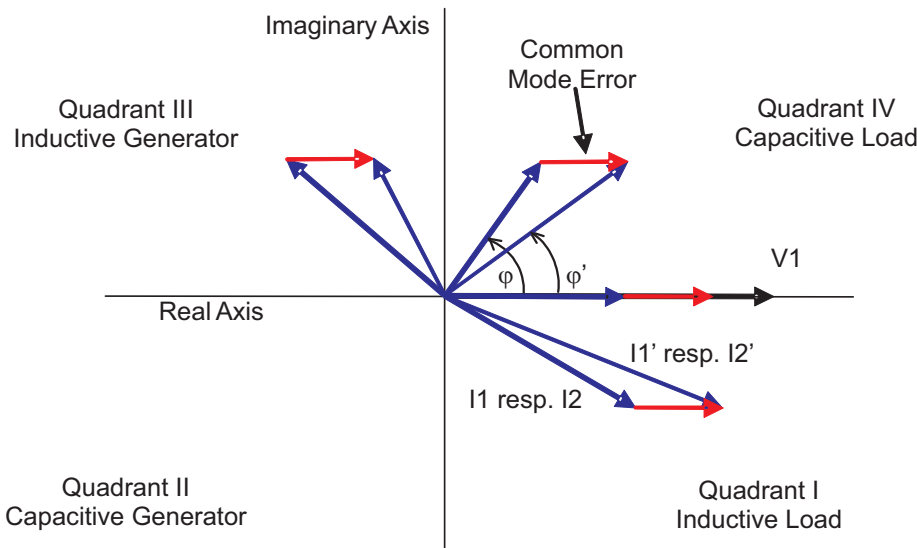
The dc removal function is called with a repetition frequency of 6 Hz if  $V_1$  is missing.

With the safety function of the Zero Crossing Watchdog, energy measurements are still possible without  $V_1$  connected: the correctly measured value IRMS is multiplied by a defined value for  $V_1$ , for example, 100%. The multiplication and accumulation is made by the CPU in this case.

### 2.10 Common Mode Rejection (ESP430CE1A and ESP430CE1B)

Figure 5 shows the common mode influence of the voltage  $V_1$  to the currents  $I_1$  and  $I_2$ . This influence is visible only at very low currents. The common mode influence is a constant error value (shown red in Figure 5) in phase with the voltage  $V_1$ . The common mode influence changes the phase angle  $\varphi$  to  $\varphi'$  and the current values from  $I_1$  and  $I_2$  to  $I_1'$  and  $I_2'$  dependent on the quadrant of the current.

These two changes introduce a measurement error that depends on the phase angle  $\varphi$  and the current value.



NOTE: References to  $I_2$  and  $I_2'$  do not apply to the ESP430CE1B.

Figure 5. Common-Mode Influence to the Current Path

Figure 6 shows the dependence of the measurement error to the phase angle  $\varphi$ . It is described by the  $\cos^{-1}\varphi$  function.

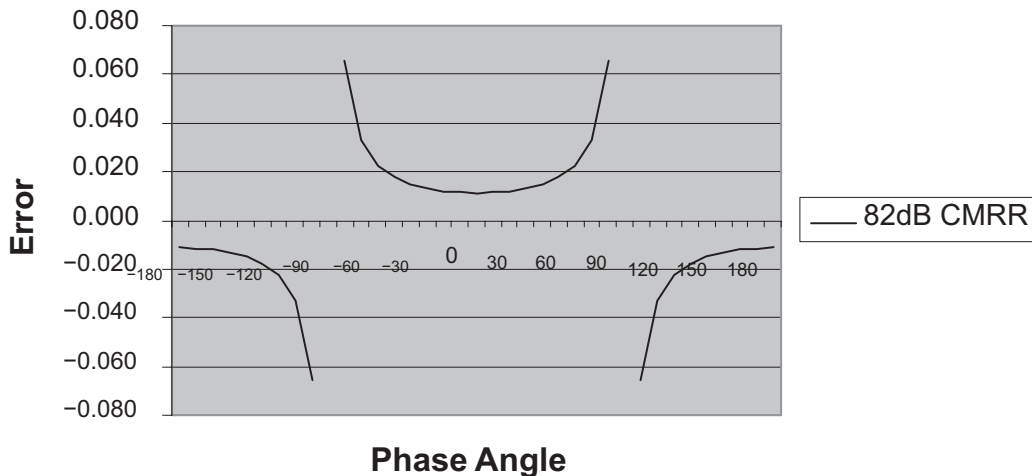


Figure 6. E-Meter Error Due to CMRR

Due to the constant value and phase angle of the introduced common mode error, it is possible to correct this error: it is only necessary to subtract its value from all measured active energy values.

The value in address CORRCOMP controls the common mode rejection function of the ESP430CE1A:

- If (CORRCOMP) = 0: the common mode rejection function is switched off.
- If (CORRCOMP) > 0: the value is a quarter of the actual value to be used. This is to allow also the compensation of small common mode influences.

The value in CORRCOMP is approximately given by:

$$(\text{CORRCOMP}) = 0.25 \times 10^{(0.05 \times \text{CMRR})} \quad (37)$$

The compensation value (CORRCOMPStore) for the active energies is calculated with the formula:

$$(\text{CORRCOMPStore}) = \frac{(V1\text{RMS})^2}{4 \times (\text{CORRCOMP})} \quad (38)$$

(CORRCOMPStore) is used for the correction of all measured active energies:

- Active energy for 4096 samples (ACTENERGY1 and ACTENERGY2). The common mode correction is made with the value for (CORRCOMPStore) of the actual 4096 samples.
- Active energy for a single mains period (ACTENSPER1 and ACTENSPER2). The common mode correction is made with the value for (CORRCOMPStore) of the last 4096 samples, not of the actual ones: the actual value of (CORRCOMPStore) is not yet available.
- Active energy used with bit ILREACHEDFG if bit MB = 0 (ILREACHEDFG is set dependent on the reached energy level). The common mode correction is made with the value for (CORRCOMPStore) of the last 4096 samples, not of the actual ones: the actual value for (CORRCOMPStore) is not yet available.

The reactive energy is not influenced by the common mode and, therefore, needs no correction. The apparent energy is calculated with the corrected active energy and the not influenced reactive energy, and is also correct.

## 2.11 Maximum Spike for V<sub>1</sub> Filter (ESP430CE1A and ESP430CE1B)

The value in DELTAV1MAX defines the maximum tolerable change from one V<sub>1</sub> sample to the next one if the V<sub>1</sub> Filter is enabled (bit V1FILTER = 1). If the V<sub>1</sub> Filter is enabled and the change from one V<sub>1</sub> sample to the last one exceeds the value in DELTAV1MAX (absolute values are used), then a linear approximation is made for the value N<sub>v1n</sub>. Otherwise the N<sub>v1n</sub> value is used unmodified.

Format	Unsigned Integer Word	+16.0
Range	0x00 to 0xFFFF	0.0 to +65535
Resolution	1 step	
Initialization	0x0	

### Formulas

$|N_{v1n} - N_{v1n-1}| < (\text{DELTAV1MAX}) \rightarrow$  sample v1n is used as is

$|N_{v1n} - N_{v1n-1}| \geq (\text{DELTAV1MAX}) \rightarrow N_{v1n} = (N_{v1n-1} - N_{v1n-2}) + N_{v1n-1} = 2N_{v1n-1} - 2N_{v1n-2}$

$$(\text{DELTAV1MAX}) \geq 2\pi \times f_{\text{mains max}} \times \frac{N_{\text{ADC max}}}{f_{\text{ADC}}} \times k_{\text{safety}} \quad \text{value for (DELTAV1MAX)} \quad (39)$$

### Example

The V1FILTER is used with a used ADC range of 95%, a maximum mains frequency of 66 Hz, an ADC frequency of 2048 Hz, and a safety factor of 1.2. The value for (DELTAV1MAX) is:

$$(\text{DELTAV1MAX}) \geq 2\pi \times 66 \times \frac{0.95 \times 0x7FFF}{2048} \times 1.2 = 7564 = 0x1D8B \quad (40)$$

## 2.12 Common Mode Rejection Ratio (ESP430CE1A and ESP430CE1B)

The value in CORRCOMP defines the value of the common mode rejection ratio for the two current ADCs due to the voltage ADC. If the value in CORRCOMP is zero, no correction of the common mode influence is made. The value in CORRCOMP is multiplied by 4 before its use to allow the compensation of small common mode influences. The calculated compensation value is stored in the RAM address CORRCOMPStore and used for the correction of all active energies [4096 samples, single mains period and energy level count (bit MB = 0)]. The correction depends on the squared value of (V1RMS).

Format	Unsigned Integer Word	+16.0
Range	0x00 to 0xFFFF	0.0 to +262140 (108.37 dB)
Resolution	4	
Initialization	0x0	

### Formulas

$$(\text{CORRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CORRCOMP})} \text{ [steps}^2\text{]}$$

$$(\text{CORRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CORRCOMPStore})} \text{ [1]} \quad (41)$$

### Example

The necessary CMRR compensation for active energy 1 is 3554 steps<sup>2</sup>. The measured RMS value V1RMS for voltage V<sub>1</sub> is 29EAh. This leads to a value for CORRCOMP:

$$(\text{CORRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CORRCOMP})} = \frac{0x29EA^2}{4 \times 3554} = 8098.82 \quad (42)$$

The rounded value 8099 (1FA3h) is written to address CORRCOMP.

### Example

An electricity meter showed the following common mode errors for small currents dependent on the phase angle  $\varphi$  (the absolute value of all four  $|\cos\varphi| = 0.5$ ):

$$I_1 = 10 \text{ A (10\% } I_{\max}), \varphi = 0^\circ, \text{Err}_{\text{Hi}} = +0.1\% \text{ calibrated value}$$

$$I_1 = 0.2 \text{ A (0.2\% } I_{\max}), \varphi = +120^\circ, \text{Err}_{\text{Lo}120} = -1.8\%$$

$$I_1 = 0.2 \text{ A (0.2\% } I_{\max}), \varphi = +60^\circ, \text{Err}_{\text{Lo}60} = +2.2\%$$

$$I_1 = 0.2 \text{ A (0.2\% } I_{\max}), \varphi = 0^\circ, \text{Err}_{\text{Lo}0} = +1.4\%$$

$$I_1 = 0.2 \text{ A (0.2\% } I_{\max}), \varphi = -60^\circ, \text{Err}_{\text{Lo}-60} = +1.9\%$$

$$I_1 = 0.2 \text{ A (0.2\% } I_{\max}), \varphi = -120^\circ, \text{Err}_{\text{Lo}-120} = -2.2\%$$

The measured RMS value (V1RMS) for voltage V<sub>1</sub> is 29EAh. The correct value for (ACTENERGY1) for I<sub>1</sub> = 0.2 A and  $\varphi = 0^\circ$  is 533E1h. The necessary correction value for the active energies (CORRCOMPStore) is:

$$(\text{CORRCOMPStore}) = 0.25 \times (|\text{Err}_{\text{Lo}120}| + |\text{Err}_{\text{Lo}60}| + |\text{Err}_{\text{Lo}-60}| + |\text{Err}_{\text{Lo}-120}|) \times (\text{ACTENERGY1}) \times |\cos\varphi|$$

$$(\text{CORRCOMPStore}) = 0.25 \times (|-0.018| + |0.022| + |0.019| + |-0.022|) \times 533E1h \times 0.5 = 3452.23 \quad (43)$$

To get the needed correction value 3452 with the measured V<sub>1</sub> voltage:

$$(\text{CORRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CORRCOMPStore})} = \frac{0x29EA^2}{4 \times 3452.23} = 8337.57 \quad (44)$$

The rounded value 8338 is written to address CORRCOMP. The correction value (CORRCOMPStore) is:

$$(\text{CORRCOMPStore}) = \frac{(\text{V1RMS})^2}{4 \times (\text{CORRCOMP})} = \frac{0x29EA^2}{4 \times 8338} = 3452.05 \quad (45)$$



With this correction value, the six measured errors improve to:

$$I_1 = 10 \text{ A (10\% I}_{\max}), \phi = 0^\circ, \text{Err}_{\text{Hi}} = -202 \text{ ppm (calibrated value)}$$

$$I_1 = 0.2 \text{ A (0.2\% I}_{\max}), \phi = +120^\circ, \text{Err}_{\text{Lo120}} = +0.22\%$$

$$I_1 = 0.2 \text{ A (0.2\% I}_{\max}), \phi = +60^\circ, \text{Err}_{\text{Lo60}} = +0.17\%$$

$$I_1 = 0.2 \text{ A (0.2\% I}_{\max}), \phi = 0^\circ, \text{Err}_{\text{Lo0}} = +0.39\%$$

$$I_1 = 0.2 \text{ A (0.2\% I}_{\max}), \phi = -60^\circ, \text{Err}_{\text{Lo-60}} = -0.12\%$$

$$I_1 = 0.2 \text{ A (0.2\% I}_{\max}), \phi = -120^\circ, \text{Err}_{\text{Lo-120}} = -0.18\%$$

If the phase angles used for the previous calculation show different values for  $|\cos \phi|$ , then a correction to equal absolute phase angles is necessary. This is made with the formula:

$$\text{Err}_{\text{Lo}\phi_{\text{corr}}} = \text{Err}_{\text{Lo}\phi} \times \frac{\cos \phi}{\cos \phi_{\text{corr}}} \quad (46)$$

For example, the  $120^\circ$  error  $\text{Err}_{\text{Lo120}}$  is measured with a phase angle  $\phi = +124^\circ$ , due to the calibration equipment.

$$I_1 = 0.2 \text{ A (0.2\% I}_{\max})$$

$$\phi = +124^\circ$$

$$\text{Err}_{\text{Lo124}} = -2.0\%$$

$$\text{Err}_{\text{Lo120}} = \text{Err}_{\text{Lo124}} \times \frac{\cos \phi}{\cos \phi_{\text{corr}}} = -2.0\% \times \frac{\cos 124}{\cos 120} = -2.237\% \quad (47)$$

The corrected electricity meter error with  $\phi = +120^\circ$  is  $-2.237\%$ .

## 2.13 ESP430CE1, ESP430CE1A, and ESP430CE1B Return Registers Description

The return registers are used to pass calculated results and status information from the ESP430 to the CPU.

### 2.13.1 ESP430\_STAT0: Embedded Processor Status Register 0

ESP430\_STAT0 and the ESP430\_STAT1 indicate the occurrence of ESP430CE1, ESP430CE1A, and ESP430CE1B events to the CPU. The ESP430\_STAT1 is present only in the ESP430CE1A. When the corresponding enable bit is set in the EVENT parameter register, a change in value from 0 to 1 of each ESP430\_STAT0/ESP430\_STAT1 bit triggers a mailbox message to be sent from the ESP430 to the CPU. ESP430\_STAT0 and ESP430\_STAT1 flags are set independently of the settings in EVENT. [Table 10](#) describes the ESP430\_STAT0 bits. [Table 11](#) describes the ESP430\_STAT1 bits.

**Table 10. ESP430\_STAT0 Bit Summary**

Name	Bit Function
ACTIVEFG	Indicates the ESP430 is in MEASURE or CALIBRATION mode and is active. I2PEAKFG <sup>(1)</sup> Indicates an overcurrent condition has occurred on I <sub>2</sub> as defined by IPEAKLEVEL when exceeded for three contiguous I <sub>2</sub> samples. When set, the larger I <sub>x</sub> value is stored in IPEAK. Cannot be cleared by the CPU.
I1PEAKFG <sup>(1)</sup>	Indicates an overcurrent condition has occurred on I <sub>1</sub> as defined by IPEAKLEVEL when exceeded for three contiguous I <sub>1</sub> samples. When set, the larger I <sub>x</sub> value is stored in IPEAK. Cannot be cleared by the CPU.
VPEAKFG	Indicates an overvoltage condition has occurred on V <sub>1</sub> as defined by VPEAKLEVEL when exceeded for three contiguous V <sub>1</sub> samples. Cannot be cleared by the CPU.
VDROPFG	Indicates an undervoltage condition has occurred on V <sub>1</sub> as defined by VDROPLEVEL and VDROPCYCLS. Cannot be cleared by the CPU.
NEGENFG	Indicates that negative energy has been accumulated over the last 4096 measurements. This can be caused by meter tampering or delivery of energy into the line by the load. Treatment of negative energy is defined by ESP430_CTRL0 bits NE0 and NE1. Cannot be cleared by the CPU.
TAMPFG <sup>(1)</sup>	Indicates possible meter tampering has occurred. See ESP430CE1 Energy Measurement Configurations for more information on tamper detection. Cannot be cleared by the CPU.
CALRDYFG	Indicates the end of the calibration routine and availability of new active energy values in ACTENERGYx. This flag only applies when the ESP430 is in CALIBRATION mode. Cleared when the ESP430 is sent into IDLE mode.
ZXTRFG	Indicates the occurrence of a trailing-edge zero crossing (positive-to-negative) on V <sub>1</sub> . The following tasks are performed following a trailing-edge zero crossing: <ul style="list-style-type: none"> <li>• If pending, a temperature measurement is initiated.</li> <li>• Undervoltage checks are performed for the last mains period, and VDROPF is set accordingly.</li> </ul> All tasks except the temperature result are completed with the next available waveform samples after the zero crossing indicated by WFSRDYFG immediately after ZXTRFG has been set. To simplify flag handling ZXLDG can be used to indicate completion of the ZXTRFG tasks. Cleared when a leading-edge zero crossing occurs and cannot be reset by the CPU.
ZXLDG	Indicates the occurrence of a leading-edge zero crossing (negative-to-positive) on V <sub>1</sub> . The following tasks are performed following a leading-edge zero crossing: <ul style="list-style-type: none"> <li>• If pending, a temperature measurement is initiated.</li> <li>• MAINSPERIOD is calculated and updated.</li> <li>• Load type is determined and an internal counter increments for a capacitive load or decrements for an inductive load. This value is written to CAPIND after every 4096 mains periods.</li> <li>• LINECYCLCNT increments.</li> <li>• ACTENSPER1 and ACTENSPER2 are updated.</li> <li>• VPEAK and IPEAK are updated.</li> </ul> All tasks except the temperature result are completed with the next available waveform samples after the zero crossing indicated by WFSRDYFG immediately after ZXLDG has been set. To simplify flag handling ZXTRFG can be used to indicate completion of the ZXLDG tasks. Cleared when a trailing-edge zero crossing occurs and cannot be reset by the CPU.
ENRDYFG	Indicates new calculated ESP430 values are ready. Associated registers are V1RMS, IRMS, ACTENERGYx, REACTENERGY, APPENERGY, POWERFCT and CAPIND. Cleared when the event message is sent or by the mCLR_EVENT control command.
ILREACHEDFG	Indicates that the interrupt level threshold for energy accumulation or number of measurements performed was reached as defined by the INTRPTLEVL parameter register and the MB control bit in ESP430_CTRL0. Cleared when the event message is sent or by the mCLR_EVENT control command.

<sup>(1)</sup> Not present in the ESP430CE1B

**Table 10. ESP430\_STAT0 Bit Summary (continued)**

Name	Bit Function
I2GTI1FG <sup>(1)</sup>	Indicates the current channel with the larger RMS value over the last 4096 samples and is set when $I_2$ RMS > $I_1$ RMS if CURR_I2 = 1. I2GTI1FG is always zero when CURR_I2 = 0. Cannot be cleared by the CPU.
WFSRDYFG	Indicates new waveform samples are ready in WAVEFSV1, WAVEFSI1 and WAVEFSI2 registers. Cleared when the event message is sent or by the mCLR_EVENT control command.

**Table 11. ESP430\_STAT1 Bit Summary<sup>(1)</sup>**

Name	Bit Function
Reserved	Bits 0 and 1 are reserved.
ILNEGFG	Interrupt Level Negative Bit. The ILNEGFG bit (bit 2) indicates the sign of the energy of the reached Interrupt Level. 0 = Energy is positive 1 = Energy is negative Set if the energy of the reached interrupt level is negative. Reset if the energy of the reached interrupt level is positive. It is not reset by sending an event message or with the command CLR_EVENT.
Reserved	Bits 3 to 9 are reserved.
V1PEAKNEGFG	$V_1$ Negative Peak Bit. The V1PEAKNEGFG bit (bit 10) indicates the sign of the measured $V_1$ peak. 0 = Last $V_1$ peak was positive. 1 = Last $V_1$ peak was negative. The bit is not reset by sending an event message or with the command CLR_EVENT.
I1PEAKNEGFG	$I_1$ Negative Peak Bit. The I1PEAKNEGFG bit (bit 11) indicates the sign of the measured $I_1$ peak. 0 = Last $I_1$ peak was positive. 1 = Last $I_1$ peak was negative. The bit is not reset by sending an event message or with the command CLR_EVENT.
I2PEAKNEGFG <sup>(2)</sup>	$I_2$ Negative Peak Bit. The I2PEAKNEGFG bit (bit 12) indicates the sign of the measured $I_2$ peak. 0 = Last $I_2$ peak was positive 1 = Last $I_2$ peak was negative The bit is not reset by sending an event message or with the command CLR_EVENT.
Reserved	Bits 13 to 15 are reserved.

<sup>(1)</sup> Present in only the ESP430CE1A and ESP430CE1B

<sup>(2)</sup> Not present in the ESP430CE1B

### 2.13.2 WAVEFSV1: $V_1$ Waveform Sample

The last offset-corrected ADC sample for  $V_1$  is in WAVEFSV1. The correction of the original ADC result  $N_{V1ADC}$  is made with the offset correction for  $V_1$  contained in V1OFFSET and a second offset depending on bit DCREM\_V1.

Format	Signed integer	$\pm 15.0$
Range	0x8000 to 0x07FFF	-32768 to +32767
Resolution	1 step	

#### Formulas

DCREM\_V1 = 0:

$$(WAVEFSV1) = N_{V1ADC} - N_{V1SC} + (V1OFFSET) \quad (48)$$

DCREM\_V1 = 1:

$$(WAVEFSV1) = N_{V1} = N_{V1ADC} - N_{V1DCREM} + (V1OFFSET) \quad (49)$$

$$V_1 = k_{V1} \times (WAVEFSV1) \quad (50)$$

Where:

$N_{V1ADC}$  = Conversion value from SD16  $V_1$  channel

$N_{V1SC}$  = ESP430-corrected offset value taken during INIT with shunted SD16  $V_1$  channel inputs.

$N_{V1DCREM}$  = ESP430-corrected offset value calculated by the DC removal algorithm (see DCREM\_V1 description).

$V_1$  = Meter-specific result obtained by multiplying WAVEFSV1 with the meter constant  $k_{V1}$ .

#### Example

An input voltage sample corresponding to a conversion result of 0x32D8 was measured. DCREM\_V1 = 0 (DC removal function is off). The value for  $N_{V1SC}$  = 0xFFFFB (-0x5) and V1OFFSET = 0x13. WAVEFSV1 is calculated as:

$$(WAVEFSV1) = 0x32D8 + 0x5 + 0x13 = 0x32F0 \quad (51)$$

### 2.13.3 WAVEFSIx: I<sub>x</sub> Waveform Sample

The last offset-corrected ADC sample for I<sub>x</sub> is in WAVEFSIx, where x = 1 or 2 for I<sub>1</sub> or I<sub>2</sub>, respectively. The correction of the original ADC result N<sub>IXADC</sub> is made with the offset correction for I<sub>x</sub> contained in IxOFFSET, a second offset depending on bit DCREM\_Ix and the adaptation value for I<sub>x</sub> in ADAPTIx.

Format	Signed integer	±15.0
Range	0x8000 to 0x07FFF	-32768 to +32767
Resolution	1 step	

#### Formulas

DCREM\_Ix = 0:

$$(WAVEFSIx) = N_{IXADC} - N_{IXSC} + (IxOFFSET) \times (ADAPTIx) \times 2^{-14} \quad (52)$$

DCREM\_Ix = 1:

$$(WAVEFSIx) = N_{IXADC} - N_{IXDC} + (IxOFFSET) \times (ADAPTIx) \times 2^{-14} \quad (53)$$

$$I_x = k_{Ix} \times (WAVEFSIx) \quad (54)$$

Where:

N<sub>IXADC</sub> = Conversion value from SD16 I<sub>x</sub> channel

N<sub>IXSC</sub> = ESP430-corrected offset value taken during INIT with shunted SD16 I<sub>x</sub> channel inputs.

N<sub>IXDCREM</sub> = ESP430-corrected offset value calculated by the DC removal algorithm (see DCREM\_Ix description)

I<sub>x</sub> = Meter-specific result obtained by multiplying WAVEFSIx with the meter constant k<sub>Ix</sub>.

#### Example

An input current sample corresponding to a conversion result of 0x1234 on I<sub>1</sub> was measured. DCREM\_I1 = 1 (DC removal function is on), the value for NI1DCREM = 0xFFFFB (-0x5) and I1OFFSET = 0xFFEF (-0x11). With ADAPT11 = 0x40CF (1.01264) the corrected value written to WAVEFSI1 is:

$$(WAVEFSI1) = (0x1234 - 0xFFFFB + 0xFFEF) \times 0x40C \times 2^{-14} = 0x1262 \quad (55)$$

### 2.13.4 ACTENERGYx: I<sub>x</sub> Active Energy

The calculated active energy of I<sub>x</sub> for the last 4096 ADC measurements is stored in ACTENERGYx, where x = 1 or 2 for I<sub>1</sub> and I<sub>2</sub>, respectively. This value also represents the average active power P<sub>actx</sub> over the same measurement time (ACTENERGYx = ACTENERGYx\_HI, ACTENERGYx\_LO = 32 bits).

#### ESP430CE1A and ESP430CE1B

The comparison of the two absolute, active energies (ACTENERGY1) and (ACTENERGY2) defines the flag I2GTI1FG (I<sub>2</sub> greater than I<sub>1</sub>). I2GTI1FG is not present in the ESP430CE1B:

- If |(ACTENERGY1)| ≥ |(ACTENERGY2)|: I2GTI1FG = 0
- If |(ACTENERGY2)| > |(ACTENERGY1)|: I2GTI1FG = 1

The compensation value (CORRCOMPStore) for the common mode influence is subtracted from the calculated active energy 1. The compensation value is zero if the common mode compensation is switched off ((CORRCOMP) = 0).

#### ESP430CE1A

The comparison of the two absolute, active energies (ACTENERGY1) and (ACTENERGY2) defines the flag I2GTI1FG:

- If |(ACTENERGY1)| ≥ |(ACTENERGY2)|: I2GTI1FG = 0
- If |(ACTENERGY2)| > |(ACTENERGY1)|: I2GTI1FG = 1

The compensation value (CORRCOMPStore) for the common mode influence is subtracted from the calculated active energy 2 if bit I2CMRR = 1 in ESP430\_CTRL0. The compensation value is zero if the common mode compensation is switched off ((CORRCOMP) = 0).

Format	Signed integer	±31.0
Range	0x80000000 to 0x07FFFFFFF	
Resolution	1 step <sup>2</sup> = 1/C <sub>Z1</sub>	Normal operation
	16 steps <sup>2</sup> = 16/C <sub>Zx</sub>	Calibration mode

#### Formulas

$$(\text{ACTENERGYx}) = \frac{1}{4096} \times \sum_{i=1}^{4096} (\text{WAVEFSV1})_x (\text{WAVEFSI}_x) \text{ [steps}^2\text{]} \quad (56)$$

Energy:

$$W_{\text{actx}} = \frac{(\text{ACTENERGYx})}{C_{Zx}} = (\text{ACTENERGYx}) \times k_{ix} \times k_{v1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]} \quad (57)$$

Power:

$$P_{\text{actx}} = \frac{(\text{ACTENERGYx})}{C_{Zx}} \times \frac{f_{\text{ADC}}}{4096} = (\text{ACTENERGYx}) \times k_{ix} \times k_{v1} \text{ [W]} \quad (58)$$

---

**NOTE:** ACTENERGYx and STARTCURR

When the RMS value for I<sub>x</sub> is smaller than the value in STARTCURR, ACTENERGYx is set to zero.

---

### 2.13.5 REACTENERGY: Reactive Energy

The calculated reactive energy of the last 4096 measurements is stored in REACTENERGY. This value also represents the average reactive power  $P_{\text{react}}$  over the same measurement time.

(REACTENERGY = REACTENERGY\_HI, REACTENERGY\_LO = 32 bits)

I2GTI1FG determines if the reactive energy is calculated for  $I_1$  or  $I_2$ . The larger current is always used for the calculation of REACTENERGY. I2GTI1FG is not present in the ESP430CE1B.

- I2GTI1FG = 0: ACTENERGY1 and APPENERGY are used to calculate  $W_{\text{react}}$ .
- I2GTI1FG = 1: ACTENERGY2 and APPENERGY are used to calculate  $W_{\text{react}}$ .

#### ESP430CE1

Format	Unsigned integer	+31.0
Range	0x00000000 to 0x07FFFFFFF	
Resolution	1 step <sup>2</sup> = 1/C <sub>Z</sub> = 1/C <sub>Z1</sub> = 1/C <sub>Z2</sub>	

#### Formulas

I2GTI1FG = 0:

$$(\text{REACTENERGY}) = \sqrt{(\text{APPENERGY})^2 - (\text{ACTENERGY1})^2} \text{ [steps}^2\text{]}$$

$$W_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z1}} = (\text{REACTENERGY}) \times k_{I1} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]} \quad (59)$$

I2GTI1FG = 1:

$$(\text{REACTENERGY}) = \sqrt{(\text{APPENERGY})^2 - (\text{ACTENERGY2})^2} \text{ [steps}^2\text{]}$$

$$W_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z2}} = (\text{REACTENERGY}) \times k_{I2} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]} \quad (60)$$

The average reactive power of the last 4096 measurements is:

I2GTI1FG = 0:

$$P_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z1}} \times \frac{f_{\text{ADC}}}{4096} = (\text{REACTENERGY}) \times k_{I1} \times k_{V1} \text{ [W]} \quad (61)$$

I2GTI1FG = 1:

$$P_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z2}} \times \frac{f_{\text{ADC}}}{4096} = (\text{REACTENERGY}) \times k_{I2} \times k_{V2} \text{ [W]} \quad (62)$$

#### ESP430CE1A and ESP430CE1B

Format	Signed integer	±31.0
Range	0x80000000 to 0x07FFFFFFF	
Resolution	1 step <sup>2</sup> = 1/C <sub>Z</sub> = 1/C <sub>Z1</sub> = 1/C <sub>Z2</sub>	

#### Formulas

I2GTI1FG = 0:

$$(\text{REACTENERGY}) = \sum_{n=0}^{4095} \frac{(\text{WAVEFSI1}_n \times \text{WAVEFSV1}_{n-1}) \times (\text{WAVEFSI1}_{n-1} \times \text{WAVEFSV1}_n)}{2 \times \sin(2\pi \times \frac{256}{\text{MAINS PERIOD}})}$$

$$W_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z1}} = (\text{REACTENERGY}) \times k_{I1} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]} \quad (63)$$

I2GTI1FG = 1:

$$\begin{aligned}
 (\text{REACTENERGY}) &= \sum_{n=0}^{4095} \frac{(\text{WAVEFSI2}_n \times \text{WAVEFSV1}_{n-1}) \times (\text{WAVEFSI2}_{n-1} \times \text{WAVEFSV1}_n)}{2 \times \sin(2\pi \times \frac{256}{\text{MAINSPERIOD}})} \\
 W_{\text{react}} &= \frac{(\text{REACTENERGY})}{C_{Z2}} = (\text{REACTENERGY}) \times k_{I2} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]}
 \end{aligned} \tag{64}$$

The average reactive power of the last 4096 measurements is:

I2GTI1FG = 0:

$$P_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z1}} \times \frac{f_{\text{ADC}}}{4096} = (\text{REACTENERGY}) \times k_{I1} \times k_{V1} \text{ [W]} \tag{65}$$

I2GTI1FG = 1:

$$P_{\text{react}} = \frac{(\text{REACTENERGY})}{C_{Z2}} \times \frac{f_{\text{ADC}}}{4096} = (\text{REACTENERGY}) \times k_{I2} \times k_{V2} \text{ [W]} \tag{66}$$

### 2.13.6 APPENERGY: Apparent Energy

The calculated apparent energy of the last 4096 measurements is stored in APPENERGY. This value also represents the average apparent power  $P_{\text{app}}$  over the same measurement time.

(APPENERGY = APPENERGY\_HI, APPENERGY\_LO = 32 bits)

I2GTI1FG determines if the apparent energy is calculated for  $I_1$  or  $I_2$ . The larger current is always used for the calculation of APPENERGY.

- I2GTI1FG = 0:  $I_1$  RMS = IRMS and V1RMS are used for the calculation
- I2GTI1FG = 1:  $I_2$  RMS = IRMS and V1RMS are used for the calculation

Format	Signed integer	±31.0
Range	0x80000000 to 0x07FFFFFFF	
Resolution	1 step <sup>2</sup> = 1/C <sub>Z</sub> = 1/C <sub>Z1</sub> = 1/C <sub>Z2</sub>	

#### Formulas

Apparent energy (ESP430CE1):

$$(\text{APPENERGY}) = (\text{V1RMS}) \times (\text{IRMS}) \text{ [steps}^2\text{]} \tag{67}$$

Apparent energy (ESP430CE1A and ESP430CE1B):

$$(\text{APPENERGY}) = \sqrt{(\text{REACTENERGY})^2 + (\text{ACTENERGY})^2} \tag{68}$$

I2GTI1FG = 0:

$$W_{\text{app}} = \frac{(\text{APPENERGY})}{C_{Z1}} = (\text{APPENERGY}) \times k_{I1} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]} \tag{69}$$

I2GTI1FG = 1:

$$W_{\text{app}} = \frac{(\text{APPENERGY})}{C_{Z2}} = (\text{APPENERGY}) \times k_{I2} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \text{ [Ws]} \tag{70}$$

Average apparent power:

I2GTI1FG = 0:

$$P_{\text{app}} = \frac{(\text{APPENERGY})}{C_{Z1}} \times \frac{f_{\text{ADC}}}{4096} = (\text{APPENERGY}) \times k_{I1} \times k_{V1} \text{ [W]} \tag{71}$$

I2GTI1FG = 1:

$$P_{\text{app}} = \frac{(\text{APPENERGY})}{C_{Z2}} \times \frac{f_{\text{ADC}}}{4096} = (\text{APPENERGY}) \times k_{I2} \times k_{V2} \text{ [W]} \tag{72}$$



### 2.13.7 ACTENSPERx: I<sub>x</sub> Active Energy Over One Mains Period

The calculated active energy of I<sub>x</sub> during the last mains period is stored in ACTENSPERx, where x = 1 or 2 for I<sub>1</sub> or I<sub>2</sub>, respectively. ACTENSPERx is calculated with each leading edge zero crossing of the mains voltage and is useful for calibration purposes. The availability of the latest calculated result is indicated by WFSRDYFG after ZXLDFFG = 1.

(ACTENSPERx = ACTENSPERx\_HI, ACTENSPERx\_LO = 32 bits)

#### ESP430CE1A and ESP430CE1B

The compensation value (CORRCOMPStore) for the common mode influence is corrected with the measured mains period at address MAINSPERIOD and subtracted from the calculated active energy 1. The compensation value is zero if the common mode compensation is switched off ((CORRCOMP) = 0). For (CORRCOMPStore) the value of the last 4096 samples is used: the new value is not yet available.

Format	Signed integer	±31.0
Range	0x80000000 to 0x07FFFFFFF	
Resolution	1 step <sup>2</sup> = 1/C <sub>Zx</sub>	

#### Formulas

Energy during last mains period:

$$W_{xSP} = \frac{(\text{ACTENSPERx})}{C_{Zx}} \text{ [Ws]} \quad (73)$$

Power during last mains period:

$$\begin{aligned} P_x &= \frac{(\text{ACTENSPERx})}{C_{Zx} \times T_{\text{mains}}} = (\text{ACTENSPERx}) \times k_{ix} \times k_{V1} \times \frac{4096}{f_{\text{ADC}}} \times f_{\text{MAINS}} = \\ &= (\text{ACTENSPER1}) \times k_{ix} \times k_{V1} \times \frac{4096 \times 256}{(\text{MAINSPERIOD})} \text{ [W]} \end{aligned} \quad (74)$$

Jitter of the energy value in ACTENSPERx is small when voltage and current have constant values and is due to the small uncertainty of the measured energy near the zero crossing of the voltage. The jitter (e) coming from this uncertainty for PF = 1 is:

$$e = \frac{\pm \left( \sin \left( \frac{f_{\text{mains}}}{f_{\text{ADC}}} \times 360^\circ \right) \right)^2}{\frac{f_{\text{ADC}}}{f_{\text{mains}}} \times 2} \quad (75)$$

For f<sub>mains</sub> = 50 Hz and f<sub>ADC</sub> = 4096 Hz the resulting jitter e (relative to 1.0) is:

$$e = \pm \frac{\left( \sin \left( \frac{50}{4096} \times 360^\circ \right) \right)^2}{\frac{4096}{50} \times 2} = \pm \frac{(\sin 4.39453)^2}{81.92 \times 2} = \pm 143.34 \text{Ex}10^{-6} \quad (76)$$

---

#### NOTE: Treatment of Negative Energy

When negative active energy is measured, ACTENSPERx is not set to zero. The measured energy is calculated and provided in the appropriate return register.

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### 2.13.8 POWERFCT: Power Factor

The calculated power factor of the last 4096 measurements is stored in POWERFCT. I2GTI1FG determines if the power factor is calculated for  $I_1$  or  $I_2$ . The larger current channel is always used for the calculation.

- I2GTI1FG = 0: ACTENERGY1 and APPENERGY are used for the calculation
- I2GTI1FG = 1: ACTENERGY2 and APPENERGY are used for the calculation

Format	Unsigned integer.fraction	+1.14
Range	0x00 to 0x4000	0.0 to 1.000
Resolution	$61.035 \times 10^{-6}$	$2^{-14}$

#### Formulas

$$(\text{POWERFCT}) = \frac{(\text{ACTENERGYx})}{(\text{APPENERGY})}$$

$$\text{PF} = (\text{POWERFCT}) \times 2^{-14} \quad (77)$$

#### Example

POWERFCT contains the calculated value 0x2ABC. The corresponding power factor PF is:

$$\text{PF} = 0x2ABC \times 2^{-14} = 0.66772 \quad (78)$$

For a pure sinusoid,  $\text{PF} = \cos\phi$ . This results in:

$$\phi = \arccos(\text{PF}) = \arccos(0.66772) = 48.108^\circ \quad (79)$$

---

**NOTE:** The sign of the angle is indicated by the value in CAPIND.

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**NOTE:** Power Factor Angle

The sign of the calculated angle is indicated by the value in CAPIND.

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**NOTE:** ESP430CE1A and ESP430CE1B

The nature of the angle  $\phi$  (inductive or capacitive load) can be seen in (REACTENERGY). The reactive energy is negative for capacitive loads and positive for inductive loads.

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### 2.13.9 CAPIND: Capacitive and Inductive Indication

The average phase shift during the last 4096 measurements is stored in CAPIND. With each leading-edge zero crossing of  $V_1$ , the phase shift between the selected current  $I_x$  and  $V_1$  is calculated where  $x = 1$  or  $2$  for  $I_1$  or  $I_2$ , respectively. I2GTI1FG determines if CAPIND is calculated for  $I_1$  or  $I_2$ . The larger current of the last 4096 measurements is always used for the calculation.

If the current lags the voltage (inductive phase shift), an internal counter decrements. If the current leads the voltage (capacitive phase shift), the counter increments. For a zero phase shift the counter is not changed. The internal counter value is written to CAPIND after 4096 measurements and reset.

Format	Signed word	$\pm 15.0$
Range	0x8000 to 0x7FFF	-32768 to +32767
Resolution	1 mains cycle	

#### Formulas

If (CAPIND) > 0 : capacitive phase shift

If (CAPIND) = 0 : no phase shift

If (CAPIND) < 0 : inductive phase shift

#### Example

CAPIND contains the value 0xFFFFE ( $-0x2$ ). This indicates a small average inductive phase shift during the last 4096 measurements. This is normally caused by power factors close to 1.0. The corresponding power factor is contained in POWERFCT.

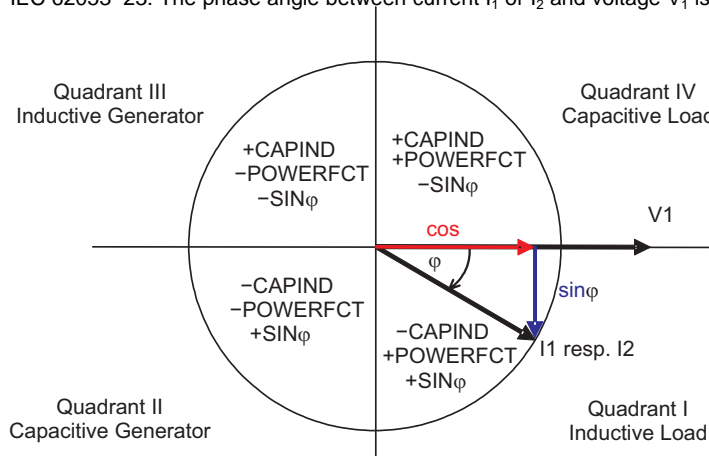
### 2.13.10 Inductive and Capacitive Indication

Energy measurement for the full 360° range of  $\phi$  is possible with NEx = 10b (see Table 12).

**Table 12. Four Quadrant Energy Measurement IEC 62053–23**

CAPIND	POWERFCT	sin	Quadrant	Energy	Reactive Energy <sup>(1)</sup>
Negative	Positive	Positive	I	Inductive load	Positive
Negative	Negative	Positive	II	Capacitive generator	Positive
Positive	Negative	Negative	III	Inductive generator	Negative
Positive	Positive	Negative	IV	Capacitive load	Negative

- <sup>(1)</sup> The sign of  $\sin\phi$  shows the sign of the involved reactive power.  
 ESP430CE1: The reactive power (REACTENERGY) is an absolute value (always positive).  
 ESP430CE1A: The reactive power (REACTENERGY) is a signed value with the sign of  $\sin\phi$ .  
 IEC 62053–23: The phase angle between current  $I_1$  or  $I_2$  and voltage  $V_1$  is defined to be positive in the clockwise direction.



### ESP430CE1A and ESP430CE1B

The average phase sequence during the last 4096 measurements is stored in word CAPIND: with each leading zero crossing of the mains voltage, the phase shift between the selected current  $I_x$  and voltage  $V_1$  is calculated. The flag I2GTI1FG decides if CAPIND is calculated for current  $I_1$  or current  $I_2$ . This means the higher current of the last 4096 measurements is used for the calculation. I2GTI1FG is not present in the ESP430CE1B.

- I2GTI1FG = 0:  $I_1$  is used for the calculation
- I2GTI1FG = 1:  $I_2$  is used for the calculation

If the current lags the voltage (inductive phase shift) an internal counter is decremented, if the current leads the voltage (capacitive phase shift), the counter is incremented. If the phase shift is zero, the counter is not changed.

The check for leading or lagging of the current is made with each leading zero voltage crossing of voltage  $V_1$ .

The counter is written to word CAPIND after 4096 measurements and then cleared. Flags NE0 and NE1 indicate the update of (CAPIND).

Format	Signed integer	+15.0
Range	$\pm f_{\text{mains}} \times 4096 / f_{\text{ADC}}$	-264 to +264 ( $f_{\text{mains}} = 66 \text{ Hz}$ , $f_{\text{ADC}} = 1024 \text{ Hz}$ )
Resolution	1 mains cycle	

### Formulas

If (CAPIND) > 0: Capacitive phase shift

If (CAPIND) = 0: No phase shift (resistive)

If (CAPIND) < 0: Inductive phase shift

### Example

(CAPIND) contains the value 0xFFFE (-2). This indicates a small average inductive phase shift during the last second. This is normally caused by power factors  $\cos\phi$  very near to 1.0. The corresponding  $\cos\phi$  is contained in word POWERFCT.

#### 2.13.11 MAINSPERIOD: Calculated Mains Period

The mains period  $T_{\text{mains}}$  is calculated and stored in MAINSPERIOD. The value for MAINSPERIOD is measured between two leading-edge zero crossings of  $V_1$  and is updated for each mains period.

Format	Unsigned integer	+15.0
Range	0x00 to 0x7FFF	0 to +32767
Resolution	1 ESP430 time base unit	

### Formulas

$$T_{\text{mains}} = (\text{MAINSPERIOD}) \times \frac{1}{f_{\text{ADC}} \times 256} \text{ [s]} \quad (80)$$

### Example

MAINSPERIOD contains the value 0x5050 where  $f_{\text{ADC}} = 4096 \text{ Hz}$  (1 ESP430 time base unit =  $2^{-20} \text{ s} = 954 \text{ ns}$ ). The corresponding mains period  $t_{\text{mains}}$  is:

$$t_{\text{mains}} = 0x5050 \times 2^{-20} = 19.607 \text{ [ms]} \quad (81)$$

This equals a mains frequency of approximately 51Hz.

#### 2.13.12 V1RMS: $V_1$ RMS Voltage

The value in V1RMS represents the calculated RMS value of  $V_1$  for the last 4096 voltage samples. The offset corrected ADC samples given in WAVEFSV1 are used for the calculation.

Format	Unsigned integer	+15.0
Range	0x00 to 0x7FFF	0 to +32767
Resolution	1 step = $1 k_{V1}$	

### Formulas

$$(\text{V1RMS}) = \sqrt{\frac{1}{4096} \times \sum_{i=1}^{4096} (\text{WAVEFSV1})^2} \text{ [steps]} \quad (82)$$

$$v1_{\text{RMS}} = k_{V1} \times (\text{V1RMS}) \text{ [V]} \quad (82)$$

### Example

V1RMS contains the value 0x3BCC (15308). With  $k_{V1} = 15.365513 \times 10^{-3}$ , this corresponds to an RMS value for  $V_1$  of:

$$v1_{\text{RMS}} = 15.365513 \times 10^{-3} \times 0x3BCC = 235.22 \text{ [V]} \quad (83)$$

### 2.13.13 IRMS: I<sub>1</sub> or I<sub>2</sub> RMS Current

The value in IRMS represents the RMS value of the current I<sub>1</sub> or I<sub>2</sub> for the last 4096 measurements. The corrected ADC samples in WAVEFSI1 or WAVEFSI2 are used for the calculation. If two current sensors are used, I<sub>1</sub> RMS and I<sub>2</sub> RMS are internally calculated and compared. I2GTI1FG is set according to the result and the larger value is given in IRMS.

(IRMS = IRMS\_HI.IRMS\_LO = 32 bits)

- I<sub>1</sub> RMS ≥ I<sub>2</sub> RMS: I2GTI1FG = 0, I<sub>1</sub> RMS is stored in IRMS
- I<sub>1</sub> RMS < I<sub>2</sub> RMS: I2GTI1FG = 1, I<sub>2</sub> RMS is stored in IRMS

Format	Unsigned integer.fraction	+15.2
Range	0x0.0 to 0x07FFF.C000	0.0 to +32767.75
Resolution	0.25 steps = 0.25 k <sub>ix</sub>	

#### Formulas

I2GTI1FG = 0:

$$(\text{IRMS}) = \sqrt{\frac{1}{4096} \times \sum_{i=1}^{4096} (\text{WAVEFSI1})^2} \text{ [steps]}$$

$$i1_{\text{RMS}} = k_{i1} \times (\text{IRMS}) \text{ [A]} \quad (84)$$

I2GTI1FG = 1:

$$(\text{IRMS}) = \sqrt{\frac{1}{4096} \times \sum_{i=1}^{4096} (\text{WAVEFSI2})^2} \text{ [steps]}$$

$$i2_{\text{RMS}} = k_{i2} \times (\text{IRMS}) \text{ [A]} \quad (85)$$

#### Example

IRMS contains the value 0x5A1C4 (23068.25). For k<sub>i1</sub> = 2.21946x10<sup>-3</sup>, this corresponds to an RMS value for I<sub>1</sub> of:

$$i1_{\text{RMS}} = 2.21946 \times 10^{-3} \times 0x5A1C4 = 51.2 \text{ [A]} \quad (86)$$

### ESP430CE1A and ESP430CE1B

#### Voltage V<sub>1</sub> is in range:

The values of the apparent energy (APPENERGY) and the RMS value of voltage V<sub>1</sub> (V1RMS) are used for the calculation of I<sub>1RMS</sub>, without regard to I<sub>2RMS</sub>. If two current sensors are in use, the flag I2GTI1FG defines for which current the RMS value is calculated:

- If I2GTI1FG = 0 (I<sub>1RMS</sub>) is stored in (IRMS)
- If I2GTI1FG = 1 (I<sub>2RMS</sub>) is stored in (IRMS)

For a better resolution the 16 bits of the fractional part are stored, too. The (IRMS) value is used for the start current detection. Flags NE0 and NE1 indicate the update of (IRMS).

Format	Unsigned Integer.Fraction	+15.16 in two words
Range	0x0.0 to 0x07FFF.FFFF	0.0 to +32767.99
Resolution	2 <sup>-16</sup> steps	

**Formulas**

$$I_{sRMS} = \sqrt{\frac{\sum_{n=0}^{4095} i_{sn}^2}{4096}} \text{ [A]} \quad \text{Definition}$$

$$(\text{IRMS}) = \frac{(\text{APPENERGY})}{(\text{V1RMS})} \text{ [steps]} \quad I_{sRMS} = (\text{IRMS}) \times K_{Is} \text{ [A]}$$

$$I_{sRMS} = \frac{I_{spp}}{2} \times \sqrt{0.5} \text{ [A]} \quad \text{For sinusoidal currents} \quad (87)$$

**When voltage  $V_1$  is very low or missing**

The summed, absolute values of  $I_1$  and  $I_2$  (representing the mean values of  $I_1$  and  $I_2$ ) are used for the calculation of  $I_{1RMS}$  and  $I_{2RMS}$ . If two current sensors are in use, the flag I2GTI1FG is defined by the two summed-up values of ( $I_{1mean}$ ) and ( $I_{2mean}$ ):

- If ( $I_{1mean}$ )  $\geq$  ( $I_{2mean}$ ): I2GTI1FG = 0 ( $I_{1mean}$ ) is used for the calculation
- If ( $I_{1mean}$ ) < ( $I_{2mean}$ ): I2GTI1FG = 1 ( $I_{2mean}$ ) is used for the calculation

The calculation of (IRMS) despite missing  $V_1$  allows the CPU an emergency mode.

**Formulas**

$$(\text{IRMS}) = \frac{\pi}{2\sqrt{2}} \times (I1mean) = \frac{\pi}{2\sqrt{2}} \times \frac{\sum_{n=0}^{4095} |I_{1n}|}{4096} \text{ [steps]} \quad \text{I2GTI1FG} = 0$$

$$(\text{IRMS}) = \frac{\pi}{2\sqrt{2}} \times (I2mean) = \frac{\pi}{2\sqrt{2}} \times \frac{\sum_{n=0}^{4095} |I_{2n}|}{4096} \text{ [steps]} \quad \text{I2GTI1FG} = 1 \quad (88)$$

---

**NOTE:** The factor  $\pi/(2\sqrt{2})$  (1.11072) converts the mean value of a sine wave to the RMS value.

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**ESP430CE1B**

In addition, on the ESP430CE1B, current measurement using the following formula is available (see [Table 15](#)).

$$(\text{IRMS\_2}) = \sqrt{\frac{1}{4096} \times \sum_{i=1}^{4096} (\text{WAVEFS1})^2} \text{ [steps]}$$

$$i1_{RMS} = k_{I1} \times (\text{IRMS\_2}) \text{ [A]} \quad (89)$$

### 2.13.14 VPEAK: V<sub>1</sub> Peak Voltage

The value in VPEAK is the absolute maximum ADC value for V<sub>1</sub> measured during the last mains period. The existing V<sub>1</sub> peak value is overwritten only if three larger contiguous samples are taken. The offset corrected value in WAVEFSV1 is used for the comparison.

Format	Unsigned integer	+15.0
Range	0x00 to 0x07FFF	0 to +32767
Resolution	1 step = 1 k <sub>V1</sub>	

#### Formulas

$$v1_{\text{peak}} = k_{V1} \times (\text{VPEAK}) \text{ [V]} \quad (90)$$

### 2.13.15 IPEAK: I<sub>1</sub> or I<sub>2</sub> Peak Current

The value in IPEAK is the absolute maximum ADC value for I<sub>1</sub> or I<sub>2</sub> measured during the last mains period. The peak values are calculated independently for both I<sub>1</sub> and I<sub>2</sub>. The internal peak values are overwritten only if three larger contiguous samples are taken. I2GTI1FG defines which I<sub>x</sub> value is written to IPEAK after the leading-edge zero crossing of V<sub>1</sub>:

- I2GTI1FG = 0: Internal I<sub>1</sub> peak value is written to IPEAK
- I2GTI1FG = 1: Internal I<sub>2</sub> peak value is written to IPEAK

Format	Unsigned integer	+15.0
Range	0x00 to 0x07FFF	0 to +32767
Resolution	1 step = 1 k <sub>I1</sub> (or 1 k <sub>I2</sub> )	

#### Formulas

I2GTI1FG = 0:

$$i1_{\text{peak}} = k_{I1} \times (\text{IPEAK}) \text{ [A]} \quad (91)$$

I2GTI1FG = 1:

$$i2_{\text{peak}} = k_{I2} \times (\text{IPEAK}) \text{ [A]} \quad (92)$$

### 2.13.16 LINECYCLCNT: Line Cycle Count

The number of mains frequency periods is accumulated in LINECYCLCNT. The counter is updated with the leading-edge zero crossing of V<sub>1</sub> (LINECYCLCNT = LINECYCLCNT\_HI, LINECYCLCNT\_LO = 32-bit value).

Format	Unsigned integer	+32.0
Range	0x00 to 0xFFFFFFFF	0 to 4.295E+9
Resolution	1 mains cycle	

#### Example

LINECYCLCNT contains the value 0xFE4567 indicating 16,663,911 mains cycles occurred since the last overflow. This is equivalent to 92 hours, 34 minutes and 38 seconds for  $f_{\text{mains}} = 50$  Hz.



### 2.13.17 NMBMEAS: ADC Conversion Count

The counter NMBMEAS accumulates the number of measurements since last being cleared by the CPU or ESP430 depending on MB. NMBMEAS increments at the rate given by  $f_{ADC}$ .

- MB = 0: NMBMEAS counts up with each measurement and rolls over after reaching 0xFFFFFFFF. Counting restarts at zero.
- MB = 1: When NMBMEAS reaches the value stored in INTRPTLEVL, ILREACHEDFG is set. Counting restarts at zero.

Format	Unsigned integer	+32.0
Range	0x0 to 0xFFFFFFFF	0 to 4.295E+9
Resolution	1 measurement	

## 2.14 ESP430CE1A Calibration

Single-point and dual-point meter calibration are possible using the ESP430. When single point calibration is used, the slope (GAINCORR1 and GAINCORR2) is calibrated. When dual-point calibration is required, the offset (POFFSET1 and POFFSET2) is calculated in addition to the slope.

To determine the slope and offset constants for a given meter, two calibration methodologies are implemented in the ESP430:

- Calibration over a defined number of mains periods (Calibration Mode)
- Calibration using continuous measurements (Measurement Mode)

### 2.14.1 Calibration Over a Defined Number of Mains Periods

This calibration method uses the internal calculations for the products of WAVEFSV1 × WAVEFSI1 and WAVEFSV1 × WAVEFSI2. These numbers are 16 times smaller than the energy values in ACTENERGY1 and ACTENERGY2. The values in ACTENERGY1 and ACTENERGY2 are adapted to the meter constants  $C_{Z1}$  and  $C_{Z2}$ . The smaller energy results allow for a longer calibration execution time.

The calibration sequence is given by the following flow:

- Configure CURR\_I2 according to the desired configuration.
- parameter registers are initialized for the load point measured by the CPU.
- The ESP430 is set to Calibration mode by the CPU.
- Calibration begins on the next leading-edge zero crossing of  $V_1$ . After measurement for the number of mains periods defined by CALCYCLCNT, the calculated active energy is stored in ACTENERGY1 and ACTENERGY2.
- The flag CALRDY is set indicating the available measurement results. The same flow is repeated for the second calibration point if required.

#### Formulas

Calibration is performed during CALCYCCNT mains periods with the two currents  $I_{1HI}$  and  $I_{1LO}$ . The nominal energy results for the two calibration points are:

$$n_{Hcalc} = C_{Z1} \times I_{1HI} \times V_1 \times PF \times \frac{(CALCYCCNT)}{f_{MAINS}} \times \frac{f_{ADC}}{2^{16}} \text{ [steps}^2\text{]}$$

$$n_{LOcalc} = C_{Z1} \times I_{1LO} \times V_1 \times PF \times \frac{(CALCYCCNT)}{f_{MAINS}} \times \frac{f_{ADC}}{2^{16}} \text{ [steps}^2\text{]}$$
(93)

The resulting values for the slope and offset are:

Slope:

$$(\text{GAINCORR1}) = \frac{n_{\text{Hlcalc}} - n_{\text{LOcalc}}}{n_{\text{Hlmeas}} - n_{\text{LOmeas}}} \times 2^{14} \quad (94)$$

Offset:

$$(\text{POFFSET1}) = \frac{n_{\text{Hlmeas}} \times n_{\text{LOcalc}} - n_{\text{LOmeas}} \times n_{\text{Hlcalc}}}{n_{\text{Hlmeas}} - n_{\text{LOmeas}}} \times \frac{f_{\text{MAINS}}}{(\text{CALCYCCNT})} \times \frac{2^{16}}{f_{\text{ADC}}} \quad (95)$$

Where:

$n_{\text{Hlcalc}}$  = Calculated energy at the high current calibration point [steps<sup>2</sup>]

$n_{\text{Hlmeas}}$  = Measured energy at the high current calibration point [steps<sup>2</sup>]

$n_{\text{LOcalc}}$  = Calculated energy at the low current calibration point [steps<sup>2</sup>]

$n_{\text{LOmeas}}$  = Measured energy at the low current calibration point [steps<sup>2</sup>]

The above formulas shown for  $I_1$  are also valid for  $I_2$ . For single point calibration, the “LO” parameters should be set to 0 in the gain correction equation.

### Example

The  $I_1$  path is calibrated with the following values (meter constants are assumed):

$$V_1 = 230 \text{ V}$$

$$I_{1\text{HI}} = 20 \text{ A}$$

$$I_{1\text{LO}} = 1 \text{ A}$$

$$\text{PF} = 1.0$$

$$\text{CALCYCCNT} = 20$$

$$f_{\text{ADC}} = 4096 \text{ Hz}$$

$$f_{\text{mains}} = 50 \text{ Hz}$$

The nominal measurement results  $n_{\text{Hlcalc}}$  and  $n_{\text{LOcalc}}$  are:

$$\begin{aligned} n_{\text{Hlcalc}} &= 29,322.80806 \times 20.0 \times 230 \times 1.0 \times \frac{20}{50} \times \frac{4096}{2^{16}} = \\ &= 3,372,122.927 = 0x0033,745B \text{ [steps}^2\text{]} \\ n_{\text{LOcalc}} &= 29,322.80806 \times 1.0 \times 230 \times 1.0 \times \frac{20}{50} \times \frac{4096}{2^{16}} = \\ &= 168,606.146 = 0x0002,929E \text{ [steps}^2\text{]} \end{aligned} \quad (96)$$

The measurement results for the two calibration points  $I_{1\text{LO}}$  and  $I_{1\text{HI}}$  are:

$$n_{1\text{Hlmeas}} = 0x32F0A2 \text{ (-1.0\% error compared to } n_{1\text{Hlcalc}} = 0x33745B)$$

$$n_{1\text{LOmeas}} = 0x29FCA \text{ (+2.0\% error compared to } n_{1\text{LOcalc}} = 0x2929E)$$

For the above results, the rounded slope written to GAINCORR1 is:

$$\begin{aligned} (\text{GAINCORR1}) &= \frac{0x0033,745B - 0x0002,929E}{0x0032,F0A2 - 0x0002,9FCA} \times 2^{14} = \\ &= 1.01171 \times 2^{14} = 0x40C0 \end{aligned} \quad (97)$$

The offset written to POFFSET1 is:

$$\begin{aligned} (\text{POFFSET1}) &= \frac{0x32,F0A2 \times 0x2,929E - 0x2,9FCA \times 0x33,745B}{0x32,F0A2 - 0x2,9FCA} \times \frac{50}{20} \times \frac{2^{16}}{4096} \\ &= -215,465 = 0xFFFC,B657 \end{aligned} \quad (98)$$

The calculated value in POFFSET1 is the offset for each product  $\text{WAVEFSV1} \times \text{WAVEFSI1}$  and ranges from -230 to +230 (-109 to +109).

If the measured calibration points are corrected with the calculated slope and offset:

$$n_{\text{corr}} = (n_{\text{meas}} \times (\text{GAINCORR1})) \times 2^{-14} + (\text{P1OFFSET}) \times \frac{\text{CALCYCCNT}}{f_{\text{MAINS}}} \times \frac{f_{\text{ADC}}}{2^{16}}$$

$$n_{\text{Hicorr}} = 0x32, F0A2 \times 0x40C0 \times 2^{-14} + 0xFFFC, B657 \times \frac{20}{50} \times \frac{4096}{2^{16}} =$$

$$= 3, 372, 137 = 0x0033, 7469$$

$$n_{\text{Locorr}} = 0x2, 9FCA \times 0x40C0 \times 2^{-14} + 0xFFFC, B657 \times \frac{20}{50} \times \frac{4096}{2^{16}} =$$

$$= 168, 607 = 0x2, 929F \quad (99)$$

### 2.14.2 Calibration Using Continuous Measurements

The CPU initializes the ESP430 for normal measurement (Measurement Mode). The energy values written after each mains period to ACTENSPER1 (and ACTENSPER2 if enabled) can be converted by the CPU into a proportional, constant output frequency containing information for the mean value of the measured energy. Timer\_A can be used for the generation of the energy-proportional output frequency.

The calibration sequence is (repeat for two-point calibration):

- Configure CURR\_I2 according to the desired configuration.
- parameter registers are initialized for the load point measured by the CPU
- The ESP430 is set to Measurement Mode by the CPU
- The first result in ACTENSPER1 (and ACTENSPER2 if enabled) should be ignored, due to the possibility of calculating over a partial mains period. Each subsequent result in ACTENSPER1 (and ACTENSPER2) is used for the calculations for the required number of mains cycles.
- Energy results for the last mains period are available in ACTENSPER1 and ACTENSPER2. This is indicated by ZXLDYFG and WFSRDYFG.
- The CPU resets WFSRDYFG and processes the results with the following equations.

#### Formulas

Calibration is performed for a single or multiple mains periods with the two currents  $I_{1\text{HI}}$  and  $I_{1\text{LO}}$ . The nominal energy results for the two calibration points are:

$$n_{\text{Hicalc}} = C_{Z1} \times I_{1\text{HI}} \times V_1 \times \text{PF} \times \frac{(\text{CALCYCCNT})}{f_{\text{MAINS}}} \times \frac{f_{\text{ADC}}}{4096} \text{ [steps}^2\text{]}$$

$$n_{\text{LOcalc}} = C_{Z1} \times I_{1\text{LO}} \times V_1 \times \text{PF} \times \frac{(\text{CALCYCCNT})}{f_{\text{MAINS}}} \times \frac{f_{\text{ADC}}}{4096} \text{ [steps}^2\text{]} \quad (100)$$

The resulting values for the slope and offset are:

Slope:

$$(\text{GAINCORR1}) = \frac{n_{\text{Hicalc}} - n_{\text{LOcalc}}}{n_{\text{Hlmeas}} - n_{\text{LOmeas}}} \times 2^{14} \quad (101)$$

Offset:

$$(\text{POFFSET1}) = \frac{n_{\text{Hlmeas}} \times n_{\text{LOcalc}} - n_{\text{LOmeas}} \times n_{\text{Hicalc}}}{n_{\text{Hlmeas}} - n_{\text{LOmeas}}} \times \frac{f_{\text{MAINS}}}{(\text{CALCYCCNT})} \times \frac{4096}{f_{\text{ADC}}} \quad (102)$$

**Example**

$I_1$  is calibrated with the following values (meter constants are assumed):

$$V_1 = 230 \text{ V}$$

$$I_{1HI} = 20 \text{ A}$$

$$I_{1LO} = 1 \text{ A}$$

$$PF = 1.0$$

$$CALCYCCNT = 1$$

$$f_{ADC} = 2048 \text{ Hz}$$

$$f_{mains} = 50 \text{ Hz}$$

The nominal measurement results  $n_{HIcalc}$  and  $n_{LOcalc}$  are:

$$\begin{aligned} n_{HIcalc} &= 29,322.80806 \times 20.0 \times 230 \times 1.0 \times \frac{1}{50} \times \frac{2048}{4096} = \\ &= 1,348,849.171 = 0x14,94F1 \text{ [steps}^2\text{]} \end{aligned}$$

$$\begin{aligned} n_{LOcalc} &= 29,322.80806 \times 1.0 \times 230 \times 1.0 \times \frac{1}{50} \times \frac{2048}{4096} = \\ &= 67,442.458 = 0x1,0772 \end{aligned} \tag{103}$$

The measurement results for the two calibration points  $I_{1LO}$  and  $I_{1HI}$  are:

$$n_{1HImeas} = 0x146040 \text{ (-1.0\% error compared to } n_{1HIcalc} = 0x1494F1\text{)}$$

$$n_{1LOmeas} = 0x10CB7 \text{ (+2.0\% error compared to } n_{1LOcalc} = 0x10772\text{)}$$

With the above results the rounded slope in GAINCORR1 is:

$$\begin{aligned} (\text{GAINCORR1}) &= \frac{0x14,94F1 - 0x1,0772}{0x14,6040 - 0x1,0CB7} \times 2^{14} = \\ &= 1.01171 \times 2^{14} = 0x40C0 \end{aligned} \tag{104}$$

The offset in P1OFFSET1 is:

$$\begin{aligned} (\text{POFFSET1}) &= \frac{0x14,6040 \times 0x1,0772 - 0x1,0CB7 \times 0x14,94F1}{0x14,6040 - 0x1,0CB7} \times \frac{50}{1} \times \frac{4096}{2048} = \\ &= -215,489 = 0xFFFC, B63F \end{aligned} \tag{105}$$

If the measured calibration points are corrected with the calculated slope and offset:

$$\begin{aligned} n_{corr} &= (n_{meas} \times (\text{GAINCORR1})) \times 2^{-14} + (\text{P1OFFSET1}) \times \frac{\text{CALCYCCNT}}{f_{MAINS}} \times \frac{f_{ADC}}{4096} \\ n_{HIcorr} &= 0x14,6040 \times 0x40C0 \times 2^{-14} + 0xFFFC, B63F \times \frac{1}{50} \times \frac{2048}{4096} = \\ &= 1,348,890 = 0x0014,951A \\ n_{LOcorr} &= 0x1,0CB7 \times 0x40C0 \times 2^{-14} + 0xFFFC, B63F \times \frac{1}{50} \times \frac{2048}{4096} = \\ &= 67,441 = 0x1,0771 \end{aligned} \tag{106}$$

The resulting error for both corrections is  $+3.1 \times 10^{-5}$  or 31 ppm.

When compared to calibration over a defined number of mains periods, the larger resulting error for calibration using continuous measurements is due to the smaller return register results caused by measurement over only one mains period. Using additional cycles minimizes this error.

### 3 ESP430CE1, ESP430CE1A, and ESP430CE1B Registers

Table 13, Table 14, and Table 15 list the ESP430 registers.

**Table 13. Control Registers**

Register	Acronym	Register Type	Address	Initial State After PUC
ESP430CE1 Control	ESPCTL	Read/write	0150h	0x00
Mailbox Control	MBCTL	Read/write	0152h	0x00
Incoming Mailbox 0	MBIN0	Read	0154h	0x00
Incoming Mailbox 1	MBIN1	Read	0156h	0x00
Outgoing Mailbox 0	MBOUT0	Write	0158h	0x00
Outgoing Mailbox 1	MBOUT1	Write	015Ah	0x00

**Table 14. Parameter Registers<sup>(1)</sup>**

Register	Acronym	Register Type	Address	Initial State After PUC
ESP430 Control 0	ESP430_CTRL0	Read/write	N/A	0x00
Event Message Enable	EVENT	Read/write	N/A	0x00
I <sub>1</sub> Phase Correction	PHASECORR1	Read/write	N/A	0x00
I <sub>2</sub> Phase Correction <sup>(2)</sup>	PHASECORR2	Read/write	N/A	0x00
V <sub>1</sub> Offset Correction	V1OFFSET	Read/write	N/A	0x00
I <sub>1</sub> Offset Correction	I1OFFSET	Read/write	N/A	0x00
I <sub>2</sub> Offset Correction <sup>(2)</sup>	I2OFFSET	Read/write	N/A	0x00
I <sub>1</sub> Adaptation Factor	ADAPTI1	Read/write	N/A	0x00
I <sub>2</sub> Adaptation Factor <sup>(2)</sup>	ADAPTI2	Read/write	N/A	0x00
V <sub>1</sub> x I <sub>1</sub> Gain Correction	GAINCORR1	Read/write	N/A	0x00
V <sub>1</sub> x I <sub>1</sub> Offset Correction LSW	POFFSET1_LO	Read/write	N/A	0x00
V <sub>1</sub> x I <sub>1</sub> Offset Correction MSW	POFFSET1_HI	Read/write	N/A	0x00
V <sub>1</sub> x I <sub>2</sub> Gain Correction <sup>(2)</sup>	GAINCORR2	Read/write	N/A	0x00
V <sub>1</sub> x I <sub>2</sub> Offset Correction LSW <sup>(2)</sup>	POFFSET2_LO	Read/write	N/A	0x00
V <sub>1</sub> x I <sub>2</sub> Offset Correction MSW <sup>(2)</sup>	POFFSET2_HI	Read/write	N/A	0x00
Energy Overflow LSW	INTRPTLEVL_LO	Read/write	N/A	0x00
Energy Overflow MSW	INTRPTLEVL_HI	Read/write	N/A	0x00
Calibration Cycle Count	CALCYCLCNT	Read/write	N/A	0x00
I <sub>1</sub> , I <sub>2</sub> Meter Threshold LSW	STARTCURR_FRAC	Read/write	N/A	0x00
I <sub>1</sub> , I <sub>2</sub> Meter Threshold MSW	STARTCURR_INT	Read/write	N/A	0x00
Mains Nominal Frequency	NOMFREQ	Read/write	N/A	0x00
V <sub>1</sub> Drop Cycle Counter	VDROPCYCLS	Read/write	N/A	0x00
I <sub>1</sub> :I <sub>2</sub> Tamper Ratio <sup>(2)</sup>	RATIOTAMP	Read/write	N/A	0x00
I <sub>1</sub> I <sub>2</sub> Tamper Level <sup>(2)</sup>	ITAMP	Read/write	N/A	0x00
V <sub>1</sub> Drop Level Threshold	VDROPLEVEL	Read/write	N/A	0x00
V <sub>1</sub> Peak Level Threshold	VPEAKLEVEL	Read/write	N/A	0x00
I <sub>1</sub> , I <sub>2</sub> Peak Level Threshold	IPEAKLEVEL	Read/write	N/A	0x00
DC Removal Period Count	DCREMPER	Read/write	N/A	0x00
	DELTAV1MAX <sup>(2)</sup>	Read/write	N/A	0x00
	CORRCOMP <sup>(2)</sup>	Read/write	N/A	0x00
	FADCU <sup>(2)</sup>	Read/write	N/A	0x00

<sup>(1)</sup> All parameter registers are accessed using the mailbox registers and are not mapped within the memory space of the CPU.

<sup>(2)</sup> Present only in devices with the ESP430CE1A and ESP430CE1B.

**Table 15. Return Registers**

Register	Acronym	Register Type	Address	Initial State After PUC
ESP430 Status 0	ESP430_STAT0	Read	01C0h	0x00
ESP430 Status 1 <sup>(1)</sup>	ESP430_STAT1	Read	01C2h	0x00
V <sub>1</sub> Waveform Sample	WAVEFSV1	Read	01C4h	0x00
I <sub>1</sub> Waveform Sample	WAVEFSI1	Read	01CAh	0x00
I <sub>2</sub> Waveform Sample <sup>(2)</sup>	WAVEFSI2	Read	01CCh	0x00
I <sub>1</sub> Active Energy LSW	ACTENERGY1_LO	Read	01D0h	0x00
I <sub>1</sub> Active Energy MSW	ACTENERGY1_HI	Read	01D2h	0x00
I <sub>2</sub> Active Energy LSW <sup>(2)</sup>	ACTENERGY2_LO	Read	01D4h	0x00
I <sub>2</sub> Active Energy MSW <sup>(2)</sup>	ACTENERGY2_HI	Read	01D6h	0x00
Reactive Energy LSW	REACTENERGY_LO	Read	01D8h	0x00
Reactive Energy MSW	REACTENERGY_HI	Read	01DAh	0x00
Apparent Energy LSW	APPENERGY_LO	Read	01DCh	0x00
Apparent Energy MSW	APPENERGY_HI	Read	01DEh	0x00
I <sub>1</sub> Active Energy Per Cycle LSW	ACTENPER1_LO	Read	01E0h	0x00
I <sub>1</sub> Active Energy Per Cycle MSW	ACTENPER1_HI	Read	01E2h	0x00
I <sub>2</sub> Active Energy Per Cycle LSW <sup>(2)</sup>	ACTENPER2_LO	Read	01E4h	0x00
I <sub>2</sub> Active Energy Per Cycle MSW <sup>(2)</sup>	ACTENPER2_HI	Read	01E6h	0x00
I <sub>1</sub> RMS_2 LSW Result <sup>(3)</sup>	IRMS_2_LO	Read	01E4h	0x00
I <sub>1</sub> RMS_2 MSW Result <sup>(3)</sup>	IRMS_2_HI	Read	01E6h	0x00
Power Factor	POWERFCT	Read	01E8h	0x00
Capacitive and Inductive Cycle Counter	CAPIND	Read	01EAh	0x00
Mains Line Cycle Period	MAINSPERIOD	Read	01ECh	0x00
V <sub>1</sub> RMS Result	V1RMS	Read	01EEh	0x00
I <sub>x</sub> RMS LSW Result	IRMS_LO	Read	01F0h	0x00
I <sub>x</sub> RMS MSW Result	IRMS_HI	Read	01F2h	0x00
V <sub>1</sub> Peak Result	VPEAK	Read	01F4h	0x00
I <sub>x</sub> Peak Result	IPEAK	Read	01F6h	0x00
Line Cycle Counter LSW Result	LINECYCLCNT_LO	Read	01F8h	0x00
Line Cycle Counter MSW Result	LINECYCLCNT_HI	Read	01FAh	0x00
Measurement Counter LSW Result	NMBMEAS_LO	Read	01FCh	0x00
Measurement Counter MSW Result	NMBMEAS_HI	Read	01FEh	0x00

<sup>(1)</sup> Present only in devices with the ESP430CE1A and ESP430CE1B

<sup>(2)</sup> Not present in the ESP430CE1B

<sup>(3)</sup> Present in the ESP430CE1B only

### 3.1 ESPCTL, ESP430 Control Register

**Figure 7. ESPCTL Register**

15	14	13	12	11	10	9	8
ESPLOOP	Reserved						
rw-0	r-0	r-0	r-0	r-0	r-0	r-0	rw-0
7	6	5	4	3	2	1	0
Reserved				ESPISW	Reserved	ESPSUSP	ESPEN
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

**Table 16. ESPCTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ESPLOOP	RW	0	Loop-back enable. Allows writing to the normally "read-only" return registers when EN = 0. 0 = Loop mode disabled 1 = Loop mode enabled
14-9	Reserved	R	0	Reserved
8-4	Reserved	RW	0	Reserved
3	ESPISW	RW	0	Interrupt switch enable. This bit controls the routing of shared module interrupts (SD16 and hardware multiplier) when ESPSUSP = 1. Modifying ESPISW clears the interrupt enable bits of each shared module. 0 = Interrupts routed to the ESP430 and serviced when ESPSUSP = 0 1 = Interrupts routed to the CPU
2	Reserved	RW	0	Reserved
1	ESPSUSP	RW	0	ESP430 module suspend 0 = ESP430 active 1 = ESP430 activity halted
0	ESPEN	RW	0	ESP430 module enable 0 = ESP430 disabled 1 = ESP430 enabled

### 3.2 MBCTL, Mailbox Control Register

**Figure 8. MBCTL Register**

15	14	13	12	11	10	9	8
Reserved				OUT1IE	OUT0IE	OUT1IFG	OUT0IFG
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
CLR1OFF	CLR0OFF	IN1IE	IN0IE	OUT1FG	OUT0FG	IN1IFG	IN0IFG
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

**Table 17. MBCTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0	Reserved
11	OUT1IE	RW	0	Outgoing Mailbox 1 interrupt enable 0 = Interrupt disabled 1 = Interrupt enabled
10	OUT0IE	RW	0	Outgoing Mailbox 0 interrupt enable 0 = Interrupt disabled 1 = Interrupt enabled
9	OUT1IFG	RW	0	Outgoing Mailbox 1 interrupt flag. This bit is set when OUT1IFG is cleared indicating the message in MBOU1 has been processed by the ESP430. OUT1IFG is cleared when a message is written to MBOU1 or by software. 0 = No interrupt pending 1 = Interrupt pending
8	OUT0IFG	RW	0	Outgoing Mailbox 0 interrupt flag. This bit is set when OUT0IFG is cleared indicating the message in MBOU0 has been processed by the ESP430. OUT0IFG is cleared when a message is written to MBOU0 or by software. 0 = No interrupt pending 1 = Interrupt pending
7	CLR1OFF	RW	0	Incoming Mailbox 1 interrupt flag auto-clear disable. 0 = IN1IFG is automatically cleared when MBIN1 is read by the CPU 1 = IN1IFG must be cleared in software by the CPU
6	CLR0OFF	RW	0	Incoming Mailbox 0 interrupt flag auto-clear disable. 0 = IN0IFG is automatically cleared when MBIN0 is read by the CPU 1 = IN0IFG must be cleared in software by the CPU
5	IN1IE	RW	0	Incoming Mailbox 1 interrupt enable 0 = Interrupt disabled 1 = Interrupt enabled
4	IN0IE	RW	0	Incoming Mailbox 0 interrupt enable 0 = Interrupt disabled 1 = Interrupt enabled
3	OUT1FG	RW	0	Outgoing Mailbox 1 flag. This bit is set when a message is written to MBOU1 and is cleared after it has been processed by the ESP430.
2	IN1IFG	RW	0	Outgoing Mailbox 0 flag. This bit is set when a message is written to MBOU0 and is cleared after it has been processed by the ESP430.
1	IN1IFG	RW	0	Incoming Mailbox 1 interrupt flag. This bit is set when a new message is available in MBIN1. 0 = No interrupt pending 1 = Interrupt pending
0	IN0IFG	RW	0	Incoming Mailbox 0 interrupt flag. This bit is set when a new message is available in MBIN0. 0 = No interrupt pending 1 = Interrupt pending



### 3.3 MBIN0, Incoming Command Mailbox Register

**Figure 9. MBIN0 Register**

15	14	13	12	11	10	9	8
Incoming Command							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Incoming Command							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

### 3.4 MBIN1, Incoming Data Mailbox Register

**Figure 10. MBIN1 Register**

15	14	13	12	11	10	9	8
Incoming Data							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Incoming Data							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

### 3.5 MBOUT0, Outgoing Command Mailbox Register

**Figure 11. MBOUT0 Register**

15	14	13	12	11	10	9	8
Outgoing Command							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Outgoing Command							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

### 3.6 MBOUT1, Outgoing Data Mailbox Register

**Figure 12. MBOUT1 Register**

15	14	13	12	11	10	9	8
Outgoing Data							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Outgoing Data							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

### 3.7 ESP430\_CTRL0, ESP430 Control Parameter Register

**Figure 13. ESP430\_CTRL0 Register**

15	14	13	12	11	10	9	8
Reserved						I2CMRR	V1FILTER
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
DCREM_I2	DCREM_I1	DCREM_V1	NE1	NE0	MB	CURR_I1	CURR_I2
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

**Table 18. ESP430\_CTRL0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-10	Reserved	RW	0	Reserved
9	I2CMRR	RW	0	Switches the common-mode rejection function for current $I_2$ . 0 = Disabled 1 = Enabled Present only in the ESP430CE1A. Reserved in other devices.
8	V1FILTER	RW	0	Switches the spike filter function for voltage $V_1$ . 0 = Disabled 1 = Enabled Present only in the ESP430CE1A and ESP430CE1B.
7	DCREM_I2	RW	0	$I_2$ DC removal algorithm enable 0 = Disabled 1 = Enabled Not present in the ESP430CE1B.
6	DCREM_I1	RW	0	$I_1$ DC removal algorithm enable 0 = Disabled 1 = Enabled
5	DCREM_V1	RW	0	$V_1$ DC removal algorithm enable 0 = Disabled 1 = Enabled
4-3		RW	0	Negative active energy control select 00 = Negative active energy is set to zero 01 = Absolute active energy is used by ESP430 10 = Negative active energy is used by ESP430 11 = Reserved
2	MB	RW	0	Energy threshold select 0 = INTRPTLEVL = energy level 1 = INTRPTLEVL = measurement count
1	CURR_I1	RW	0	$I_1$ current channel sensor select 0 = $I_1$ active 1 = Reserved
0	CURR_I2	RW	0	$I_2$ current channel enable 0 = $I_2$ disabled 1 = $I_2$ active Not present in the ESP430CE1B.

### 3.8 EVENT, ESP430 Event Message Enable Parameter Register

**Figure 14. EVENT Register**

15	14	13	12	11	10	9	8
ACTIVEME	Reserved		I2PEAKME	I1PEAKME	VPEAKME	VDROPME	NEGENME
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
TAMPME	CALRDYME	ZXTRME	ZXLDME	ENRDYME	ILREACHEDME	I2GT1ME	WFSRDYME
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

**Table 19. EVENT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ACTIVEME	RW	0	ACTIVEFG message enable 0 = Disabled 1 = Enabled
14-13	Reserved	RW	0	Reserved
12	I2PEAKME	RW	0	I2PEAKFG message enable 0 = Disabled 1 = Enabled Not present in the ESP430CE1B.
11	I1PEAKME	RW	0	I1PEAKFG message enable 0 = Disabled 1 = Enabled
10	VPEAKME	RW	0	VPEAKFG message enable 0 = Disabled 1 = Enabled
9	VDROPME	RW	0	VDROPFG message enable 0 = Disabled 1 = Enabled
8	NEGENME	RW	0	NEGENFG message enable 0 = Disabled 1 = Enabled
7	TAMPME	RW	0	TAMPFG message enable 0 = Disabled 1 = Enabled Not present in the ESP430CE1B.
6	CALRDYME	RW	0	CALRDYFG message enable 0 = Disabled 1 = Enabled
5	ZXTRME	RW	0	ZXTRFG message enable 0 = Disabled 1 = Enabled
4	ZXLDME	RW	0	ZXLDFG message enable 0 = Disabled 1 = Enabled
3	ENRDYME	RW	0	ENRDYFG message enable 0 = Disabled 1 = Enabled
2	ILREACHEDME	RW	0	ILREACHEDFG message enable 0 = Disabled 1 = Enabled

**Table 19. EVENT Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
1	I2GTI1ME	RW	0	I2GTI1FG message enable 0 = Disabled 1 = Enabled Not present in the ESP430CE1B.
0	WFSRDYME	RW	0	WFSRDYFG message enable 0 = Disabled 1 = Enabled

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**NOTE: Remaining Parameter Registers**

See [Section 2.8](#) for descriptions of the rest of the parameter registers. These registers represent 8-bit or 16-bit values and do not contain individual bit definitions.

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### 3.9 ESP430\_STAT0, ESP430 Status Return Register 0

**Figure 15. ESP430\_STAT0 Register**

15	14	13	12	11	10	9	8
ACTIVEFG	Reserved		I2PEAKFG	I1PEAKFG	VPEAKFG	VDROPFG	NEGENFG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
TAMPFG	CALRDYFG	ZXTRFG	ZXLDFG	ENRDYFG	ILREACHEDFG	I2GTI1FG	WFSRDYFG
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

**Table 20. ESP430\_STAT0 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ACTIVEFG	R	0	ESP430 status flag 0 ESP430 is in IDLE mode 1 ESP430 is in ACTIVE mode
14-13	Reserved	R	0	Reserved
12	I2PEAKFG	R	0	I <sub>2</sub> over-current flag. I2PEAKFG is set when the peak I <sub>2</sub> current measured exceeds IPEAKLEVEL for three or more consecutive samples. 0 = Line normal 1 = Line overcurrent detected Not present in the ESP430CE1B.
11	I1PEAKFG	R	0	I <sub>1</sub> over-current flag. I1PEAKFG is set when the peak I <sub>1</sub> current measured exceeds IPEAKLEVEL for three or more consecutive samples. 0 = Line normal 1 = Line over-current detected
10	VPEAKFG	R	0	V <sub>1</sub> over-voltage flag. VPEAKFG is set when the peak V <sub>1</sub> voltage measured exceeds VPEAKLEVEL for three or more consecutive samples. 0 = Line normal 1 = Line over-voltage detected
9	VDROPFG	R	0	V <sub>1</sub> under-voltage flag. VDROPF is set when the peak V <sub>1</sub> voltage measured is less than VDROPLEVEL for the number of consecutive mains cycles defined by VDROPCYCLS. VDROPF is also set if V1RMS is less than 0.088 x VDROPLEVEL to insure notification if V <sub>1</sub> = 0 and no zero crossings occur. Maximum response time is 2 seconds. 0 = Line normal 1 = Line under-voltage detected
8	NEGENFG	R	0	Negative energy flag. Negative energy sum calculated over the last 4096 samples. 0 = Event message sent if NEGENME = 1 or CLR_EVENT command issued by CPU 1 = Negative energy detected
7	TAMPFG	R	0	Tampered meter flag. Tamper detection is monitored at a frequency of f <sub>ADC</sub> /4096 (for example, 1 Hz for f <sub>ADC</sub> = 4096 Hz). 0 = Normal operation 1 = Potential tamper condition detected Not present in the ESP430CE1B.
6	CALRDYFG	R	0	Calibration ready flag. 0 = Event message sent if CALRDYME = 1, CLR_EVENT command issued by CPU or ESP430 set into Idle mode. 1 = Calibration cycle complete, new values ready in ACTENERGYx.
5	ZXTRFG	R	0	V <sub>1</sub> zero crossing, trailing-edge flag (negative-going zero crossing). 0 = Leading-edge zero crossing occurred 1 = Trailing edge zero crossing occurred
4	ZXLDFG	R	0	V <sub>1</sub> zero crossing, leading-edge flag (positive-going zero crossing). 0 = Trailing-edge zero crossing occurred 1 = Leading-edge zero crossing occurred

**Table 20. ESP430\_STAT0 Register Field Descriptions (continued)**

Bit	Field	Type	Reset	Description
3	ENRDYFG	R	0	Energy ready flag. Indicates update of V1RMS, IRMS, ACTENERGYx, REACTENERGY, APPENERGY, POWERFCT and CAPIND registers. 0 = Event message sent if ENRDYME = 1 or CLR_EVENT command issued by CPU 1 = Updated results available
2	ILREACHEDFG	R	0	Interrupt energy level reached flag. 0 = Event message sent if ILREACHEDME = 1 or CLR_EVENT command issued by CPU 1 = Interrupt level reached as defined by MB and INTRPTLEVL
1	I2GTI1FG	R	0	I <sub>2</sub> greater than I <sub>1</sub> flag. 0 = I <sub>1</sub> RMS > I <sub>2</sub> RMS during last 4096 measurements 1 = I <sub>2</sub> RMS > I <sub>1</sub> RMS during last 4096 measurements Not present in the ESP430CE1B.
0	WFSRDYFG	R	0	Waveform samples ready flag. Indicates update of WAVEFSV1 and WAVEFSIx registers. Values are offset-corrected and updated at f <sub>ADC</sub> . 0 = Event message sent if WFSRDYME = 1 or CLR_EVENT command issued by CPU 1 = Updated results available

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**NOTE: Remaining Return Registers**

See [Section 2.13](#) for descriptions of the remaining return registers. These registers represent 8-bit or 16-bit values and do not contain individual bit definitions.

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### 3.10 ESP430\_STAT1, ESP430 Status Return Register 1

This register is present only in devices with ESP430CE1A and ESP430CE1B.

**Figure 16. ESP430\_STAT1 Register**

15	14	13	12	11	10	9	8
Reserved			I2PEAKNEGFG	I1PEAKNEGFG	V1PEAKNEGF G	Reserved	
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Reserved					ILNEGFG	Reserved	
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

**Table 21. ESP430\_STAT1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0	Reserved
12	I2PEAKNEGFG	R	0	Indicates the sign of the measured $I_2$ peak. The bit is not reset by sending an event message or with the command CLR_EVENT. 0 = Last $I_2$ peak was positive 1 = Last $I_2$ peak was negative Not present in the ESP430CE1B.
11	I1PEAKNEGFG	R	0	Indicates the sign of the measured $I_1$ peak. The bit is not reset by sending an event message or with the command CLR_EVENT. 0 = Last $I_1$ peak was positive 1 = Last $I_1$ peak was negative
10	V1PEAKNEGFG	R	0	Indicates the sign of the measured $V_1$ peak. The bit is not reset by sending an event message or with the command CLR_EVENT. 0 = Last $V_1$ peak was positive 1 = Last $V_1$ peak was negative
9-3	Reserved	R	0	Reserved
2	ILNEGFG	R	0	Indicates the sign of the energy of the reached Interrupt Level. Set if the energy of the reached interrupt level is negative. Reset if the energy of the reached interrupt level is positive. It is not reset by sending an event message or with the command CLR_EVENT. 0 = Energy is positive 1 = Energy is negative
1-0	Reserved	R	0	Reserved

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## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from August 5, 2008 to October 18, 2018

**Page**

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- Formatting and editorial changes throughout document, including changes to section numbering ..... 1
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