Texas Instruments

TSW1100 User's Guide

User's Guide

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Introduction

Texas Instrument's TSW1100 allows for high speed digital data capture from TI's high speed, high resolution analog to digital converters (ADC). It comes complete with software allowing the user to quickly evaluate TI's ADCs without the need for expensive logic analyzers and complex analysis routines. The TSW1100 features data capture speeds of up to 170MSPS and data capture depths of up to 16 bits by 1 million points deep. It can operate in dual channel mode allowing simultaneous capture of a dual channel ADC. Data is transferred via USB interface allowing easy PC control and it requires only one power supply for operation.

1.1 Features

- ADC Digital Data Capture
- Simplifies high speed ADC evaluation
- 1 MB capture depth at 170MSPS
- 16 bit support
- Single channel or dual channel operation
- Synchronous dual channel data capture
- Trigger data capture
- Operation off a single wall-mount DC power supply
- USB interface to PC
- Software that computes ADC performance
- Ability to save and recall data sets
- Embedded Logic Analyzer mode
- Field Upgradeable

1.2 Required Setup

- PC with USB and a screen resolution 1024 $\times$ 768
- 12V DC power supply
- Compatible TI ADC EVM

Software Installation

2.1 Minimum Requirements

Before installing the software please verify that your PC will meet the following minimum requirements:

- Microsoft™ Windows 2000, or XP operating system
- 1024 x 768 screen resolution
- USB 1.1 compatible input

Other configurations may work, however they remain untested. Users should be advised that when capturing larger data set, PC equipped with the latest processors and ample memory tend to perform best.

2.2 Installing the ADC Capture Tool

Upon inserting the CD into the PC, Windows should automatically start the installation process. If for some reason it does not prompt you with the install message seen in Figure 2-1, explore the contents of the CD and run setup.exe.

Figure 2-1. ADC Capture Install Screen

2.3 Installing the TSW1100 Instrument Drivers

Immediately following the installation of the ADC Capture Card software tool, the setup will prompt you to install the instrument drivers for the TSW1100. When driver installation starts you will be greeted by the screen in Figure 2-2, please accept the default values to complete the installation. Because the USB device driver is unsigned by Microsoft, the installation software will have to do an extra step to register itself with the operating system. Figure 2-3 illustrates a successful device registration.

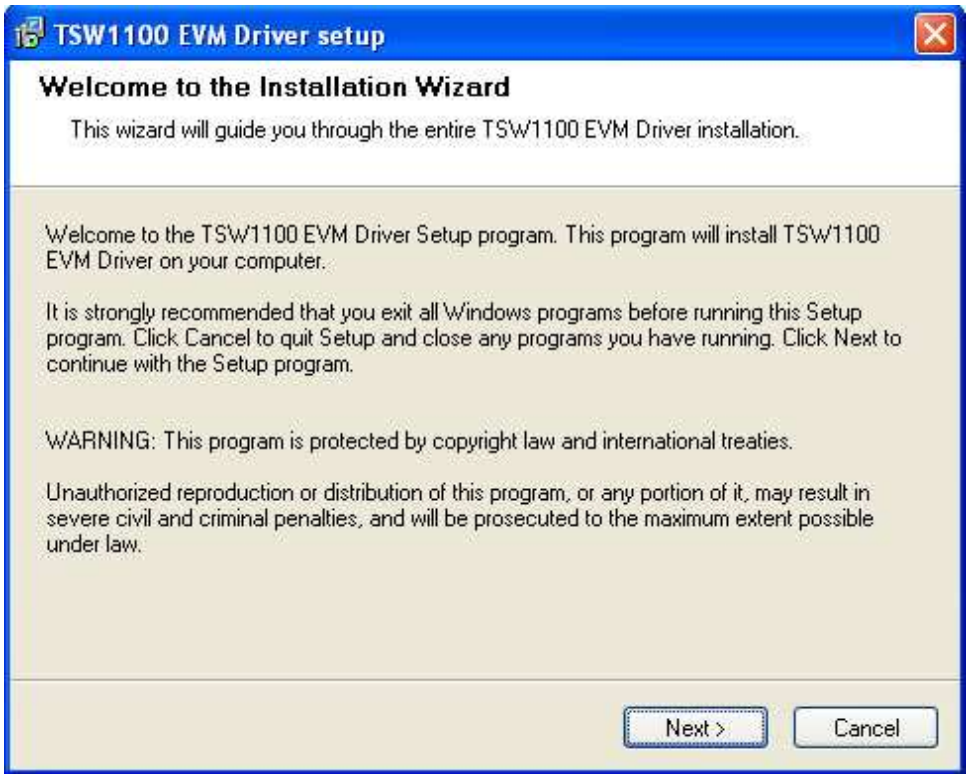

Figure 2-2. TSW1100 Driver Installation

Figure 2-3. TSW1100 Driver Registered and Ready to Use

2.4 Verifying the TSW1100 Driver Installation

Upon installation of the TSW1100 Instrument Drivers, you can quickly verify its operation by the following procedure. Without an ADC EVM attached, power on the TSW1100 by connecting a 12V DC power supply. Immediately after power up, LED D13 will briefly illuminate and turn off. Now connect a USB cable from the PC to the TSW1100. If this is your first time connecting to the device, Windows will recognize the new hardware and guide you through the final steps of setup. To verify a complete installation, open Windows Hardware Device Manager and the TSW1000 should be list under USB Devices as seen in Figure 2-4.

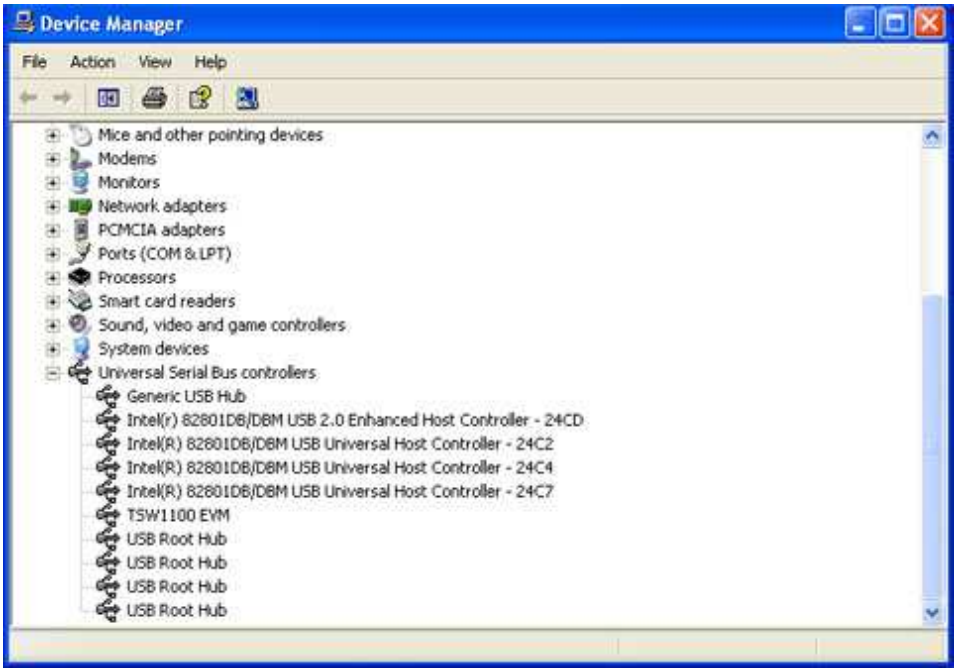

Figure 2-4. Hardware Device Manager

Startup Procedure for Successful Operation

Before connecting an ADC, please refer to the TSW1100 website to view the most up to date version of the ADC EVM compatibility list.

3.1 Connecting to a Texas Instrument's HS ADC EVM

On compatible TI ADC EVMs', connect the right angle digital data output connector to either of the TSW1100's J1 or J2. J1 connects to channel 1 of the TSW1100 while J2 connects to channel 2.

3.2 Provide power to the ADC EVM

Follow the ADC EVM User's Guide instructions and power on the ADC EVM.

3.3 Providing power to the TSW1100

You can either use a wall-mount power supply connected to J7 or you can use a lab supply that can supply a +12VDC to J8 while connecting the return to J9. Texas Instruments recommends that you set a current limit of 600mA. Power on the TSW1100.

3.4 Connecting to the USB

With the PC turned on, connect the USB cable from the PC to the TSW1100 USB connector, J10. At this point, the PC should recognize the TSW1100. To verify, you can go to the Hardware Device Manager and select USB Device and ensure the TSW1100 is listed as a USB device. You will also see the LED D13 illuminated on the TSW1100 signaling that the device has been configured properly and is communicating with the PC. If at this point LEDs D10 - D13 are illuminated, please see the troubleshooting guide found at the end of this document.

3.5 Launching the TSW1100 Software

With the TSW1100 recognized by the hardware device manager, you can open the software package. To run the program, click on Start -> Program Files -> Texas Instruments -> TI ADC Capture Card. This will launch the main program window as seen in Figure 3-1. Upon a successful connection of the TSW1100 and launch of the software, the software package will initially display the version numbers in the Status Message window.

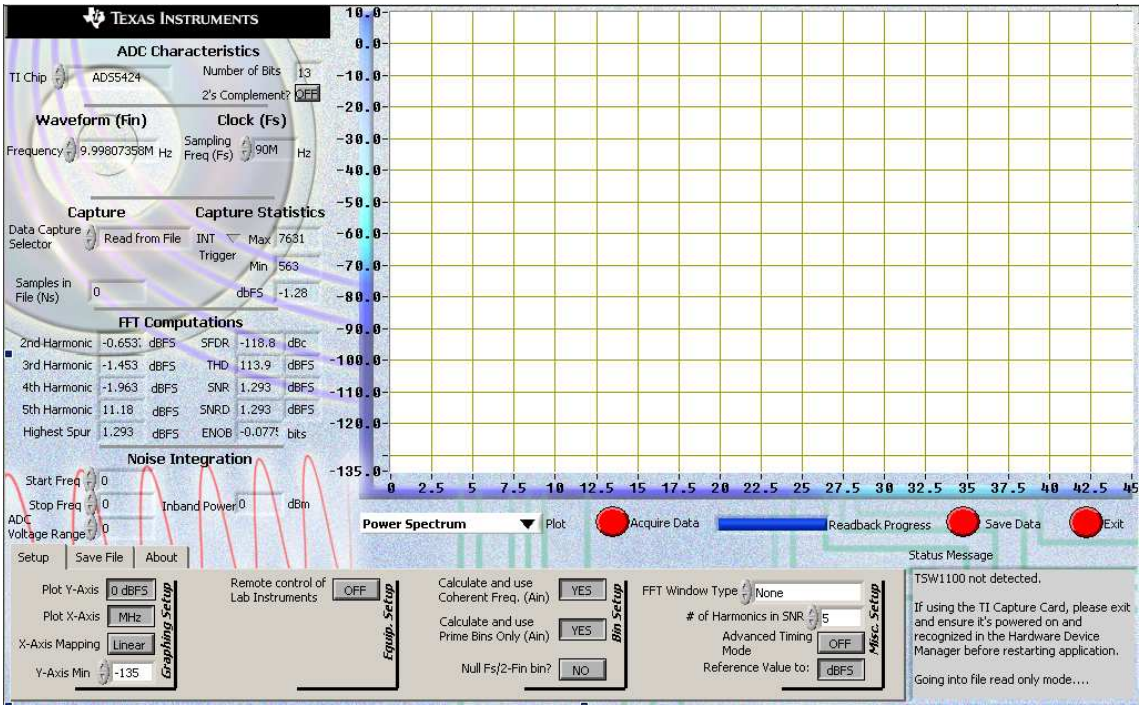

Figure 3-1. ADC Capture Card Software

Review of Software Features

4.1 Software Introduction

Accompanying the TSW1100 is a powerful software package that will allow you to operate the TSW1100 and analyze the performance of select Texas Instrument's ADCs. The ADC capture software will allow you acquire, analyze and save datasets.

4.2 Modes of Operations

The software package offers four basic modes to view the data. After you acquire a dataset by clicking on the acquire button, you can view the data in multiple formats. You can switch between these views interchangeably without the need for reacquiring data. The modes are described below in Table 4-1.

Table 4-1. Software Modes of Operation

PLOT	DESCRIPTION
Power Spectrum	Presents a power spectrum view of the acquired data. The spectrum is zoom-able for a closer inspection.
Time Domain	Presents a reconstructed time domain view of the acquired data. The data is zoom-able for closer inspection.
Unwrap Waveform	A unique view only applicable to sinusoidal coherent data capture setups. Provides a close inspection of one reconstructed period.
Logic Analyzer	Provides a look at the raw captured digital data. In this view the option is given to reorder the acquired bits.

4.3 Software Analysis Options

The TSW1100 features multiple operations that allow you to evaluate the data after you have captured a dataset. In many cases you can rearrange aspects of a dataset without having to capture a new acquisition which allows you to immediately see how a change impacts performance. In Table 4-2, you'll find a summary of key features that can be used to evaluate data after it has been captured.

Table 4-2. Software Analysis Tools

CONTROL NAME	RECALCULATES PERFORMANCE?	DESCRIPTION OF FUNCTION
2's Compliment	Yes	Ability to toggle 2's compliment decoding on an existing function.
Start Freq.	No	Start of Noise Integration Band
Stop Freq.	No	End of Noise Integration Band
ADC Voltage Range	No	ADC Full Scale input voltage range in Vpp
Plot Y-Axis	No	Ability to change the whether db or dBFS is plotted.
Plot X-Axis	No	Allows the ability to change the X-axis scale from Hz to MHz.
X-Axis Mapping	No	Allows the ability to convert X-axis scaling from a linear scale to a logarithmic scale.
Y-Axis Min	No	For FFT plots, sets the minimum to on the graphical display.

Table 4-2. Software Analysis Tools (continued)

CONTROL NAME	RECALCULATES PERFORMANCE?	DESCRIPTION OF FUNCTION
FFT Window Type	Yes	Allows the user to apply a window function to the dataset. Please note, a time domain algorithm is used for performance calculations if you select a window function.
# of Harmonics in SNR	Yes	Allows the ability to change the number of harmonics are marked on the graph, and consequently how many harmonics are excluded in the SNR calculation.
Reference Value to	Yes	Allows ability to reference performance metrics to dBFS or dBc.
D<15:0>	Yes	Only available in Logic Analyzer Mode, allows for the ability to reorder TSW1100 input bits.
Graphing Display	No	In the Power Spectrum, Time Domain and Unwrap Waveform modes, the user can change graph features such as min and max by clicking on the x and y axis numbers. In addition, the user can zoom in on a particular area by right clicking and dragging over the area of interest.

4.4 Commonly Used Software Features

4.4.1 Capture the ADC Time Domain, Perform a FFT, and Plot the Results

1. Select the ADC under evaluation – In the top left-hand corner of the user controls, find the pull-down control labeled TI Chip. Select the appropriate EVM from the list. Based off this selection, the software will automatically update the ADC Characteristic indicators: Number of Bits and 2's Compliment.
2. Configure the Input Waveform (Fin) conditions – Find the control labeled Frequency and change it to the sinusoidal frequency you would like to provide to the ADC analog input. In it's default state and for best ADC performance, the software will calculate a coherent bin based off of a prime integer and overwrites the Frequency indicator. If you are not using the Remote Control of Lab Instruments feature, then manually set your signal source output frequency to coincide with the displayed frequency.
3. Configure the ADC Sampling Frequency (Fs) conditions– Find the control labeled Sampling Rate, and set this to the value at which you want to clock the ADC.
4. Configure the TSW1100 Capture – With the understanding that J1 connects to channel 1 and J2 connects to channel 2 of the TSW1100, use the Capture control to select which channel the ADC EVM is connected to. Select the depth of capture by selecting the acquisition size in the Number of Points control.
5. Acquire Data – At this point you are ready to capture data from the ADC. You can do so by clicking on the red circular Acquire Data button located below the graph. The button will turn green and stay green until the capture is complete. After it is complete, you will see a FFT plot as well as Capture Statistics and FFT Computations.

4.4.2 Performing a Dual Channel Capture

1. Select the ADC under evaluation – In the top left-hand corner of the user controls, find the pull-down control labeled TI Chip. Select the appropriate EVM from the list. Based off this selection, the software will automatically update the ADC Characteristic indicators: Number of Bits and 2's Compliment.
2. Configure the Input Waveform (Fin) conditions – Find the control labeled Frequency and change it to the sinusoidal frequency you would like to provide to the ADC analog input. In it's default state and for best ADC performance, the software will calculate a coherent bin based off of a prime integer and overwrites the Frequency indicator. If you are not using the Remote Control of Lab Instruments feature, then manually set your signal source output frequency to coincide with the displayed frequency.
3. Configure the ADC Sampling Frequency (Fs) conditions – Find the control labeled Sampling Rate, and set this to the value at which you want to clock the ADC.
4. Configure the TSW1100 Capture – Use the Capture control to select which Chan 1 + Chan 2. Select the depth of capture by selecting the acquisition size in the Number of Points control.

5. Acquire Data – At this point you are ready to capture data from the ADC. You can do so by clicking on the red circular Acquire Data button located below the graph. After clicking the acquire button the software will wait for an external trigger, which can be applied by either depressing SW1 or providing a trigger stimulus to J5 of the TSW1100. This will synchronously capture ADC data on both channel 1 and channel 2. After it is complete, you will see a FFT plot as well as Capture Statistics and FFT Computations for the channel selected. You can view the data and performance for each channel independently.

4.4.3 Saving and Recalling Data Sets

1. Saving a data set – On the tabbed browser at the bottom, select the File Save tab. Once there make sure the File Capture Selector is set to capture a text file. You may also change the default directory path and the data format to either decimal or hexadecimal.
2. Retrieving a saved data set – On the Data Capture Selector, scroll through the list and select Read From File. Once selected, click on the red circular Acquire Data button and it will prompt you for a text file to read in. Select the appropriate text file and the saved date set will be redisplayed.
3. Performing a screen capture – Similar to saving a data set, a screen capture can be performed by the following method. First, on the tabbed browser at the bottom, select the File Save tab. Change the File Capture Selector to Screen. There are two different picture formats supported; png and jpg both of which can be selected by the Image File Type control. When you are ready to acquire the screen, click on the red circular button, Save Data.

4.5 Complete Software Overview

In Table 4-3, you'll find a complete reference of all the software features.

Table 4-3. Software Feature Descriptions

CONTROL NAME	INPUT/OUTPUT	DESCRIPTION OF FUNCTION
ADC Characteristics		
TI Chip	Input	List of compatible TI ADC EVMs.
Number of Bits	Output	Automatically populated based off of TI Chip selected.
2's Complement	Input	Automatically populated based off of TI Chip selected.
Waveform		
Frequency	Output	Based off of selections made in the Bin Setup section, this is the frequency that is actually sent to the source if Remote Control of Lab Instruments is selected. If Remote Control is not selected, manually enter this frequency into the source supplying the ADC Fin for sinusoidal evaluation setups.
Amplitude	Input	When using Remote Control of Lab Instruments, this will set the amplitude of the input waveform (Fin). Unit is dBm. Only visible if Remote Control of Lab Instruments is turned on.
Clock		
Sampling Rate	Input	ADC clock frequency (Fs). If using Remote Control of Lab Instruments this will program your AG8644 clock.
Clock Amplitude	Input	When using Remote Control of Lab Instruments, this will set the amplitude of the clock (Fs). Unit is Vrms. Only visible if Remote Control of Lab Instruments is turned on.
Capture		
Data Capture Selector	Input	Selects TSW1100 capture channel, dual channel or allows the ability to read from file.
Trigger	Input	Used in single channel capture mode, selects between Internal and External Trigger. Default is Internal trigger.
Number of Samples	Input	Selects number of samples TSW1100 will acquire during capture.
Display Channel	Input	Only visible when Data Capture Selector is set to Chan 1 + Chan 2. After dual channel capture, selects between channels 1 or 2 displayed and their corresponding performance calculations.
Capture Statistics		

Table 4-3. Software Feature Descriptions (continued)

CONTROL NAME	INPUT/OUTPUT	DESCRIPTION OF FUNCTION
Max	Output	Minimum code captured.
Min	Output	Maximum code captured.
dBFS	Output	Uses captured min code and max code to calculate decibels relative to a full scale input based off the Number of Bits the ADC has.
FFT Computations		
2nd Harmonic	Output	Amplitude of the ADC 2nd Harmonic given in dBFS.
3rd Harmonic	Output	Amplitude of the ADC 3rd Harmonic given in dBFS.
4th Harmonic	Output	Amplitude of the ADC 4th Harmonic given in dBFS.
5th Harmonic	Output	Amplitude of the ADC 5th Harmonic given in dBFS.
Highest Spur	Output	Highest Spur that is not included in the SNR calculation, given in dBFS.
SFDR	Output	Calculates the Spurious Frequency Dynamic Range based off of captured data.
THD	Output	Calculates the Total Harmonic Distortion based off of captured data.
SNR	Output	Calculates the Signal to Noise Ratio based off of capture data.
SNRD	Output	Calculates the Signal to Noise Ratio + Distortion based off of capture data.
ENOB	Output	Calculates the Effective Number of Bits based off of SNRD.
Noise Integration		
Start Freq	Input	Start of Noise Integration Band.
Stop Freq	Input	Stop of Noise Integration Band.
ADC Voltage Range	Input	
Inband Power	Output	Noise Integration result in dBm. Please note that if the fundamental is in the frequency range it is nulled out for the calculation.
Control		
Plot	Input	After acquiring a dataset, Plot selects which view to display. See Table 1 for a complete summary.
Acquire Data	Input	Begins the ADC Capture and automatically transfers the data to the PC for analysis. When the Data Capture Selector is set to Read from File and the Acquire Data is asserted this prompts the user to select a previously acquired data set stored in a text file.
Read back Progress	Output	After Acquire Data is asserted, this indicator displays the progress of the USB transfer.
Save Data	Input	Saves the current displayed data to either a screen capture or a text file for future analysis depending on the state of the File Capture Selector control.
Exit	Input	Saves the current setup state and exits the program.
Status Message	Output	Displays messages about the TSW1100 operation.
Graphing Setup		
Plot Y Axis	Input	Selects between plotting the Y axis in dB or referencing the calculation to 0 dBFS. Default = 0dBFS.
Plot X Axis	Input	Selects between Hz and MHz. Default = MHz.
X-axis Mapping	Input	Selects between a linear or logarithmic mapping of the X axis. Default = Linear.
Y-Axis Min	Input	Minimum displays Y axis amplitude level.
Equipment Setup		
Remote Control of Lab Instruments	Input	Allows for automated ADC evaluation setups that utilize GPIB control of Agilent 8644 sources. Default = Off.
Signal Generator GPIB Address	Input	GPIB value of the Signal Generator (Fin) when using Remote control of instruments. Only visible if Remote Control of Lab Instruments is turned on.

Table 4-3. Software Feature Descriptions (continued)

CONTROL NAME	INPUT/OUTPUT	DESCRIPTION OF FUNCTION
Clock Generator GPIB Address	Input	GPIB value of the Clock Generator (Fs) when using Remote control of instruments. Only visible if Remote Control of Lab Instruments is turned on.
Bin Setup		
Calculate and use Coherent Frequency	Input	Allows for calculation of a coherent bin based off of Sampling Rate, Frequency, and Number of Samples. Result of calculation will be displayed in the Frequency indicator. Default = Yes.
Calculate and use Prime Bins Only	Input	Uses prime bins only for coherent frequency calculation. For use in conjunction with Calculate and use Coherent Bins and its output is displayed in the Frequency indicator. Default = Yes.
Null Fs/2-Fin bin?	Input	Offer option to null out the bin associated with Fs/2-Fin. Default = No.
Misc Setup		
FFT Window Type	Input	Offers several window choices for FFT calculation. When using a window function, spectral performance is calculated using a time domain Fin algorithm. For coherent ADC setups, select None. Default = None.
# of Harmonics in SNR	Input	Number of harmonics used in this SNR calculation. This entry also changes the number of harmonics displayed on the graph.
Advanced Timing Mode	Input	Allows for the capture clock to be shifted with respect to the data in up to 127 increments. Default = 0.
Reference Value to	Input	Used for spectral performance calculations, refers the resulting calculation the dBFS or dBc. Default=dBFS.
Save File Tab		
File Capture Selector	Input	Selects whether the screen is capture or a test file is saved when the Save Data control is asserted. Default = Screen.
Default Directory Path	Input	Allows user to select a default directory where saved files are stored.
Text File Data Format	Input	Selects between saving data in a decimal or hex format when saving a test file. Default = Decimal.
Image file type	Input	Selects between png and jpg. Default = PNG.
Logic Analyzer Mode		
D<16:0>	Input	Only visible when in the Plot control has selected the Logic Analyzer Mode. This control allows you to reorder the data bits assigned to the input connector J1 and J2.

Review of Hardware Features

5.1 Introduction

The TSW1100 digital capture card hardware was designed to be operated in a variety of different environments. It offers a robust power management architecture which simplifying the power requirements for operation down to a single power supply. The TSW1100 offers multiple capture clock options and it allows skew adjustment between clock and data. For a complete hardware description, please consult the schematics which can be found on your hard drive in the \TI Capture Card\documentation directory.

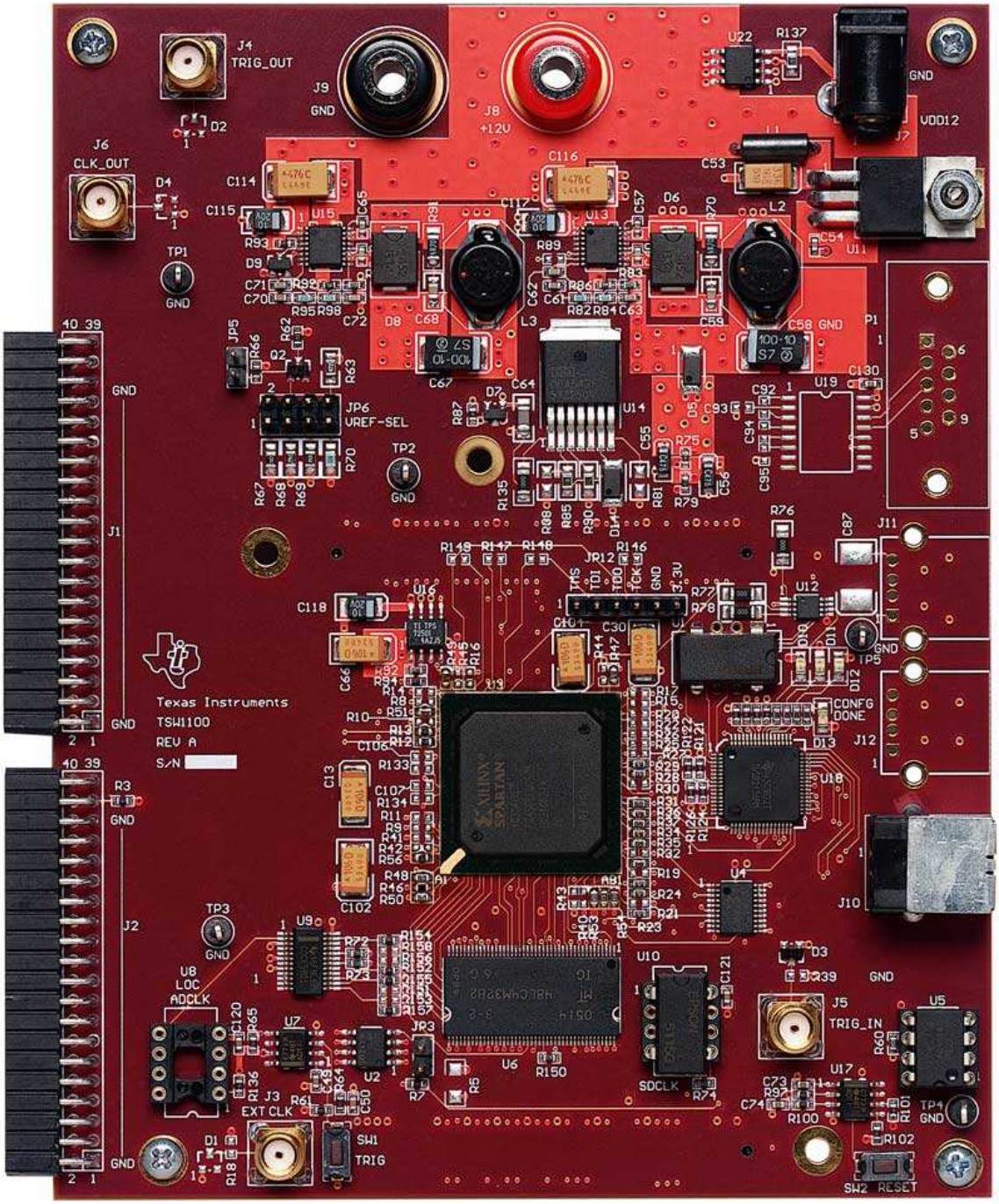

Figure 5-1. TSW1100 Hardware

5.2 FPGA

At the heart of the TSW1100 is a Xilinx Spartan 3 FPGA. The FPGA design contains 3 major features: a FIFO, a SDRAM controller, and a USB interface. Upon trigger, the FPGA will latch the data into the FIFO before being stored into the SDRAM for latter retrieval. Finally, upon a PC request, the data is retrieved and passed to the TI TUSB2136 for USB upload to the host PC.

5.3 USB interface

The USB architecture is based around a TI TUSB2136, which is a fully compliant USB 1.1 operation. It operates off of a 12MHz oscillator and makes use of an 8052 microcontroller to handle PC/FPGA requests. The microcontroller's firmware is stored on an EEPROM (U5).

5.4 Power Management

The TSW1100 accepts either +12VDC from J7 via a wall mount power supply or by using a lab power supply in which J8 is connected to +12VDC and the ground return to J9. It uses several TI TPS54350 voltage step down converters. Also featured is the TI UA7805 to provide +5VDC. In its default configuration, the power management portion of the EVM should require no user intervention.

5.5 Clock Management

5.5.1 ADC EVM Supplied Clock

For TI ADC EVMs that output a clock sometimes called Data Ready, it is preferred to use this as the capture card clock. In this scenario, the ADC EVM outputs the clock and is sent to the TSW1100 capture card on pin 2 of either J1 or J2 depending on the TSW1100 channel selected. For dual channel operation, the TSW1100 uses the clock found on channel 2, to capture both channels of data. Using the software, the user can adjust the skew between data and clock by clicking on the Advanced Timing Mode control.

5.5.2 Oscillator

In legacy applications where the ADC EVM does not supply the clock, a CMOS or TTL oscillator can be furnished by the customer and positioned at U8. The installed oscillator will provide the input frequency to a TI CDCF5801 PLL. Please consult the TSW1100 schematics and the CDCF5801 datasheet located on TI's website for device operation. The PLL provides for multiple frequency divide and multiply functions by setting the installation and removal of surface mount resistors as described in Table 5-1. The output of the PLL can be observed on J6.

Table 5-1. Local PLL Options

CDC5801 PIN	PULL-UP RESISTOR	PULL-DOWN RESISTOR
MULT1	R151	R155 (default)
MULT2	R152 (default)	R156
P2	R153	R157 (default)
P1	R154 (default)	R158
P0	GND	GND

5.5.3 External Clock

The SMA J3, reference designator EXT_CLK, is reserved for future use and is not supported.

5.6 Trigger Options

For single channel operation, by default, data is captured by using an internally fired trigger. For dual channel operation that requires data to be captured using a synchronous external trigger, two options are provided. You can use either the puss-button switch SW1 or provide a low-high (3.3V) transition on J5. The SMA J4, with reference designator Trig_Out, is reserved for future use and is not supported.

5.7 ADC Data Input

Two 40 pin right angle edge-mount connectors provide for an ADC input path. The TSW1100 channel 1 input corresponds to J1, while J2 corresponds to J2. For a full description of the pins, please refer to Table 5-2 and Table 5-3.

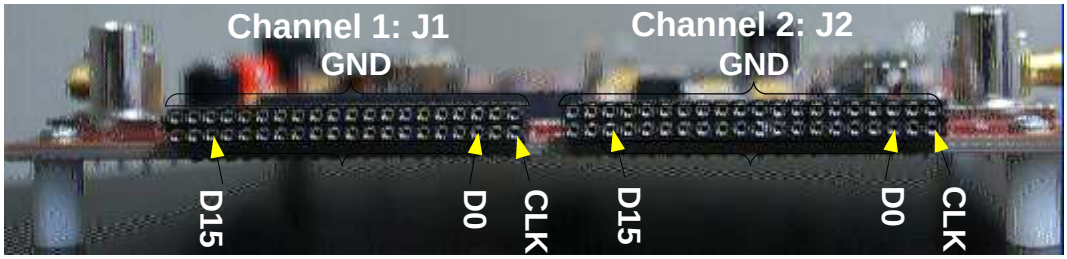

Figure 5-2. TSW1100 ADC Input Connectors

Table 5-2. Output Channel 1 Connector: J1

J1 PIN	DESCRIPTION	J1 PIN	DESCRIPTION
1	GND	21	GND
2	CLK	22	D8
3	GND	23	GND
4	NC	24	D9
5	GND	25	GND
6	D0 (LSB)	26	D10
7	GND	27	GND
8	D1	28	D11
9	GND	29	GND
10	D2	30	D12
11	GND	31	GND
12	D3	32	D13
13	GND	33	GND
14	D4	34	D14
15	GND	35	GND
16	D5	36	D15 (MSB)
17	GND	37	GND
18	D6	38	Reserved
19	GND	39	GND
20	D7	40	Reserved

Table 5-3. Output Channel 2 Connector: J2

J1 PIN	DESCRIPTION	J1 PIN	DESCRIPTION
1	GND	21	GND
2	CLK	22	D8
3	GND	23	GND
4	NC	24	D9
5	GND	25	GND
6	D0 (LSB)	26	D10
7	GND	27	GND
8	D1	28	D11

Table 5-3. Output Channel 2 Connector: J2 (continued)

J1 PIN	DESCRIPTION	J1 PIN	DESCRIPTION
9	GND	29	GND
10	D2	30	D12
11	GND	31	GND
12	D3	32	D13
13	GND	33	GND
14	D4	34	D14
15	GND	35	GND
16	D5	36	D15 (MSB)
17	GND	37	GND
18	D6	38	Reserved
19	GND	39	GND
20	D7	40	Reserved

Troubleshooting

6.1 Problem: After power up, all LEDs on the TSW1100 are illuminated and the card is not recognized.

Solution: In this situation, the TSW1100 needs to be reset. Close down the software, and reset the TSW1100 by asserting the switch located at SW2. Re-open the software package.

6.2 Problem: Software hangs after powering down the board and powering it back on.

Solution: In this situation, the TSW1100 needs to be reset. Close down the software, and reset the TSW1100 by asserting the switch located at SW2. Re-open the software package.

6.3 Problem: Software goes into read only mode and I can't get out of it even after I plug in the TSW1100.

Solution: Upon the software initialization it detects if a TSW1100 is present. If it is not present the software will go into Read File Only mode. In order to use the TSW1100, you must follow the order given by chapter 2. Please exit out of the software and first power on the TSW1100 before reopening the software package.

6.4 Problem: The software reports that I've exceeded the sampling rate of the device.

Solution: By selecting a TI chip in the software package, you are telling the TSW1100 system a little about your surrounding environment. If you set your Sampling Rate (Fs) located in the software package to a speed higher then the rated amount on the ADC under evaluation the software will warn you. The software will not let you set a sampling rate significantly above the rated maximum on the data sheet.

6.5 Problem: On large data captures it takes an long time to update the graph.

Solution: This is a know issue and it is heavily dependent on the computer memory available to it. For normal sinusoidal ADC analysis it is advisable to use 16k or 32k points.

Problem: On large data captures it takes an long time to update the graph.

Basics of ADC Measurement

While not particular to the usage of the TSW1100 data capture card, information presented in this chapter is relevant for all ADC evaluation and performance characterization.

7.1 Definitions of Measured Parameters

When a signal of frequency Fin is put into an ADC converter sampling at a frequency Fs, the result when viewed in the frequency domain (by taking an FFT of the output of the ADC) consists of the fundamental frequency, harmonics of the fundamental frequency, and noise due to quantization and other noise sources in the ADC. There are a number of figures of quality defined to describe how well the ADC reproduces the fundamental frequency while minimizing harmonic distortion and noise. This section of this document describes those figures of quality.

The figures of quality are measured using a sine wave of a certain amplitude. If a sine wave that encompasses the entire input range of the ADC, or a “full-scale” amplitude sine wave, it is defined as 0 dBFS. Subsequent test signal amplitudes are defined as a sine wave in relationship to this, for example, -1dBFS, which would be a sine wave with 89% of the full-scale amplitude. When ADC figures of merit are discussed, typically they are tested with a -1dBFS input tone, however it should be clarified when cited.

7.1.1 Spurious Free Dynamic Range (SFDR)

When looking at the spectrum of the reconstructed waveform from the ADC, the largest spike will be at the fundamental frequency or aliased frequency if greater than the Nyquist frequency. There will also be several spikes due to harmonic distortion or noise. The Spurious Free Dynamic Range (SFDR) is the difference, expressed in decibels (dBc), between the RMS amplitude of the fundamental frequency and the next largest frequency spike.

7.1.2 Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) measures the distortion provided in the reconstructed ADC signal due to harmonics of the fundamental frequency being generated by the ADC. THD does not include noise sources in the ADC, and so separates distortion in the ADC from noise generation. THD is defined as the ratio, expressed in decibels (dBc), between the RMS value of the fundamental frequency component and the RMS sum of the first several (possibly aliased) harmonics of the input frequency. Typically, the first 9 harmonics are used for the calculation.

7.1.3 Signal to Noise Ratio (SNR)

The Signal-to-Noise ratio (SNR) is the complementary measurement to the THD. Here, a ratio is taken between the RMS sum of all the noise from DC (not including DC) to Nyquist, excluding the ADC harmonics (possibly aliased) of the fundamental. That is, the RMS sum is taken over all the frequency bins that are not used in the THD calculation above, and therefore typically harmonics above the first nine are treated as noise. If one assumes that the noise is independent of the signal, then the SNR is appropriately expressed in terms of dBFS – decibels with respect to the power of a sine wave encompassing the full-scale of the ADC.

7.1.4 SNRD

Sometimes called SINAD, this measurement expresses the signal-to-noise ratio of the converter considering both harmonic distortion and noise. SNRD (signal to noise+distortion ratio) is calculated by taking the RMS sum of all components except the fundamental summed from DC (not including DC) to Nyquist divided by the power of the fundamental sine wave input.

7.1.5 Equivalent Number of Bits (ENOB)

Using either the SNR or SNRD, the equivalent number of bits of an ideal ADC can be calculated, assuming only quantization noise exists. Usually the SNRD is used.

7.2 Instrument Selection

When measuring high performance ADCs, it is important to have a setup that can reveal the true performance of the ADC such that your test setup does not influence your results.

7.2.1 Signal Source

For the selection of a signal source, there are several qualities of merit that one should look for. Phase noise, both close to the carrier and far out from the carrier should be as low as possible and be devoid of spurs. Spurious emissions must not exist or if they do exist they must be located far enough from the carrier such that they can be filtered out. A litmus test is to feed the signal source into a spectrum analyzer and verify that all spurs are indeed below the noise floor of the ADC. For best results choose a signal source with extremely low close in phase noise and use a narrow high attenuation bandpass filter centered on Fin.

7.2.2 Clock Source

In many modern high performance ADCs, the converter's S/H can accept either a sinusoidal or square wave input. In these scenarios where the ADC can accept a sinusoidal input, the comparator found at the front-end has extremely low jitter specification, or time domain uncertainty. Typically they have better jitter performance then commercially available pulse generators. Consequently, for maximum performance, it is advisable to use a sinusoidal source with extremely low phase noise with a crystal bandpass filter centered on Fs.

7.3 Coherent Sampling

This section describes the selection of the sampling and input frequencies for the ADC characterization, that allows you to use no window function. There are two requirements on these frequencies. The first is that the two frequencies be chosen so that there is no "leakage" in the FFT's spectral components. Secondly, the two frequencies are chosen so that input waveform is sampled at different phases each cycle, so that more information is added to the FFT every cycle.

Implicit in an FFT is the assumption that the signal being sampled is replicated infinitely in time before and after the sequence being sampled, and in the characterization environment this is not the case. "Leakage" results if there are discontinuities between the beginning and end of the sequence being sampled. In order to prevent leakage in the FFT, it is necessary to sample the input frequency so that the record time covers an integer number of periods of the input waveform. That is, the waveform has to be continuous when the record is duplicated forward and backward in time. The number of cycles of the input sine wave in the record is given by:

$$N_{cyc} = N_S \frac{F_S}{Fin}, \text{ where } N_{cyc} \text{ is chosen be an integer prevent spectral leakage.}$$

Selecting the number of cycles (N_{cyc}) to be an integer is called “coherent sampling.” Coherent sampling meets the first requirement of preventing FFT leakage. To meet the second requirement that the input waveform be sampled at different phases during each cycle of the input waveform, N_{cyc}/N is chosen to be an irreducible fraction – that is, N_{cyc} and N_s are chosen to be relatively prime. Since N_s is typically chosen to be a power of two so that a radix-2 FFT can be used, it suffices to choose N_{cyc} to be an odd number. The TSW1100 software can provide automatic calculation of a mutually prime coherent frequency to simplify the process of choosing Fin.

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