ADS8481EVM

This user's guide describes the characteristics, operation, and use of the ADS8481 18-bit, 1-MHz, parallel interface, analog-to-digital converter evaluation board. A complete circuit description, schematic diagram, and bill of materials are included.

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1 EVM Overview

1.1 Features

- Full-featured evaluation board for the high-speed ADS8481 18-bit, 1-MSPS, single-channel, parallel interface, SAR-type analog-to-digital converters
- Onboard signal conditioning
- Onboard reference
- Input and output digital buffers
- Onboard decoding for stacking multiple EVMs

2 Introduction

The ADS8481 is 18-bit, 1-MSPS analog-to-digital converter (ADC) with an internal 4.096-V reference and a pseudo-differential unipolar single-ended input. The device is a capacitor-based successive approximation register (SAR) converter with an inherent sample and hold. The ADS8481 has 8-bit, 16-bit, and 18-bit parallel interface bus options, allowing easy interfacing to a variety of processors.

The ADS8481EVM is an evaluation and demonstration platform for the ADS8481 ADC. The EVM board design is such that it allows the user to modify the circuits and create custom analog signal conditioning, select from reference sources and interface modes.

3 Analog Interface

The ADS8481 analog-to-digital converter has both a positive and negative analog input pin. The ADS8481EVM allows grounding the negative input pin close to the device via SJP9, shorting across the footprint of C47, or wiring in a signal separately. The negative input pin, which has a range of –200 mV up to 200 mV, is shorted to ground on the ADS8481EVM via SJP9. A signal for the positive input pin can be applied at connector P1 pin 2 (shown in Table 1) or by the center pin of SMA connector J1.

Table 1. Analog Input Connector

Description	Signal Name	Connector Pin No.		Signal Name	Description
Not connected	–	P1.1	P1.2	+	Non-inverting input channel
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Pin tied to ground	AGND	P1.9	P1.10	N/A	Reserved
Pin tied to ground	AGND	P1.11	P1.12	N/A	Reserved
Reserved	N/A	P1.13	P1.14	N/A	Reserved
Pin tied to ground	AGND	P1.15	P1.16	N/A	Reserved
Pin tied to ground	AGND	P1.17	P1.18	N/A	Reserved
	N/A	P1.19	P1.20	REF+	External reference input

3.1 Input Signal Conditioning

The analog input circuitry consisting of the THS4031 (U6) operational amplifier, allows the user to install passive components to configure it for positive or negative gains, as well as input range scaling, filtering, and leveling translation(e.g., adding a DC offset). The installed amplifier is housed in an industry standard SOIC footprint. This enables the user to replace the THS4031 with a multitude of dual- and single-supply amplifiers housed in an SOIC package. When choosing the driver amplifier, the user should consider the following requirements. The driving amplifier must be able to settle the output to an 18-bit level (0.00038%) within the sample time of the converter. It needs to have a THD performance comparable or better than the ADS8481. Lastly, the noise generated by the amplifier needs to be as low as possible, so as not to degrade the SNR performance of the ADS8481.

The noise coming through the driver amplifier is filtered by a single-pole filter using R = 12 Ω and C = 1 nF with a corner frequency of 13 MHz. The 12-Ω series resistor works with the capacitor to filter the input signal, but also isolates the amplifier from the capacitive load. The 1000-pF capacitor to ground at the input of the ADC works with the series resistor to filter the input signal, behaves like a charge reservoir, and provides a path to ground for high-frequency noise and the input current transient which occurs when the device switches from hold to sample mode. This larger external filter capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode.

The supplies to the input amplifier are selectable with solder jumper pad SJP3. When deciding on supply rails, a good rule is to add at least 2 V of head room on either side to achieve optimal performance for dual supply amplifiers. For example, if the signal applied to the amplifier is 0 V to 4 V, then the amplifier rails should be at least –2 V and +6 V. At the 16-bit and 18-bit performance nodes, the amplifier-introduced distortion can become significant if the amplifier is not given adequate headroom. Be aware when reading amplifier data sheets that they may not be specified with large amplitudes. Therefore, it may not be possible to surmise from a cursory glance how well the amplifier will behave in a system.

The default configuration from the factory is to set the input for translating a bipolar ±2-V signal to 0 V to 4 V. The necessary DC component to offset the signal is generated by U4. U4 is the low-noise THS4032 amplifier. If necessary, it can be configured to further filter the reference voltage IC, U2, and provide positive or negative gains. The ADS8481EVM leaves the factory with potentiometer, R24, set to 1.024 V.

Table 1 indicates how the solder pad jumpers should be set to select for the various supply and input options for the analog driver circuitry. The schematic for the ADS8481EVM appears in Appendix C.

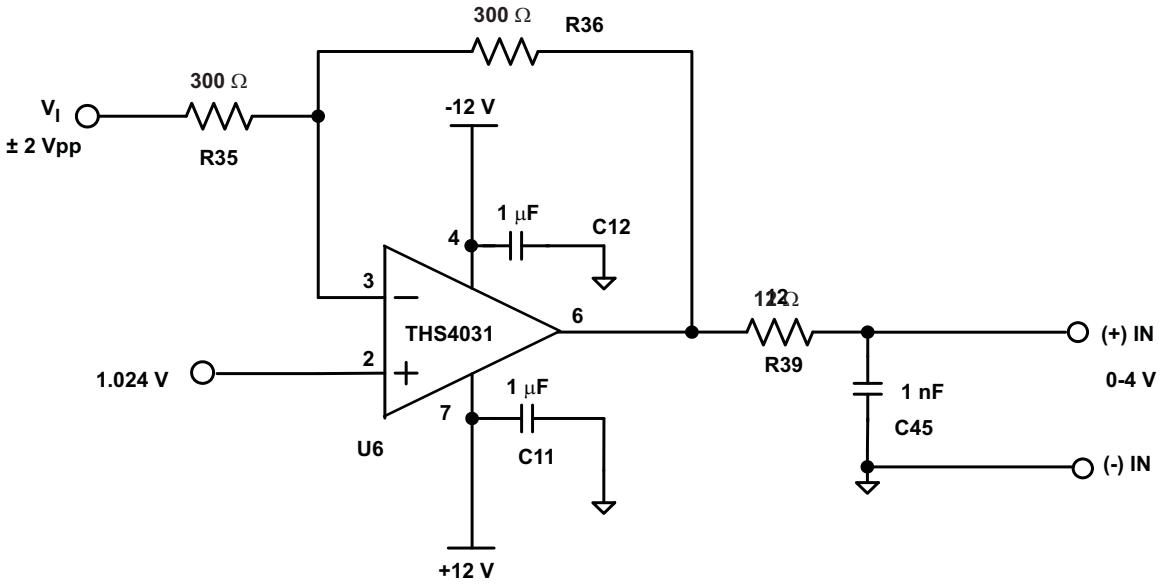


Figure 1. Input Buffer Circuit

Table 2. Analog Circuitry Jumper

Reference Designator	Description	Jumper Position	
		1-2	2-3
SJP1	Select onboard reference	**Installed** (1)	Not Installed
	Select user-supplied reference	Not Installed	Installed
SJP2	Short voltage node +DC to U6 pin 3	**Installed** (1)	N/A
SJP3	Set U6 operational amplifier minus rail supply to ground	Installed	Not installed
	Set U6 operational amplifier minus rail supply to –VCC	Not installed	**Installed** (1)
SJP4	Set U7 operational amplifier minus rail supply to ground	Installed	Not installed
	Set U7 operational amplifier minus rail supply to –VCC	Not installed	**Installed** (1)
SJP6	Set REFIN pin of ADS8481 to on-chip (internal) reference voltage.	**Installed** (1)	Not installed
	Set REFIN pin of ADS8481 to reference selected by SJP1.	Not installed	Installed
SJP7	Short voltage node –DC to U6 pin 2 via R35.	Installed	N/A
SJP8	Short voltage node +DC to U7 pin 3.	Installed	N/A
SJP9	Short –IN pin of U5 to ground at C45.	**Installed** (1)	N/A

(1) Indicates factory-installed option.

3.2 Reference

The ADS8481 can operate with an external reference voltage in the range of 3 V up to 4.2 V. It generates an on-chip 4.096-V reference voltage. The ADS8481EVM allows the user to select the external reference voltage from three sources. The first option is to use the internally generated 4.096 V from the ADC. The other two options are to select from the 3-V onboard reference (U1) or a user-supplied voltage applied at pin 20 of P1. See Table 2 for solder jumper options for selecting from the various reference sources.

The reference voltage provides the scale factor for the conversion result. The input voltage is measured against the reference voltage. It is therefore imperative that the reference voltage be clean, low noise, and well-decoupled.

The default configuration is to use the internal on-chip reference.

4 Digital Interface

The ADS8481EVM is designed for easy interfacing to multiple platforms. The digital interface input and output signals of the converter are on connectors P2, P3, and J6. These are 0.1-inch center plug and socket connectors, allowing the user to plug the ADS8481EVM onto the various motherboard interface boards from Texas Instruments, or ribbon cable onto the user development board. The following tables list the connector pinouts.

Table 3. Pinout for Parallel Control Connector P3

Description	Signal Name	Connector Pin No.		Signal Name	Description
Daughtercard Chip Select	DC_CS	P3.1	P3.2	+	Non-inverting input channel
Reserved	N/A	P3.3	P3.4	GND	Ground
Reserved	N/A	P3.5	P3.6	GND	Ground
Address line 0	A0	P3.7	P3.8	GND	Ground
Address line 1	A1	P3.9	P3.10	GND	Ground
Address line 2	A2	P3.11	P3.12	GND	Ground
Reserved	N/A	P3.13	P3.14	GND	Ground
Reserved	N/A	P3.15	P3.16	GND	Ground
Convert Start	DC_CONVST	P3.17	P3.18	GND	Ground
Interrupt pin	INTC	P3.19	P3.20	GND	Ground

Conversions are initiated on the falling edge of the Convert Start signal. It is critical when measuring large amplitude and/or high-frequency input signals that the user provide a clean, low-jitter Convert Start pulse.

The Convert Start signal can be applied to the ADS8481 from the decoder outputs or from connector P3 pin 17. Address decoder SN74ACH138 is used to generate the Read ($\overline{RD}$) and Convert Start ($\overline{CONVST}$) signals to the converter. Jumpers W3 and W4 allow the user to assign these two signals to different addresses in memory. This allows the stacking of up to two ADS8481EVMs into processor memory. See Table 4 for jumper settings. If the user applies a Convert Start signal directly on P3 pin 17, then be sure to short W6 pins 1-2. This bypasses the decoder output selected by the W4.

Note that the evaluation module does not allow the Chip Select ($\overline{CS}$) line of the converter to be assigned to different memory locations. Therefore, it is suggested that the $\overline{CS}$ line be grounded or wired to an appropriate signal of the user's processor.

Table 4. Jumper Position

Reference Designator	Description	Pin No.	
		1-2	2-3
W1	Set digital buffer supply voltage to +5 V	**Installed** (1)	Not installed
	Set digital buffer supply voltage	Not Installed	Installed
W2	Apply inverted BUSY to INTC signal to +3.3 V	**Installed** (1)	Not installed
	Apply BUSY signal to INTC signal	Not installed	Installed
W3	Set $\overline{RD}$ signal to add[0x3]	**Installed** (1)	Not installed
	Set $\overline{RD}$ signal to add[0x4]	Not installed	Installed
W4	Set $\overline{CONVST}$ signal to add[0x1]	**Installed** (1)	Not installed
	Set $\overline{CONVST}$ signal to add[0x2]	Not Installed	Installed
W5	Set $\overline{DC\_CS}$ to $\overline{CS}$ of ADS8481	**Installed** (1)	N/A
W6	Set $\overline{DC\_CONVST}$ to $\overline{CONVST}$ of ADS8481	Installed	Not installed
	Set decoder output to $\overline{CONVST}$ of ADS8481	Not installed	**Installed** (1)

(1) Indicates factory-installed option.

The data bus is available at connector P2; see Table 5 for pinout information.

Table 5. Data Bus Connector P2

Description	Signal Name	Connector Pin No.		Signal Name	Description
Data bit 0	DB0	P2.1	P2.2	GND	Ground
Data bit 1	DB1	P2.3	P2.4	GND	Ground
Data bit 2	DB2	P2.5	P2.6	GND	Ground
Data bit 3	DB3	P2.7	P2.8	GND	Ground
Data bit 4	DB4	P2.9	P2.10	GND	Ground
Data bit 5	DB5	P2.11	P2.12	GND	Ground
Data bit 6	DB6	P2.13	P2.14	GND	Ground
Data bit 7	DB7	P2.15	P2.16	GND	Ground
Data bit 8	DB8	P2.17	P2.18	GND	Ground
Data bit 9	DB9	P2.19	P2.20	GND	Ground
Data bit 10	DB10	P2.21	P2.22	GND	Ground
Data bit 11	DB11	P2.23	P2.24	GND	Ground
Data bit 12	DB12	P2.25	P2.26	GND	Ground
Data bit 13	DB13	P2.27	P2.28	GND	Ground
Data bit 14	DB14	P2.29	P2.30	GND	Ground
Data bit 15	DB15	P2.31	P2.32	GND	Ground
Data bit 16	DB16	P2.33	P2.34	GND	Ground
Data bit 17	DB17	P2.35	P2.36	GND	Ground

This evaluation module provides direct access to all the analog-to-digital converter input control and output signals via connector J4; see Table 6.

Table 6. Pinout for Converter Control Connector, J6

Description	Signal Name	Connector Pin No.		Signal Name	Description
Chip Select signal	$\overline{CS}$	J6.1	J6.2	GND	Ground
Read signal	$\overline{RD}$	J6.3	J6.4	GND	Ground
Convert Start signal	$\overline{CONVST}$	J6.5	J6.6	GND	Ground
Byte signal	BYTE	J6.7	J6.8	GND	Ground
18 or 16 bit bus signal	$\overline{BUS18}$/16	J6.9	J6.10	GND	Ground
Busy signal	BUSY	J6.11	J6.12	GND	Ground

5 Power Supplies

The EVM accepts four power supplies.

- A dual ±VA DC supply for the dual-supply operational amplifiers. Recommend ±12-VDC supply.
- A single +5-VDC supply for analog section of the board (A/D + Reference).
- A single +5-V or +3.3-VDC supply for digital section of the board (A/D + address decoder + buffers).

These voltages can be provided in two ways.

1. Wire in voltages at test points on the EVM. See Table 7.

Table 7. Power Supply Test Points

Test Point	Signal	Description
TP6	+BVDD	Apply +3.3 VDC or +5 VDC. See ADC data sheet for full range.
TP3	+AVCC	Apply +5 VDC.
TP4	+VA	Apply +12 VDC. Positive supply for amplifier.
TP5	–VA	Apply –12 VDC. Negative supply for amplifier.

2. Use the power connector J5, and derive the voltages elsewhere. The pinout for this connector is shown in Table 8. If using this connector, then set W1 jumper to connect +3.3 VDC or +5 VDC from connector to +BVDD. Short between pins 1-2 to select +5 VDC, or short between pins 2-3 to select +3.3 VDC as the source for the digital buffer voltage supply (+BVDD).

Table 8. Power Connector, J1, Pinout

Signal Power	Connector – J1		Signal
+VA (+12V)	1	2	–VA (–12V)
+5 VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
+3.3 VD	9	10	+5VD

6 Using the ADS8481EVM

The ADS8481EVM serves the functions of being a reference design, a prototyping board, and finally as an software test platform.

6.1 As a Reference Design

As a reference design, the ADS8481EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The ADS8481EVM analog input circuit is optimized for a wide bandwidth signal; therefore, the user may need to adjust the input buffer circuitry to better suit your needs. In AC-type applications where signal distortion is a concern, the user should use high quality capacitors such as Mica, polypropylene or COGs type capacitors in the signal path. In applications where the input is multiplexed, the A/D input resistor and capacitor may need to be adjusted further.

6.2 As a Prototype Board

As a prototype board, the ADS8481EVM features amplifiers in a standard 8-pin SOIC package and many resistor pads scatter around allowing the user to experiment with a host of circuits, as needed. The ADS8481EVM can be used to evaluate both dual- and single-supply amplifiers in both inverting and non-inverting configurations. The ADS8481EVM comes installed with a dual-supply amplifier which allows the user to take advantage of the full input voltage range of the converter. For applications that require signal supply operation and smaller input voltage range, the THS4031 can be replaced with the single-supply amplifier like the OPA300 or OPA350. Pad jumper SJP3 should be shorted between pads 1 and 2. This shorts the minus supply pin of the amplifier to ground. Positive supply voltage can be applied at test point TP4 or at connector J5 pin 1.

6.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5-6K interface board. The 5-6K interface board sits on the C5000 and C6000 digital signal processor starter kits (DSK). The ADS8481EVM is mapped then into the processor's memory space. The 5-6k interface board also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8481 analog-to-digital converter. For more information, see the 5-6K Interface Board user's guide (SLAU104) .

For the software engineer, the ADS8481EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user need only provide three address lines (A2, A1, and A0) and address valid line ($\overline{DC\_CS}$) to connector P2. To select which address combinations generate $\overline{RD}$ and $\overline{CONVST}$, set jumpers as shown in Table 4. Recall that the Chip Select ($\overline{CS}$) signal is not memory-mapped or tied to P2; therefore, it must be controlled by a general-purpose pin or shorted to ground at J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus by P3 and control by J3.

7 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this user's guide by its title and literature number. Updated documents can also be obtained through the TI Web site at www.ti.com.

Data Sheets:	Literature Number:
ADS8481	SLAS385
REF3240	SBVS058
REF3225	SBVS058
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318
THS4031	SLOS224
THS4032	SLOS224

Appendix A ADS8481EVM Bill of Materials

The following table contains a complete bill of materials for the ADS8481EVM. The schematic diagram also is provided for reference in Appendix C. Contact the Product Information Center or send an e-mail to *dataconvapps@list.ti.com* for questions regarding this EVM.

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part No.	Description
3	0	R16 R17 R33	603	Panasonic - ECG or Alternate	ERJ-3GEY0R00V	RES 0Ω 1/16W 5% 0603 SMD
3	0	R7 R19 R22	805	Panasonic - ECG or Alternate	ERJ-6GEY0R00V	RES 0.0Ω 1/10W 5% 0805 SMD
1	12	R39	805	Panasonic - ECG or Alternate	ERJ-6GEYJ120V	RES 12Ω 1/8W 5% 0805 SMD
3	33	R5 R25 R26	603	Yageo America or Alternate	9C06031A33R0FKHF T	RES 33.0Ω 1/10W 1% 0603 SMD
2	49.9	R1 R2	603	Panasonic - ECG or Alternate	ERJ-3EKF49R9V	RES 49.9Ω 1/10W 1% 0603 SMD
2	300	R27 R29	603			
2	300	R35 R36	805	Yageo America or Alternate	9C08052A3000FKHF T	RES 300Ω 1/8W 1% 0805 SMD
5	10k	R41–R45	603	Panasonic - ECG or Alternate	ERJ-3EKF1002V	RES 10.0kΩ 1/10W 1% 0603 SMD
1	10k	R46	805	Panasonic - ECG or Alternate	ERJ-6GEYJ103V	RES 10kΩ 1/8W 5% 0805 SMD
4	NI	R3 R4 R6 R28	603	Not Installed	Not Installed	
14	NI	R8–R10 R12 R13 R18 R20 R21R31 R32 R34 R37 R38 R40	805	Not Installed	Not Installed	
1	10K	R24	BOURNS_3296 Y	Bourns Inc.	3296Y-1-103	POT 10kΩ 3/8" SQ CERM SL MT
2	50	RP1 RP2	CTS_742	CTS Corporation	742C163470JTR	RES Array 47Ω 16TERM 8RES SMD
1	50	RP4	CTS_742_4RE S	CTS Corporation	742C083510JTR	RES Array 51Ω 8TERM 4RES SMD
1	1K	RP3	CTS_742	CTS Corporation	742C163102JTR	RES Array 1kΩ 16TERM 8RES SMD
4	MMZ2012R601A	L1 L2 L3 L4	805	TDK Corporation	MMZ2012R601A	FERRITE Chip 600Ω 500mA 0805
14	1000pF	C28–C36 C62–C65 C45	603	TDK Corporation or Alternate	C1608X7R1H102K	CAP CER 1000PF 50V XR7 10% 0603
6	0.1µF	C66–C71	603	TDK Corporation or Alternate	C1608X7R1E104K	CAP CER 0.10µF 25V X7R 10% 0603
2	0.47µF	C1 C2	603	TDK Corporation or Alternate	C1608X5R1A474K	CAP CER 0.47µF 10V X5R 10% 0603
3	1µF	C3 C5 C7	603	TDK Corporation or Alternate	C1608X5R1A105KT	CAP CER 1.0µF 10V X5R 10% 0603
5	1µF	C9–C12 C41	805	TDK Corporation or Alternate	C2012X7R1E105K	CAP CER 1.0µF 25V X7R 0805 T/R
8	2.2µF	C20–C27	603	TDK Corporation or Alternate	C1608X5R1A225MT	CAP CER 2.2µF 6.3V X5R 20% 0603
2	10µF	C38 C40	805	TDK Corporation or Alternate	C2012X5R0J106M	CAP CER 10µF 6.3V X5R 20% 0805
8	10µF	C48–C55	1206	TDK Corporation or Alternate	C3216X5R1C106M	CAP CER 10µF 16V X5R 20% 1206
1	22µF	C6	805	TDK Corporation or Alternate	C2012X5R0J226M	CAP CER 22µF 6.3V X5R 20% 0805
1	47µF	C37	1206	TDK Corporation or Alternate	C3216X5R0J476M	CAP CER 47UF 6.3V X5R 20% 1206
14	NI	C4 C8 C15 C16 C18 C19 C46 C47 C56–C61	603	Not Installed	Not Installed	

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part No.	Description
6	NI	C13 C14 C39 C42–C44	805	Not Installed	Not Installed	
1	REF3230	U1	6-SOT(DBV)	Texas Instruments	REF3230AIDBVR	3.0V 4ppm/°C, 100µA SOT23-6 Series (Bandgap) Voltage Reference
1	REF3240	U2	6-SOT(DBV)	Texas Instruments	REF3240AIDBVR	4.096V 4ppm/°C, 100µA SOT23-6 Series (Bandgap) Voltage Reference
1	ADS8481/ADS8482	U5	48-QFN(RGZ)	Texas Instruments	ADS8481IBPFBR	ADS8481 18-bit 1MSPS A/D
2	NI	U3 U7	8-SOP(D)	Not Installed	Not Installed	
1	THS4032	U4	8-SOP(D)	Texas Instruments	THS4032CD	100-MHz Low Noise Voltage-Feedback Amplifier, Dual
1	THS4031	U6	8-SOP(D)	Texas Instruments	THS4031IDR	100-MHz low-noise high-speed amplifier
4	SN74AHC245PWR	U8–U11	20-TSSOP(PW)	Texas Instruments	SN74AHC245PWR	Octal Bus Transceiver, Tri State
1	SN74AHC1G04DBV	U12	5-SOT(DBV)	Texas Instruments	SN74AHC1G04DBVR	Single Inverter Gate
1	SN74AHC138PWR	U13	16-TSSOP(PW)	Texas Instruments	SN74AHC138PWR	3-Line To 8-Line Decoder / Demultiplexer
1	SMA_PCB_MT	J1	SMA_JACK	Johnson Components Inc.	142-0701-301	Right Angle SMA Connector
3	NI	J2 J3 J4	SMA_JACK	Not Installed	Not Installed	
2	10X2X.1	P1 P3	10X2X.1_SMT_ PLUG_&_ SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT SOCKET - BOTTOM SIDE OF PWB
2	10X2X.1	Samtec			TSM-110-01-T-D-V-P	0.025" SMT Plug - top side of PWB
1	18X2X.1_SMT_PLU G _&_SOCKET	P2	18X2.1_SMT_ PLUG_&_ SOCKET	Samtec	SSW-118-22-S-D-VS	0.025" SMT Socket - bottom side of PWB
1				Samtec	TSM-118-01-T-D-V-P	0.025" SMT Plug - top side of PWB
1	5X2X.1	J5	5X2X.1_SMT_ SOCKET	Samtec	SSW-105-22-S-D-VS	0.025" SMT Socket - bottom side of PWB
1				Samtec	TSM-105-01-T-D-V-P	0.025" SMT plug - top side of PWB
1	6X2X.1	J6	6X2X.1_SMT_ PLUG_ &_ SOCKET	Samtec	TSM-106-01-T-D-V-P	0.025" SMT Plug - top side of PWB
1	2POS_JUMPER	W5	2pos_jump	Samtec	TSW-102-07-L-S	2 Position Jumper _ 0.1" spacing
5	3POS_JUMPER	W1–W4 W6	3pos_jump	Samtec	TSW-103-07-L-S	3 Position Jumper _ 0.1" spacing
4	SJP2	SJP2 SJP7 SJP8 SJP9	SJP2	Not Installed	Not Installed	
4	SJP3	SJP1 SJP3 SJP4 SJP6	SJP3	Not Installed	Not Installed	
8	TP_0.025	TP3–TP7 TP9 TP11 TP12	test_point2	Keystone Electronics	5000K–ND	Test point PC MINI 0.040"D Red
6	TP_0.025	TP1 TP2 TP8 TP10 TP13 TP14	test_point2	Keystone Electronics	5001K–ND	Test point PC MINI 0.040"D Black

Appendix B ADS8481EVM LAYOUT

Appendix B contains the EVM layout.

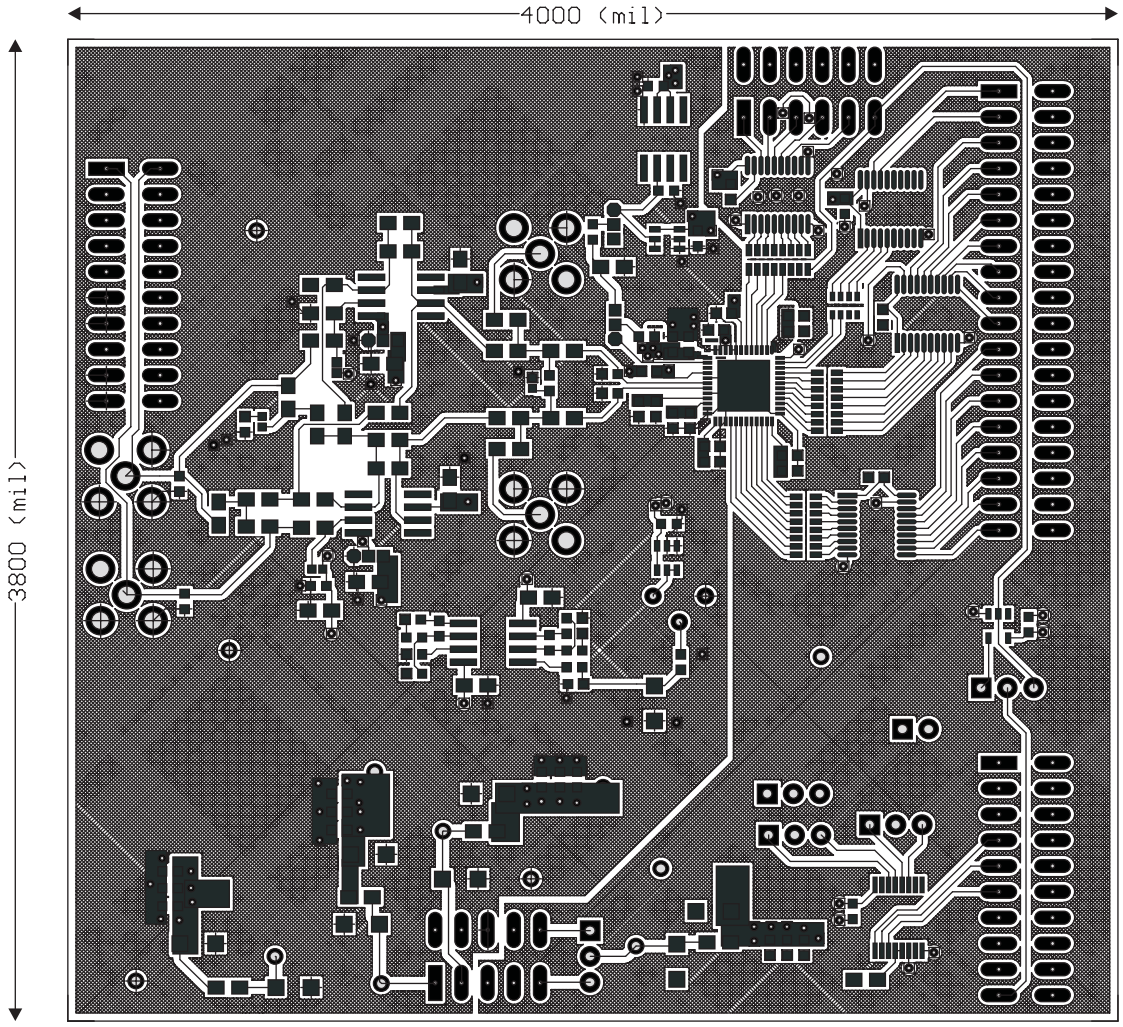


Figure B-1. Top Layer – Layer 1

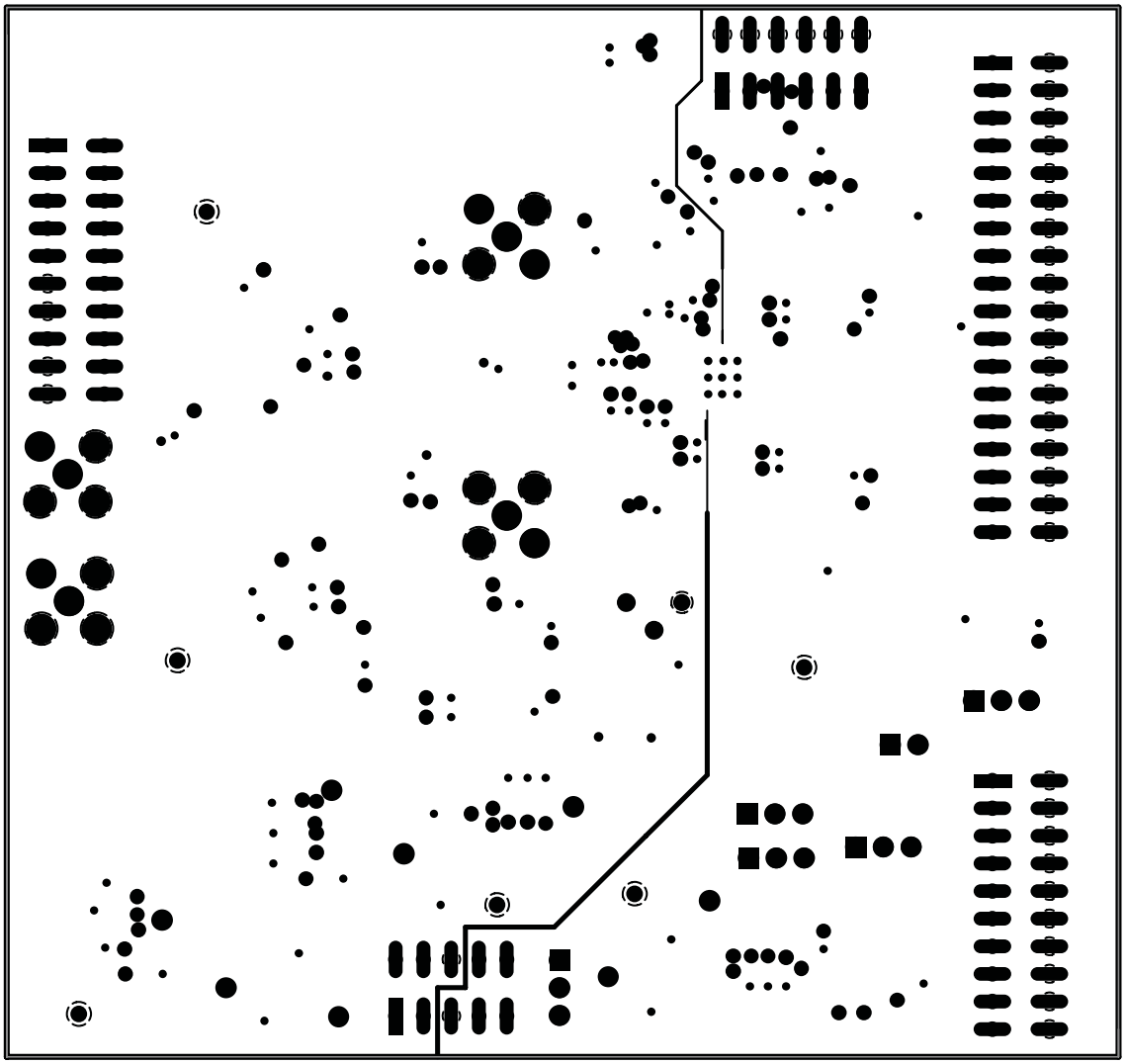


Figure B-2. Ground Plane – Layer 2

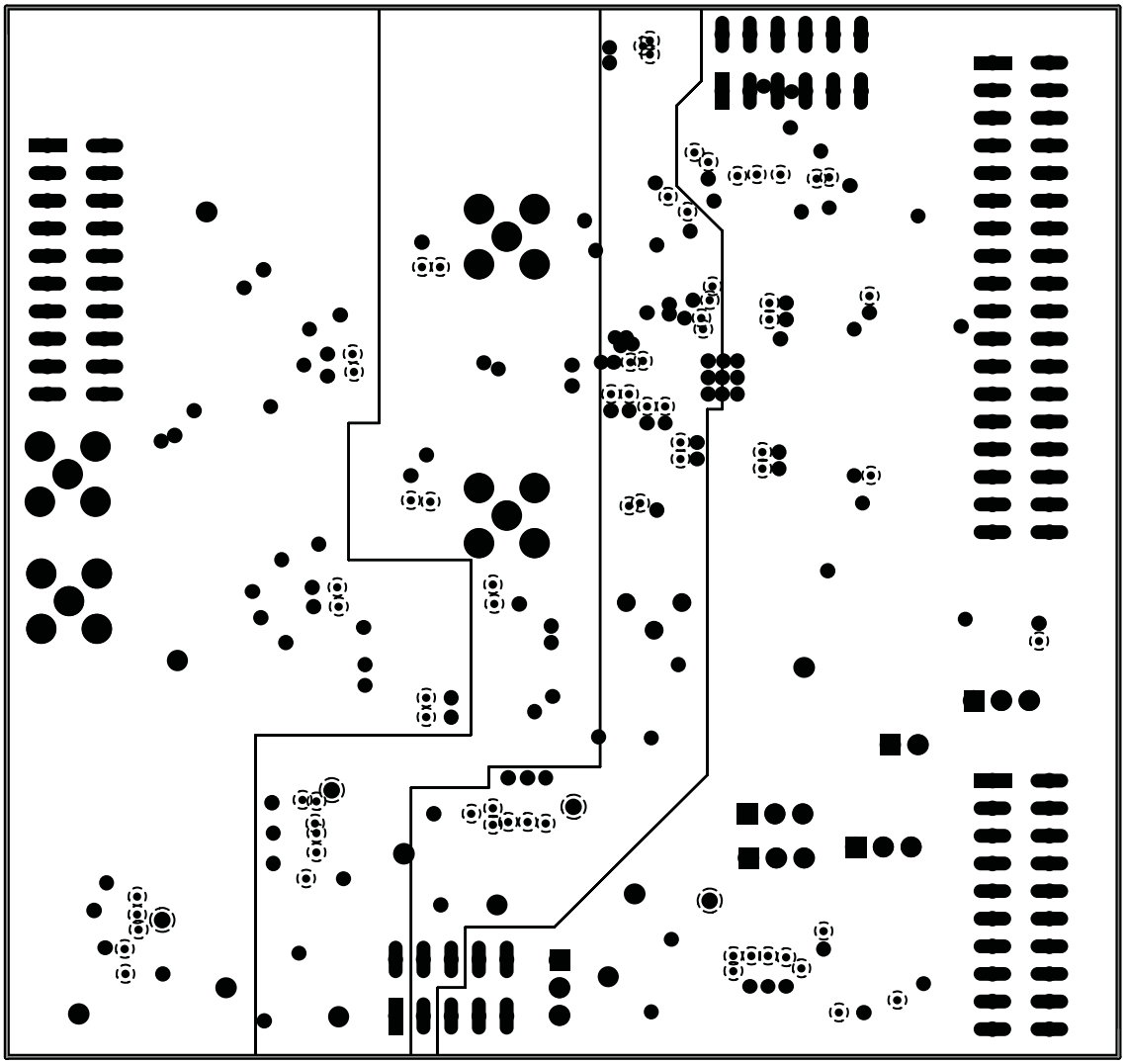


Figure B-3. Power Plane – Layer 3

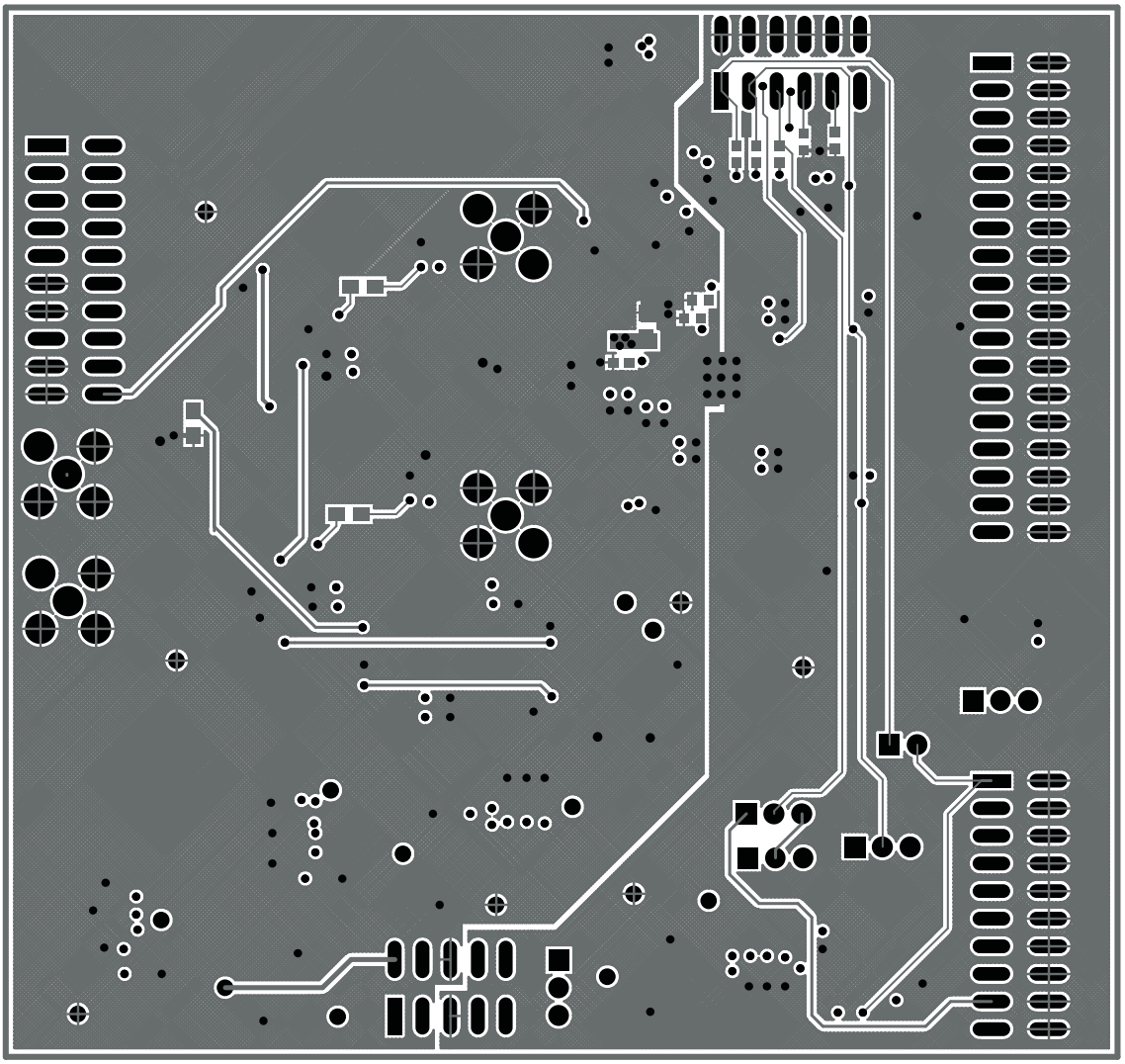


Figure B-4. Bottom Layer – Layer 4

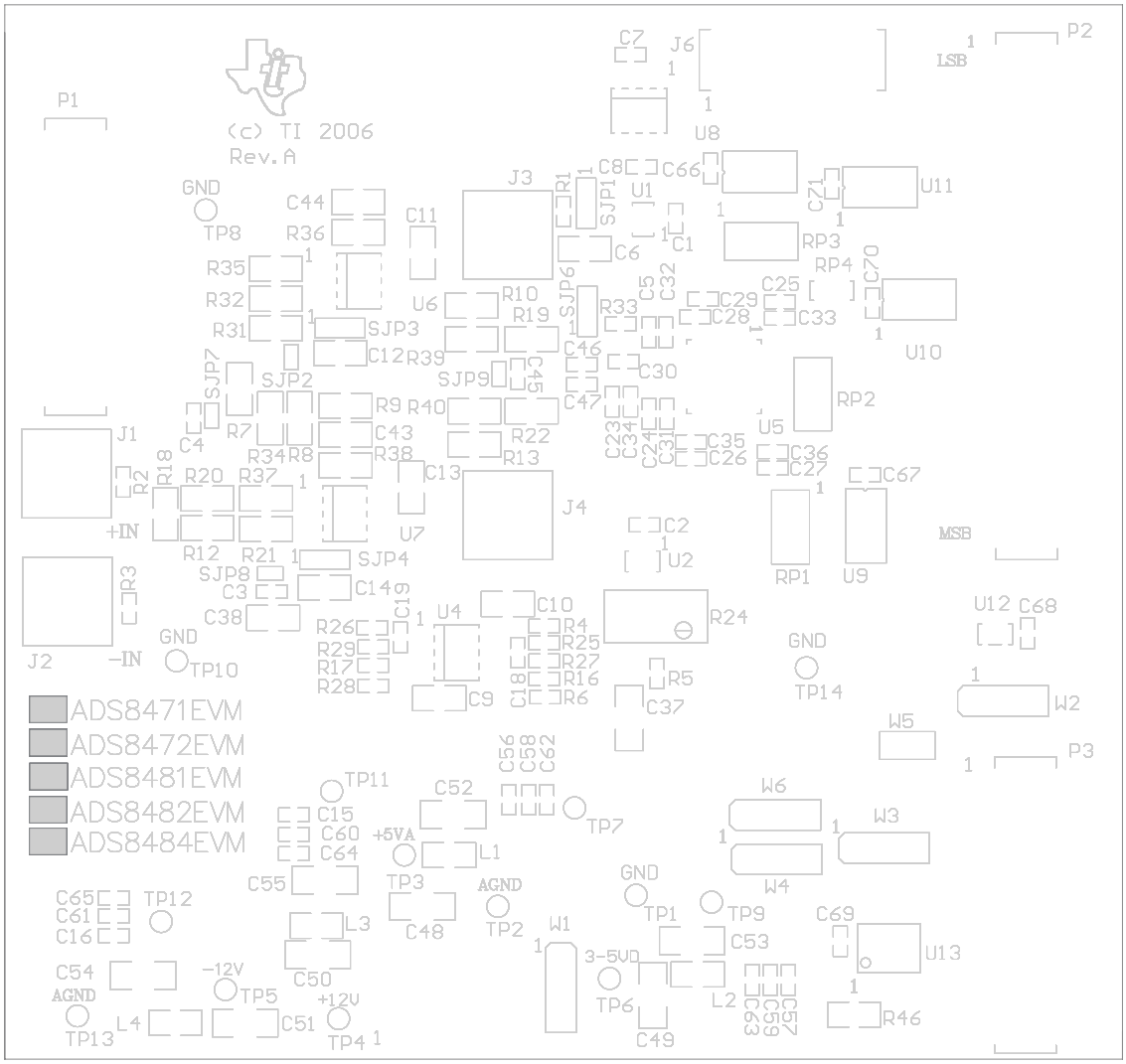


Figure B-5. Top Overlay

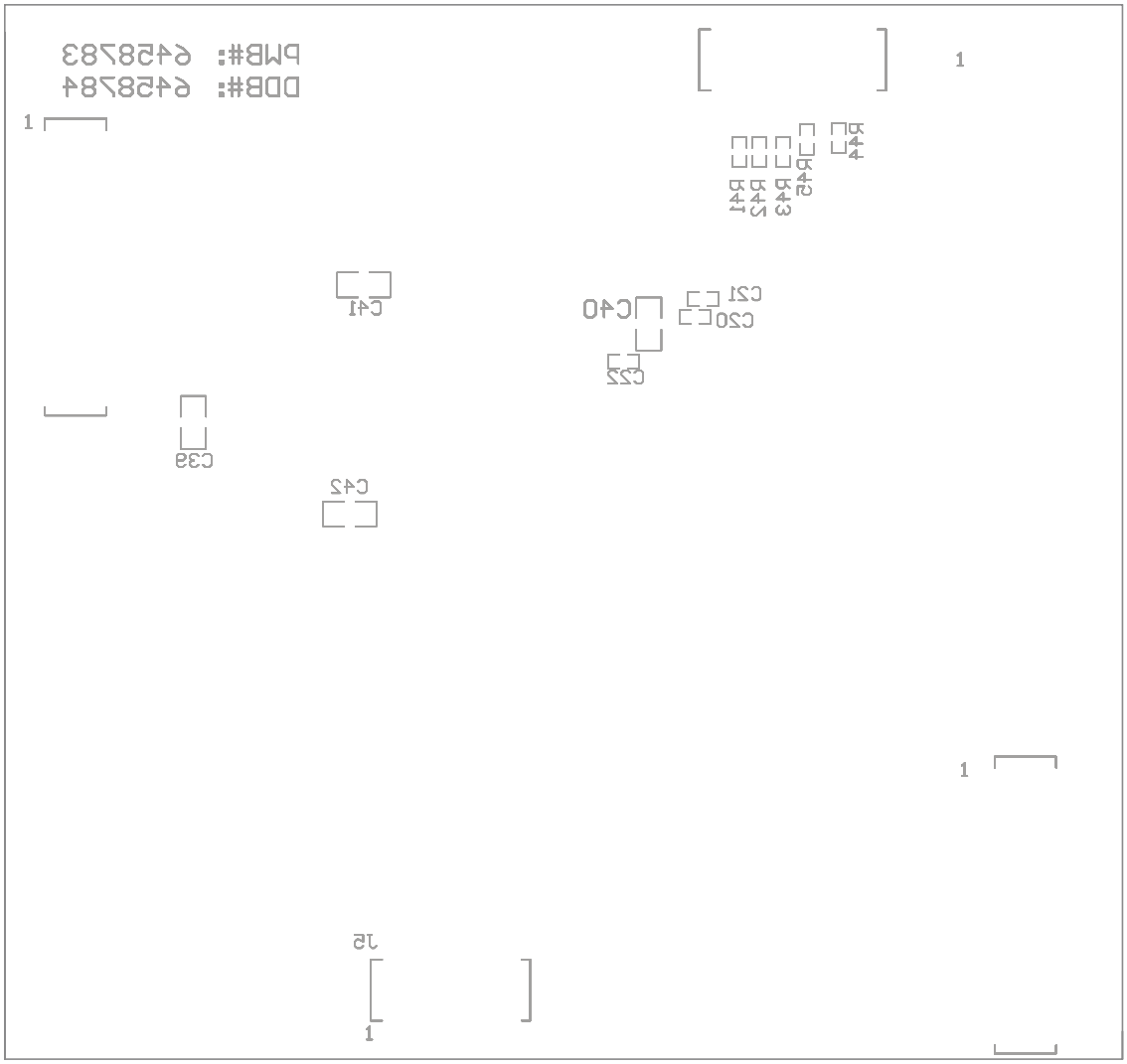
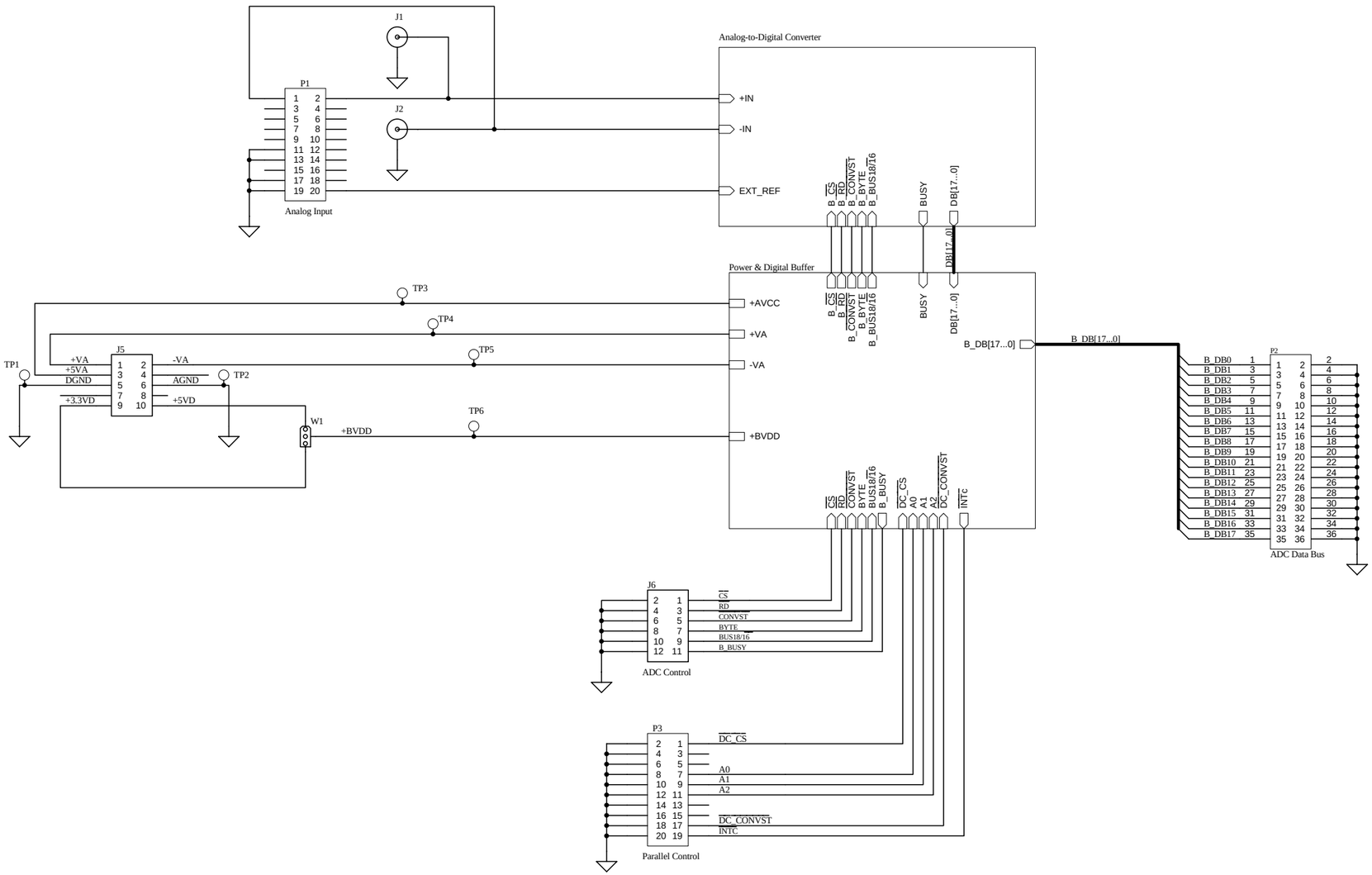


Figure B-6. Bottom Overlay

Appendix C ADS8481EVM Schematic

The ADS8481EVM schematic is appended to this page.

Revision History		
REV	ECN Number	Approved



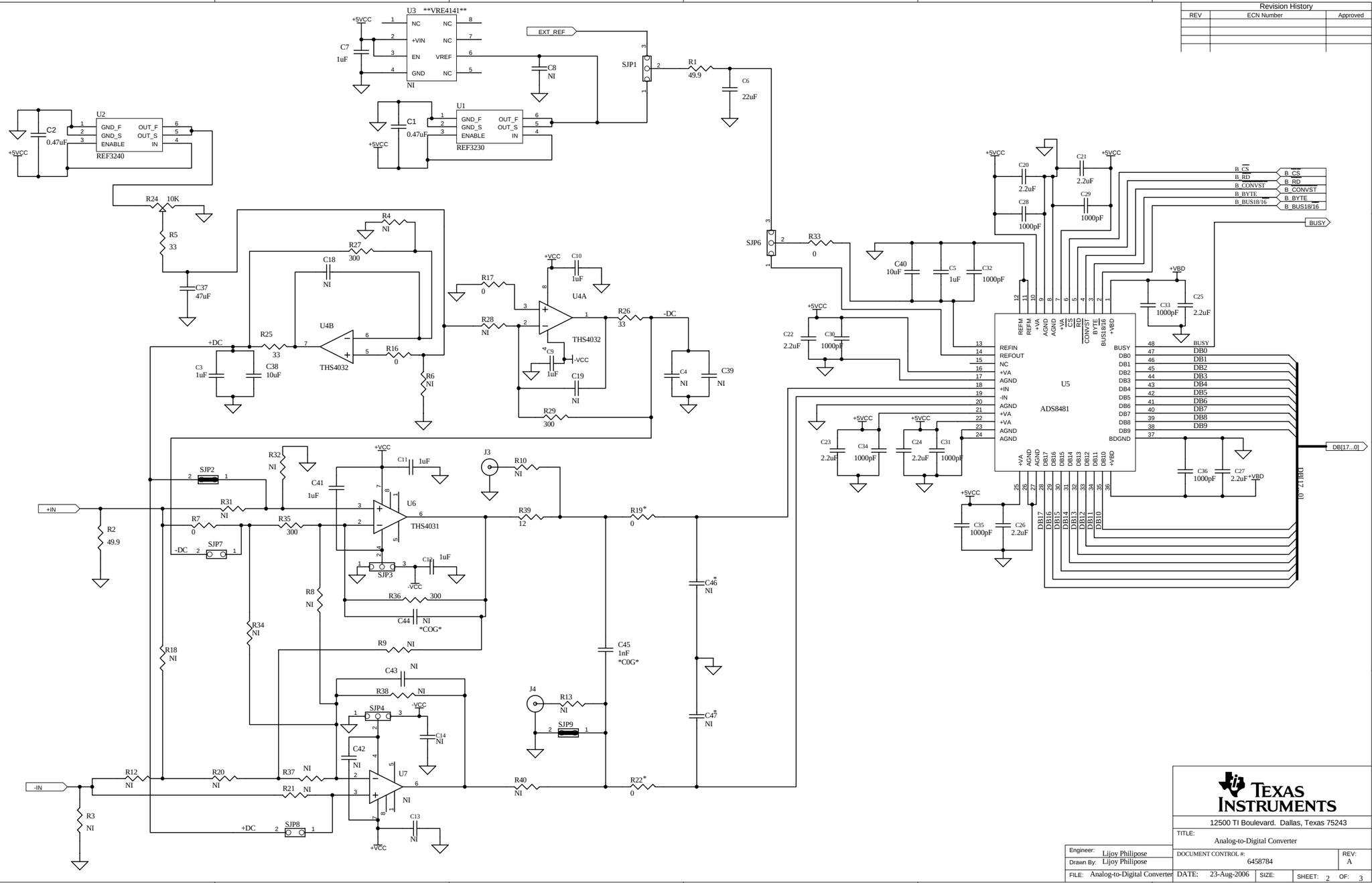
Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	BlockDiagram.sch

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

TITLE: ADS8481/ADS8482EVM Block Diagram			
DOCUMENT CONTROL #: 6458784			REV: A
DATE: 23-Aug-2006	SIZE:	SHEET: 1	OF: 3

Revision History		
REV	ECN Number	Approved



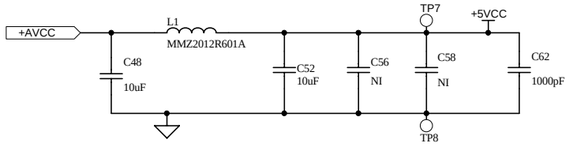
Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Analog-to-Digital Converter

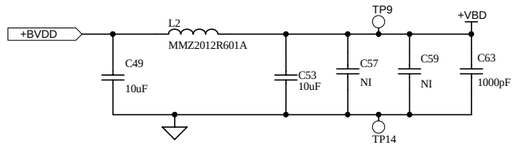
TEXAS INSTRUMENTS

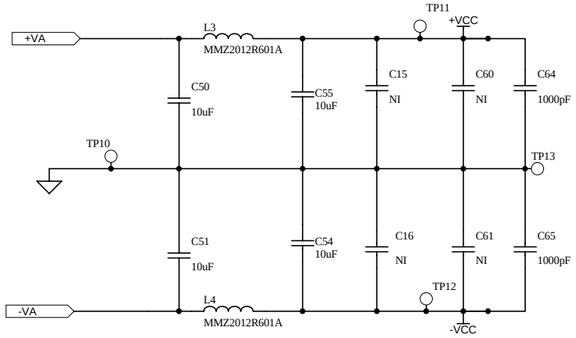
12500 TI Boulevard. Dallas, Texas 75243

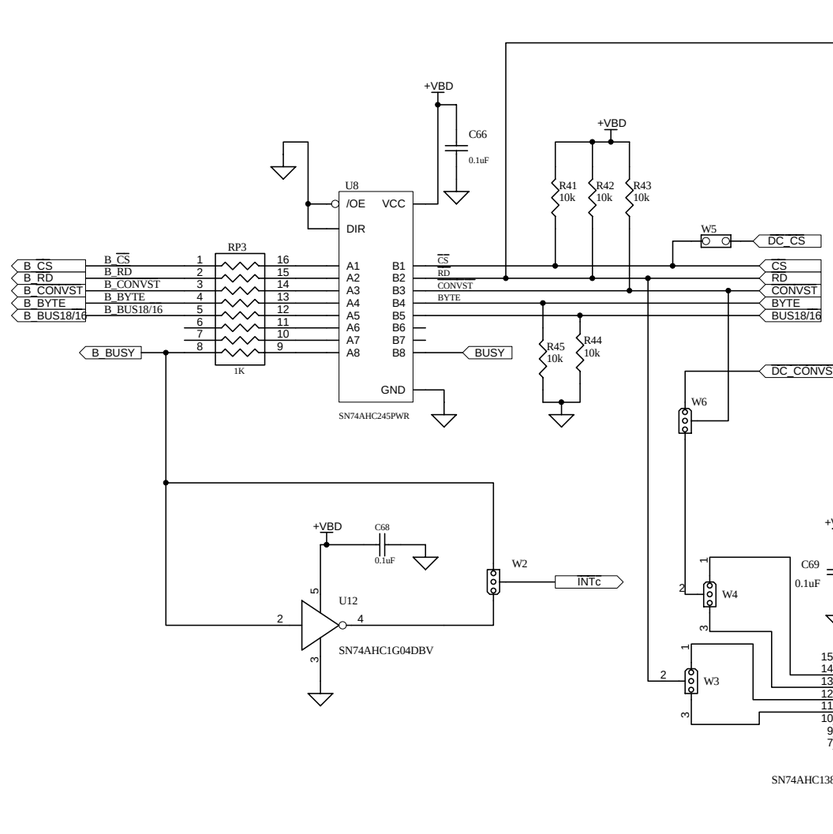
TITLE: Analog-to-Digital Converter			
DOCUMENT CONTROL #: 6458784			REV: A
DATE: 23-Aug-2006	SIZE:	SHEET: 2	OF: 3

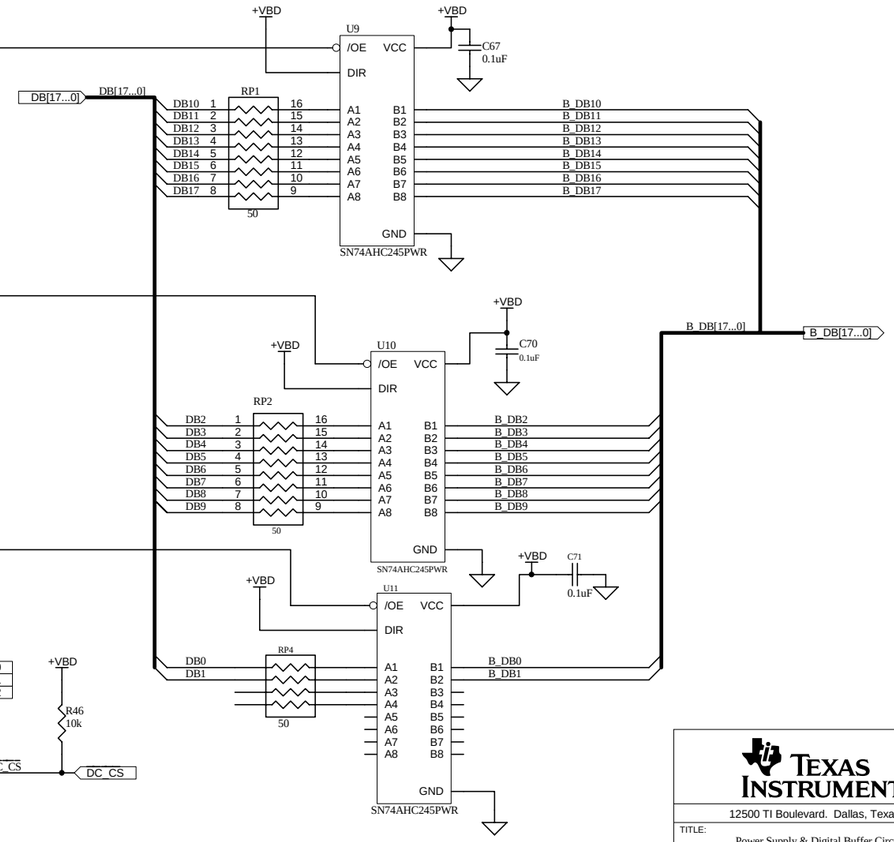
Revision History		
REV	ECN Number	Approved











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TITLE:	Power Supply & Digital Buffer Circuit
DOCUMENT CONTROL #:	6458784
REV:	A
DATE: 23-Aug-2006	SIZE:
SHEET: 3 OF: 3	
Engineer:	Lijoy Philipose
Drawn By:	Lijoy Philipose
FILE:	Power & Digital Buffer

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During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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