User's Guide SLAU429–March 2012



TSW1265EVM Evaluation Module

The TSW1265EVM evaluation module is a wideband, dual-receiver reference design and evaluation platform. The signal chain allows conversion from RF to bits using a dual-channel downconversion mixer, the LMH6521 dual-channel, digitally controlled variable gain amplifier (DVGA), and the ADS4249 14-bit 250-MSPS analog-to-digital converter (ADC). The TSW1265EVM also includes the LMK04800 dual-PLL clock jitter cleaner and generator to provide an onboard low-noise clocking solution. A provided software GUI allows for configuration of the ADS4249 and LMK04800. Either the GUI or an FPGA using the high-speed connector can control the gain of the LMH6521 DVGA. The EVM mates with the TSW1400 pattern capture and generation card to capture data from the ADS4249. Then, the High Speed Data Converter Pro software tool can perform signal analysis. The TSW1265EVM product folder on the TI web site contains the EVM schematic, bill of materials, and layout files.

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1 Introduction

1.1 Overview

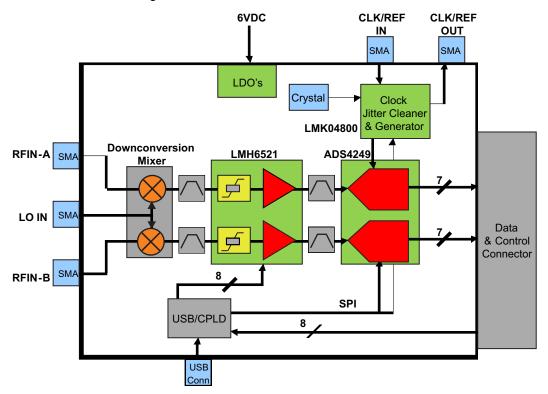
The TSW1265EVM evaluation module is a wideband, dual-receiver reference design and evaluation platform. The signal chain allows conversion from RF to bits using a dual-channel downconversion mixer, the LMH6521 dual-channel DVGA, and the ADS4249 14-bit, 250-MSPS ADC. The TSW1265EVM also includes the LMK04800 dual-PLL clock jitter cleaner and generator to provide an onboard low-noise clocking solution.

The default configuration of the board allows for an RF frequency of 1700 MHz to 2200 MHz and an LO frequency of 1750 MHz to 2700 MHz. The IF portion of the board, starting at the output of the mixer to the ADC input, is set for a center frequency of 187.5 MHz and a 1-dB bandwidth of 75 MHz. Modification of both the RF and IF frequency ranges is possible and is discussed later.

A software GUI allows for configuring the ADS4249 and LMK04800. The GUI, or alternatively through the high-speed connector with an FPGA, can control the gain of the LMH6521 DVGA. The EVM mates with the TSW1400 pattern capture and generation board to capture data from the ADS4249. The High Speed Data Converter Pro software tool then can perform signal analysis. The TSW1400 and High Speed Data Converter Pro greatly simplify the evaluation process by providing the hardware and software necessary for pattern capture and analysis.

1.2 Block Diagram

Figure 1 shows the block diagram of the TSW1265EVM.







2 Software Control

This section provides installation instructions and explanations of the TSW1265 GUI.

2.1 Installation Instructions

- 1. The software can be downloaded from the TSW1265EVM production page on www.ti.com. Find the page by searching for *TSW1265EVM*. The software appears under the *Related Products* section on the *TI Software* tab.
- 2. Extract the files from the zip file named *TSW1265 GUI vXpY Installer.zip* where *XpY* represents the version number.
- 3. Run setup.exe, and follow the installation prompts.
- 4. Start the GUI by going to the Start Menu \rightarrow All Programs \rightarrow Texas Instruments ADCs \rightarrow TSW1265 GUI.
- 5. When plugging the board into the computer for the first time through the USB cable, you are prompted to install the USB drivers.
 - Windows® XP: If Windows XP does not automatically install the drivers, follow the prompts on the screen to do so. Do not let Windows XP search Microsoft Update for the drivers, but do let Windows XP install the drivers automatically.
 - Windows 7: After installing the TSW1265 GUI, Windows 7 should automatically be able to install the drivers for the TSW1265EVM with no input from the user.

2.2 Software Operation

The TSW1265 GUI allows the user to program the ADS4249, LMH6521, and LMK04800 for proper operation. The controls for each device are split between different tabs for a simplified interface. Detailed descriptions for each tab are below.

3

Software Control



Software Control

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2.2.1 ADS4249 Control Tab

SW1265 GUI S4249 Control LMK04800		USB Status: Save Load Read All Reset USB MK04800 Advanced LMH6521 Gain
Reset/Readout Reset Readout DFF M OFF	Powerdown Modes Powerdown Global Standb OFF III O	OFF Disabled 0 0 25 x00 x29 x00
Performance Modes High Perf Mode High Freq Mode ChA High Freq Mode ChB Low Speed Mode En Low Speed Mode ChA Low Speed Mode ChB	OFF LVDS Data St OFF LVDS Clkout St Disabled CMOS Clk St OFF Cli O L Si - D	a Format 2's Comp Output Buffer Selection DDR LVDS x3F x00 strength Normal Disable Output Buffer Selection DDR LVDS x41 x00 Strength Normal Disable Output Buffer Selection Default x42 x00 Strength Max Enable LVDS Swing Disabled x45 x00 Strength Max Enable LVDS Swing 350 mV x00 x400
A	Pattern ChB isabled Offset Correction Freeze Offset Co	x02 x400 x03 x200
		LMH6521 Re

Figure 2. ADS4249 Control Tab

Table 1. ADS4249	Control Ta	b Section	Descriptions
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Section	Description
Reset/Readout	Controls the reset and readout functions. Note that readout is not currently functional.
Powerdown Modes	Put the device into either global or standby powerdown modes to lower power consumption.
Digital Functions	Enable or disable the digital gain functions and set the gain value. Also enables use of test patterns and offset correction.
Performance Modes	Set the various performance modes
Data and Clock Outputs	Change parameters of the digital and clock outputs such as levels, data format, and output buffer type.
Test Patterns	Set the test patterns of both channels for testing and troubleshooting of the digital interface.
Offset Correction	Enable and set parameters of the offset correction feature.



2.2.2 LMK04800 Main Tab

SW1265 GUI v1.0	d All Save Load F	USB Status: Read All Reset USB	EXI
DS4249 Control LMK04800 Main LMK04800 C	Outputs LMK04800 Advanced LM	IH6521 Gain	ADS4249 Register
Power Down, Reset, Mode Select		OSCout	x00 x00 x01 x00
promotion and a second contract of the second s	Dual PLL, Internal VCO	PD OSCin O Divider	x03 x00 x25 x00
CLKin Settings CLKin_SELECT_MODE Pin Select Mode CLKin0 BUF Type Bipolar CLKin1 BUF Type Bipolar CLKin0 PreR Div CLKin1 PreR Div	VCO Divider VCO Divider EN FB MUX Feedback MUX	EN OSCout0 EN OSCout1 OSCout0 Type OSCout1 Type LVDS DSCout0 MUX OSCout1 MUX Bypass Bypass	x29 x00 x2B x00 x3D x00 x3F x00 x40 x00 x41 x00 x42 x00 x45 x00 LMK04800 Register
	PLL 2 Settings		x00 x400A819
PLL 1 Settings	EN XTAL SYNC PLL2 Prescalar R Divider N Divid		x01 x400A819 x02 x400A819 x03 x200A801
SYNC PLL1 CP Tri-state R Divider N Divider CP Pol	2 4 48 PLL2 Fast PDF N Cal E) > 100 MHz 48	ivider Divider DLD Count CP Gain ivider 8192 3200 uA	x03 x200A801 x04 x000A819 x05 x400A819 x06 x0000000 x07 x0400000
Window Size DLD Count CP Gain	Ref Frequency XTAL Level	Internal Loop Filter:	x08 x0000800 x09 x2AAAAAA x0A x48A0210
PLL1 N Delay PLL1 R Delay DAC CLK Divider	OSCin Frequency	C3 2 10 pF C4 2 10 pF R3 200 R4 2 200	LMH6521 Register

Figure 3. LMK04800 Main Tab

Table 2. LMK04800 Main Tab Section Descript	lions
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Section	Description
Power Down, Reset, Mode Select	Allows for powering down and resetting the part. Also controls the mode of the LMK04800.
CLKin Settings	Enabled and select the input clock source, input buffer types, and dividers.
VCO Divider	Set the VCO divider to reduce the frequency on the clock distribution path. It is recommended to use the VCO directly.
OSCout	Control power to the OSCin port. Also enable and change parameters of the OSCout pins.
PLL 1 Settings	Configure PLL 1 settings when using the dual PLL mode.
PLL 2 Settings	Configure PLL 2 settings for both dual and single PLL mode.



Software Control

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2.2.3 LMK04800 Outputs Tab

SW1265 GUI v1.0	Send All Save Load	USB Status: Read All Reset USB	EX
Clock Out 0 and 1 Power DD Half Shift Divider Digital Delay 25 5 Analog Delay ADLY Amount Both Off 500 ps CLKout0 Type CLKout1 Type	Clock Out 2 and 3 Power DD Half Shift Digital Delay 25 5 Analog Delay ADLY Amount Both Off 500 ps CLKout2 Type CLKout3 Type	Clock Out 4 and 5 Power DD Half Shift Divider Digital Delay 25 Analog Delay ADLY Amount Both Off 500 ps CLKout4 Type CLKout5 Type	ADS4249 Register x00 x00 x01 x00 x25 x00 x25 x00 x28 x00 x3D x00 x3F x00 x40 x00 x41 x00 x42 x00
Power down Power down	Power down Power down	Power down Power down	x45 x00 LMK04800 Regist x00 x400A81
Power DD Half Shift Divider Digital Delay 1 5 Analog Delay ADLY Amount Both Off 500 ps CLKout6 Type CLKout7 Type LVCMOS Power down	Power DD Half Shift Divider Digital Delay 25 5 Analog Delay ADLY Amount Both Off 500 ps CLKout8 Type CLKout9 Type UVDS Power down	PowerDD Half ShiftDividerDigital Delay255Analog DelayADLY AmountBoth Off500 psCLKout10 TypeCLKout11 TypePower downPower down	x01 x400A81 x02 x400A81 x03 x200A80 x04 x000A81 x05 x400A81 x06 x000000 x07 x040000 x08 x000080 x09 x2AAAAA x0A x48A021 x0A x48A021

Figure 4. LMK04800 Outputs Tab

Table 3. LMK04800 Outputs	Tab Section Descriptions
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Section	Description
Clock Out 0 and 1	Configure Clock Out 0 and 1 outputs. Enable the outputs and set the divider, delay, and output buffer.
Clock Out 2 and 3	Configure Clock Out 2 and 3 outputs. Enable the outputs and set the divider, delay, and output buffer.
Clock Out 4 and 5	Configure Clock Out 4 and 5 outputs. Enable the outputs and set the divider, delay, and output buffer.
Clock Out 6 and 7	Configure Clock Out 6 and 7 outputs. Enable the outputs and set the divider, delay, and output buffer. Also select the source for the output.
Clock Out 8 and 9	Configure Clock Out 8 and 9 outputs. Enable the outputs and set the divider, delay, and output buffer. Also select the source for the output.
Clock Out 10 and 11	Configure Clock Out 10 and 11 outputs. Enable the outputs and set the divider, delay, and output buffer.



2.2.4 LMK04800 Advanced Tab

SW1265 GUI v1.0	Send All Save L 04800 Outputs LMK04800 Adva	nced LMH6521 Gain	USB Status: Reset USB	ADS4249 Register
EN_SYNC SYNC_QUAL SYNC_EN_AUTO SYNC_EN_AUTO SYNC Polarity Active Low SYNC Type Input w/ pull-up SYNC MUX	N_VTUNE_RAIL_DET	Atus Pins Setup Status_CLKin0_TYPE Dinput w/ pull-down Status_CLKin1_TYPE Dinput w/ pull-down LD TYPE Output (push-pull) LD MUX PLL1 & 2 DLD	Status_CLKin0_MUX Cogic Low Status_CLKin1_MUX Cogic Low EN LOS LOS_TIMEOUT 200 ns, 420 kHz	x00 x00 x01 x00 x03 x00 x25 x00 x29 x00 x3D x00 x3D x00 x40 x00 x41 x00 x42 x00 x45 x00 LMK04800 Regist
Holdover Mode EN_TRACK HOLDOVER MODE HOL	DOVER TYPE	A	CLKin_Sel_INV	x01 x400A81 x02 x400A81 x03 x200A80 x04 x000A81 x05 x400A81 x06 x000000 x07 x040000 x09 x2AAAAA x0A x48A021 LMH6521 Registe x1 x3F x2 x3F

Figure 5. LMK04800 Advanced Tab

Table 4. LMK04800 Advanced Tab Section Descriptions	Table 4. LMK04800	Advanced	Tab Section	Descriptions
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Section	Description	
SYNC	Enable and configure the sync functionality.	
DAC Vtune Rail Detection	Enable and control the internal DAC settings.	
Status Pins Setup	Setup the status pins for various outputs as well as control some miscellaneous functions.	
Holdover Mode	Enable and configure holdover mode.	



Software Control

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2.2.5 LMH6521 Gain Tab

TSW1265 GUI v1.0 Send All Save Load Read All Reset USB Reset USB	EXIT
ADS4249 Control LMK04800 Main LMK04800 Outputs LMK04800 Advanced LMH6521 Gain	(ADS4249 Register
Channel A GAIN A GAIN B GAIN B GAIN B GAIN B GAIN B	x00 x00 x01 x00 x03 x00 x25 x00 x29 x00 x2B x00 x3D x00 x3F x00 x40 x00 x41 x00 x42 x00 x45 x00
	x00 x400A819 x01 x400A819 x02 x400A819 x03 x200A801 x04 x000A819 x05 x400A819 x06 x000000 x07 x0400000 x07 x0400000 x08 x0000800 x09 x2AAAAAA x0A x48A0210
	LMH6521 Registers
	x1 x3F x2 x3F

Figure 6. LMH6521 Gain Tab

Table 5. LMH6521 Gain Tab Section Descriptions

Section	Description
Channel A	Set the gain for channel A of the LMH6521.
Channel B	Set the gain for channel B of the LMH6521.



2.2.6 Send All, Save, Load, Read All



Figure 7. Send All, Save, Load, and Read All

Table 6. Send All, Save, Load, and Read All Descriptions

Section	Description
Send All	Click to send all the registers for all devices. Press a few times if the board does not seem to be responding correctly.
Save	Save the register settings in a text file. Can be reloaded later to set the GUI and devices to a known state.
Load	Load a saved configuration.
Read All	This function is not currently enabled on the TSW1265 GUI.

2.2.7 USB Status

The indicator shows the status of the USB connection. The indicator is lit when the USB connection is valid. If the computer is not connected to the board, click the *Reset USB* button.

2.2.8 Exit

Click to exit the GUI. Note that the X in the upper right corner of the window has been disabled to ensure that the USB connection is closed properly.

3 Basic Test Procedure

3.1 TSW1400 Setup

See the TSW1400 User's Guide (SLWU079) for a more detailed explanation of the TSW1400 setup and its features. This document assumes that the High Speed Data Converter Pro software and the TSW1400 pattern capture and generation board are both installed and functioning properly. This information can be found at http://www.ti.com/tool/tsw1400evm.



Basic Test Procedure

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3.2 Test Setup Block Diagram

Below is a block diagram of the test setup.

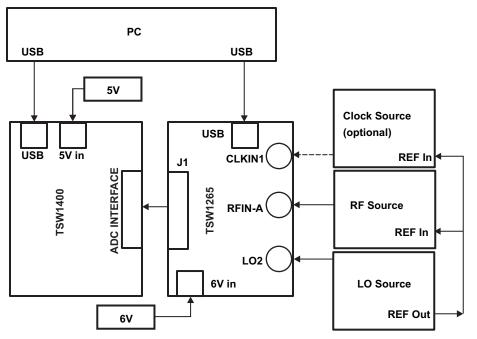


Figure 8. Test Setup Block Diagram

3.3 Quick-Start Procedure

3.3.1 TSW1400 Data Capture Card

- 1. Connect a 5-V power supply to connector J12 of the TSW1400. Flip switch SW7 to the "ON" position.
- 2. Insert a USB cable into the USB port on the TSW1400. Connect the other end to the PC.

3.3.2 TSW1265EVM

- 1. Connect a 6-V power supply to either the banana jacks or the barrel connector. If using the banana jacks, connect the positive end to J17 and the negative end to J16.
- 2. Connect a USB cable between the TSW1265 board and the PC.
- 3. Connect an LO source to the SMA connector labeled *LO2*. Set the LO source to 1960 MHz and 0 dBm.
- 4. Connect an RF source to the SMA connector labeled *RFIN-B*. Because the DVGA may come up with an unknown gain, set the amplitude of the RF input to -30 dBm to prevent overdriving the ADC on start-up. Set the frequency to 1780 MHz.
- 5. Connect the TSW1265 to the TSW1400 by connecting J1 on the TSW1265 to the ADC Interface connector on the bottom of the TSW1400.

3.3.3 TSW1265 GUI

- 1. Start the TSW1265 GUI by going to Start Menu \rightarrow All Programs \rightarrow Texas Instruments ADCs \rightarrow TSW1265 GUI.
- 2. Make sure the green indicator is lit up indicating that the TSW1265 board has been successfully connected to the PC. If not, click the "Reset USB" button. If it still is not lit up, check the USB connection. If the USB connection is correct, unplug the USB cable, wait five seconds and then plug it back in. Repeat these steps if necessary.
- 3. Click the "Load" button and select the file named "250MHz_onboard_clock.txt". Click "Ok". The file is



located in the TSW1265 GUI installation directory in the folder named "Configuration Files".

4. Click "Send All". At this point, the LED labeled "D1" on the TSW1265 should be lit indicating a PLL lock. If it is not lit, click "Send All" again.

3.3.4 High Speed Data Converter Pro

- 1. Start the High Speed Data Convert Pro software tool by going to Start Menu \rightarrow All Programs \rightarrow Texas Instruments ADCs \rightarrow High Speed Data Converter Pro.
- When it prompts for the serial number of the board, select the serial number that represents the TSW1400 that has been connected to the TSW1265. This number should be on a sticker on the TSW1400.
- 3. In the "Select ADC" drop-down box select "ADS4249". If it asks to download the firmware select "Yes". Multiple LEDs will light up on the TSW1400 once the firmware has finished downloading.
- 4. Select Single Tone from the Test Selection drop-down menu.
- 5. At the bottom left corner, enter 250M into the ADC Sampling Rate (Fs) box. Enter 180M into the ADC Input Target Frequency box. Press the Enter key.
- 6. Select *Blackman* from the drop-down box originally labeled "Rectangular". This applies a Blackman windowing function because the clock source is not synchronized to the LO and RF sources and therefore the captured data will not be coherent.
- 7. All boards and software are now set up. Click the *Capture* button. Once the capture is complete, adjust the input source amplitude and LMH6521 gain as needed to achieve approximately -1 dBFS. The LMH6521 gain can be changed on the *LMH6521* Gain tab of the TSW1265 GUI. An example of a -1-dBFS plot is shown in the figure below.

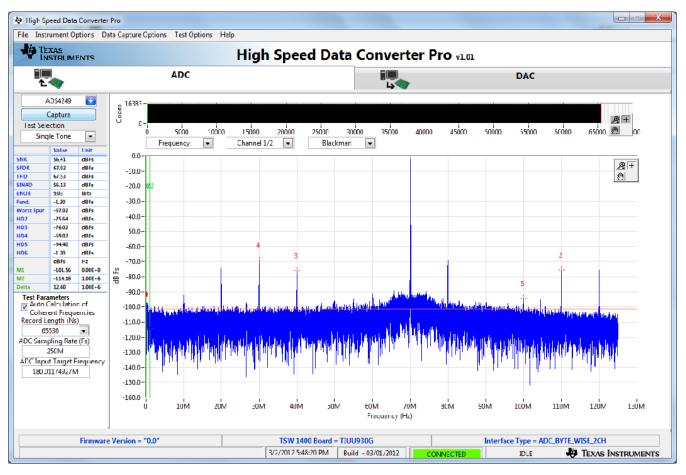


Figure 9. TSW1265 Sample Capture using the TSW1400

3.4 Optional Features and Configurations

3.4.1 Clocking

The TSW1265EVM allows for multiple clocking configurations by using the LMK04800 clock jitter cleaner and generation chip. The board comes preinstalled with a 20-MHz crystal which can be used to generate the sampling clock. The default for the board is a 250-MHz sampling clock.

Since the board is initially setup for a 250-MHz sampling clock, an LC resonant tank filter centered at 250 MHz has been placed on the clock lines to provide filtering of wideband noise. The filter has a wide enough bandwidth to allow the use of an external 245.76-MHz clock as well. If another clocking frequency is needed, the LC resonant tank will need to be changed. It can also be removed altogether, but at the cost of some added clock jitter. Use Equation 1 below to calculate the inductor and capacitor values for the desired clock frequency. F_c is the center frequency of the filter and Q can be chosen to be an arbitrary value of 25. Assume R is equal to 100 Ω . Note that the traces from the LMK04800 to the ADC add approximately 50 pF of capacitance which has already been considered in Equation 1.

$$L = \frac{1}{2\pi f \frac{Q}{R}}$$
$$C = L \left(\frac{Q}{R}\right)^2 - 50 pF$$

(1)

The TSW1265 board comes preinstalled with the LMK04803 which has an internal VCO frequency range of 1840 MHz to 2030 MHz. If the desired clock cannot be derived from this frequency range using integer dividers, then this device can be swapped out for another LMK04800 with a different VCO range. Consult the LMK04800 datasheet (SNAS489H) to determine which LMK04800 will provide the correct VCO range for the needed clocking frequency.

The LMK04800 can be setup in clock distribution mode or as a clock generator using single or dual PLL mode. The different modes of operation are discussed below.

- External Clock Mode: The LMK04800 can be setup in clock distribution mode to allow the use of an external clock source. This can be used for coherent sampling by provided a clock that is synchronized to the RF and LO signal sources. The TSW1265 GUI includes a configuration file for the external clock mode. This file is located in the TSW1265 GUI installation directory in the folder "Configuration Files" and is named "external_clock.txt". The file can be loaded by clicking the "Load" button, navigating to the correct folder, selecting the file, and clicking "Ok". Click "Send All" a few times to make sure the board is configured properly. The user provides an external clock through the "CLKIN1" SMA connector on the TSW1265 board.
- Onboard Clock using Single PLL Mode: This is the default mode of operation for the TSW1265. In this mode, the 20-MHz crystal is used to generate other frequencies by using the single PLL mode of the LMK04800. The 20-MHz crystal acts as the reference for the PLL and the divided down internal VCO acts as the clock source. There is an included configuration file that will setup the LMK04800 in single PLL mode and generate a 250-MHz sampling clock for the ADS4249. This file is located in the TSW1265 GUI installation directory in the folder "Configuration Files" and is named *250MHz_onboard_clock.txt*. The file can be loaded by clicking the *Load* button, navigating to the correct folder, selecting the file, and clicking *Ok*. Click *Send All* a few times to make sure the board is configured properly. The LED labeled *D1* on the board will light up indicating that the PLL is locked.
- Onboard Clock using Dual PLL Mode: This mode of operation allows the user to provide a low frequency reference through the CLKIN1 connector to generate a synchronized, higher frequency sampling clock. The reference can come from any source, such as a 10-MHz reference from a piece of test equipment. This allows for synchronization between all signal sources and for coherent sampling. In order to use this mode, a VCXO needs to be installed at Y2 or Y4. Additionally, R69, R66, C168, C167 should be removed and install 50 Ω for R97, 0.1 uF for C73, and 0.1 uF for C167. The user must update the loop filters if a change in the reference or VCXO occurs. Use the Clock Design Tool (http://www.ti.com/tool/clockdesigntool) to design the loop filters and PLL settings based on the reference, VCXO, and output frequencies.

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3.4.2 Changing the RF and LO Frequencies

The default RF frequency range is 1700 MHz to 2200 MHz. The default LO frequency range is 1750 MHz to 2700 MHz. These ranges are set by the MAX19995A downconversion mixer. The board was designed to work with most of the Maxim and Skyworks downconversion mixers, therefore the mixer can be replaced with a different one that has different frequency ranges. The passive components will also need to be changed based on the data sheet of the part.

3.4.3 Changing the IF Frequency

The IF frequency of the TSW1265 is fixed due to the LC filters on the board. There is a filter between the mixer and the LMH6521 and a filter between the LMH6521 and the ADS4249. These filters provide an overall 1-dB bandwidth of 75 MHz centered at 187.5 MHz. The filter between the mixer and the LMH6521 is a second-order LC filter with a 1-dB bandwidth of approximately 140 MHz. The filter between the LMH6521 and the ADS4249 is a fourth order with a bandwidth of 75 MHz.

To change the IF frequency of the TSW1265, the user needs to change the filters that are implemented on the board. There are many tools available for download online that will calculate a filter design based on frequency and ripple requirements. Use these tools to get a starting point for the filter design. Due to parasitic capacitance and inductance on the board, the user must interactively tune the filter to achieve the desired response. Once the filter has been designed for one channel, it can be implemented on the other channel as well. Note that the transformer following the IF filter is in place to correct for any imbalances between the two legs of the differential signal. For more detailed information about how to design the IF filters see the application note titled "Band-Pass Filter Design Techniques for High-Speed ADCs" (SBAA195).

3.4.4 Using the High-Speed Connector to Set the DVGA Gain

The high-speed connector (J1) on the TSW1265 board has connections that allow a user to change the gain of the LMH6521 quickly. Pins 105, 107, 109, 111, 113, 115, 117, and 119 on the connector can be used to pass the gain and latch signals from an FPGA to the DVGA. To use this feature, the jumper JP9 needs to be moved between pins 2 and 3. This configures the CPLD to route the gain from the connector rather than from the USB connection.

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- · Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

[Important Notice for Users of EVMs for RF Products in Japan]

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

- 1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
- 3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

- 1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
- 2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
- 3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
- 4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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