ADS5296A, 4-Channel 200-MSPS, and 8-Channel 80-MSPS, Analog-to-Digital Converter Evaluation Module

This user's guide gives a general overview of the ADS5296A evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS5296A analog-to-digital converters (ADC). The ADS5296A EVM provides a platform for evaluating the ADC under various signal, clock, reference, and ADC output formats.

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1 Quick View of Evaluation Setup

Figure 1 is an overview of the evaluation setup that includes the ADS5296A EVM, TSW1400 data capturing card, external equipment, personal computer (PC), and software requirements.

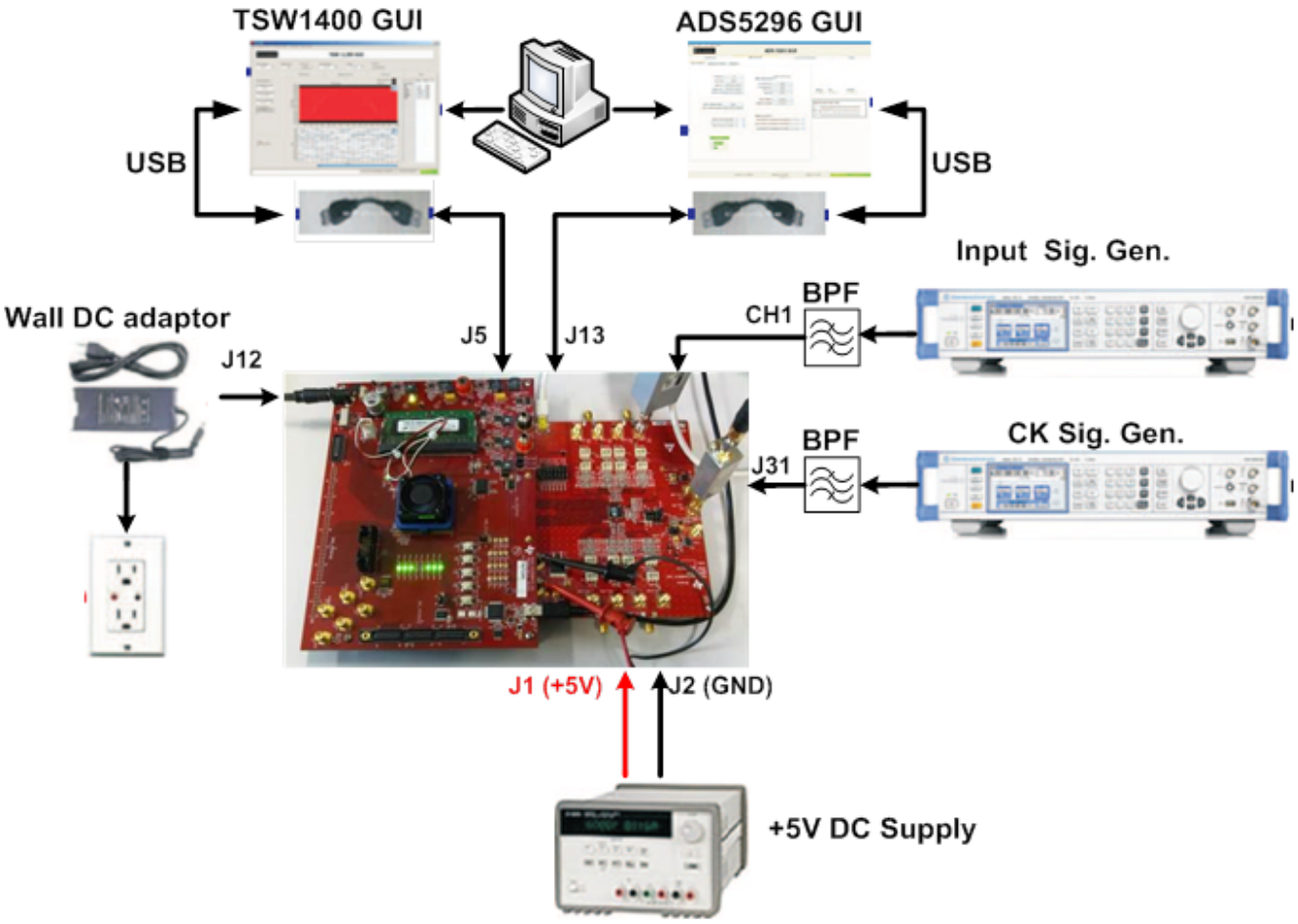

Figure 1. Evaluation Setup

TSW1400 EVM: The high-speed LVDS deserializer board is required for capturing data from the ADS5296A EVM and its analysis using the TSW1400 graphical user interface (GUI), called High Speed Data Converter Pro (*HSDCpro*). For more information pertaining to the TSW1400 EVM, see: http://focus.ti.com/docs/toolsw/folders/print/tsw1400evm.html

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, band-pass filters (BPF) are required in signal and clock paths to attenuate the harmonics and noise from the generators. (***Note: Functionality of the setup shown in Figure 1, including the LVDS interface between the ADS5296A and FPGA on the capture card, can be tested using the on-chip test pattern generator and the on-board crystal oscillator for an ADC sampling clock source.***)

Power Supply: A single +5-V supply powers the ADS5296A EVM through connectors located at **J1** and **J2**. The supply for the ADS5296A device is derived from this +5 V supply. The power supply must be able to source up to 1.5 A. The TSW1400 EVM is powered through an AC adaptor provided with its EVM kit.

USB Interface to PC: The USB connections from the ADS5296A EVM and TSW1400 EVM to the personal computer (PC) are used for communication from the GUIs to the boards. Section 2 explains the TSW1400 and ADS5296 GUI installation procedure.

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2 GUI Software Installation

The ADS5296A EVM and the TSW1400 EVM both require software installations. The following two sections explain where to find and how to install the software properly. Ensure that no USB connections are made to the EVMs until after the installations are complete.

2.1 TSW1400 EVM GUI Installation (High Speed Data Converter Pro (HSDCpro))

From the Texas Instruments website, www.ti.com, search for TSW1400. Under Technical Documents, one will find a ***Software*** section from which ***High Speed Data Converter Pro GUI Installer*** can be downloaded and saved (slwc107e.zip or higher).

- Unzip the saved folder and run the installer executable to obtain the menu shown in Figure 2.
- Click the *Install* button.

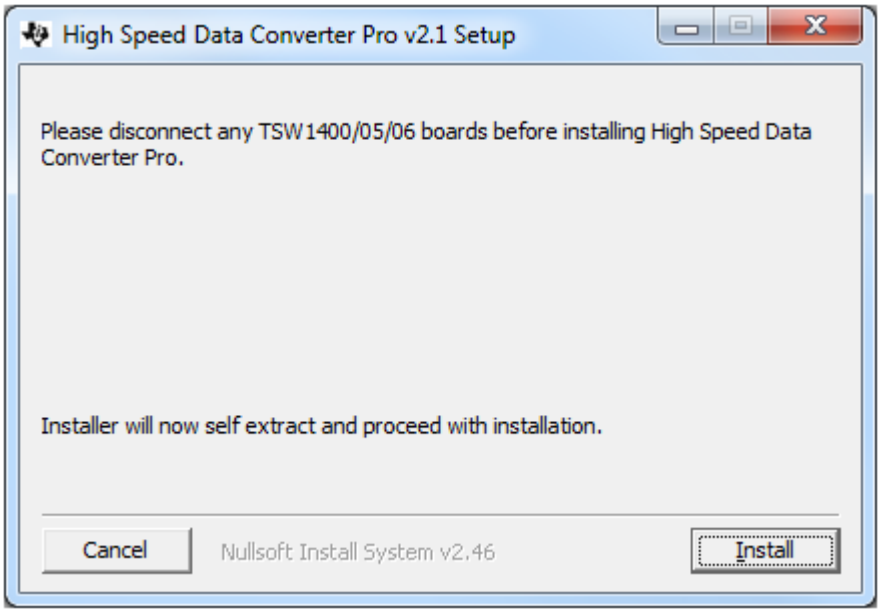

Figure 2. HSDCpro Install (a)

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- Set the destination directories, or leave as default, for the TSW1400 GUI installation and press the *Next* button as shown in Figure 3.

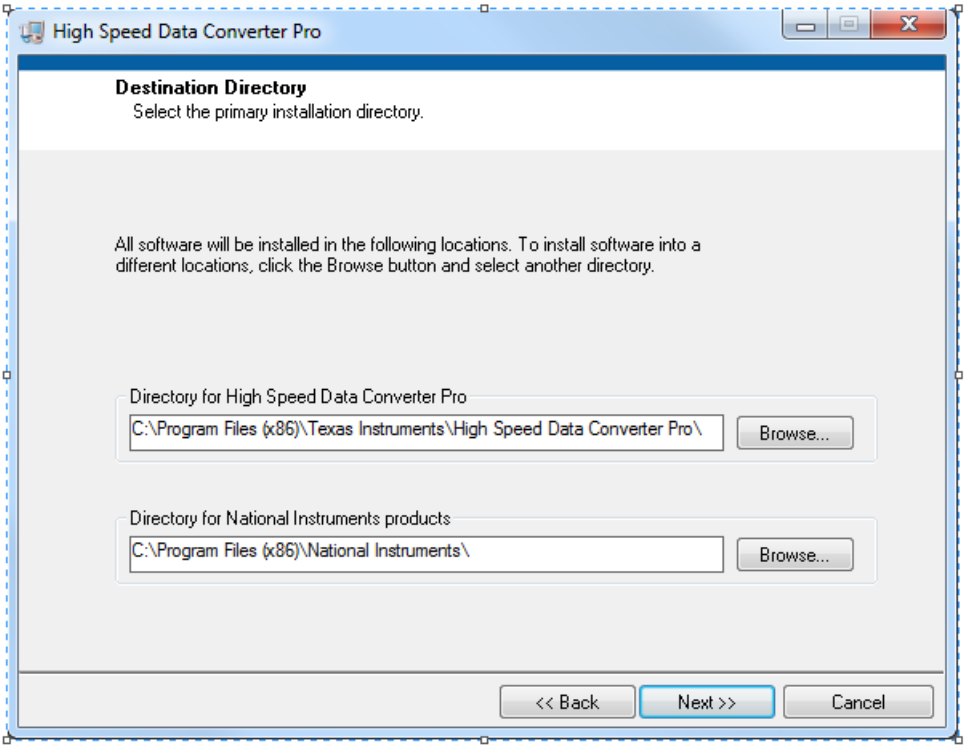

Figure 3. HSDCpro Install (b)

- Read the License Agreement from Texas Instruments and select *I accept the License Agreement* and press the *Next* button as shown in Figure 4.

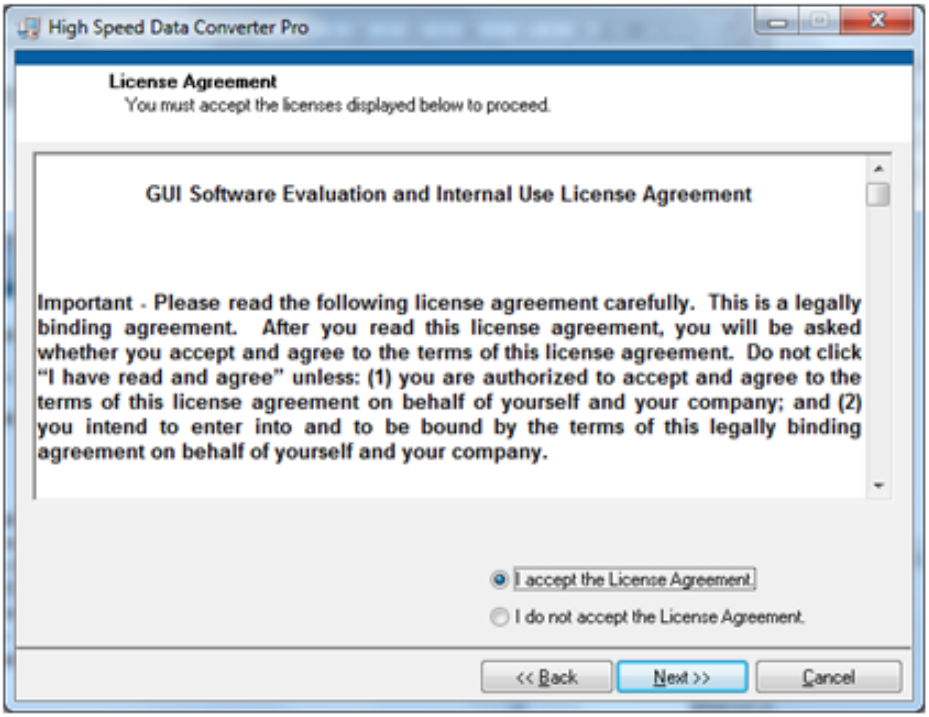

Figure 4. HSDCpro Install (c)

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- Read the License Agreement from National Instruments and select *I accept the License Agreement* and press the *Next* button as in Figure 5.

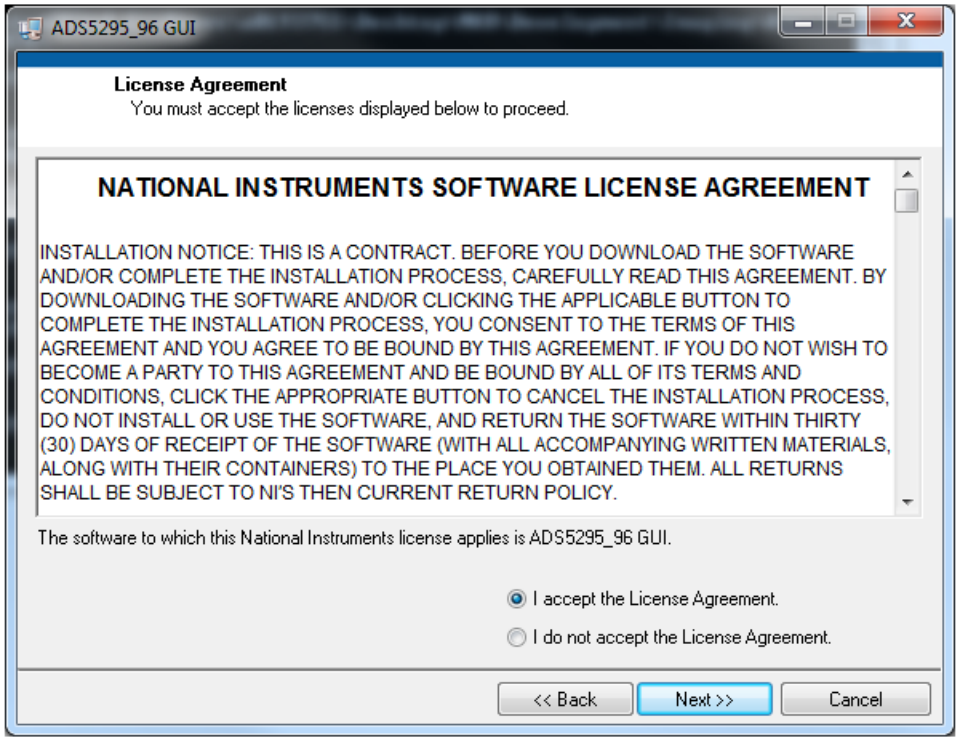

Figure 5. HSDCpro Install (d) 80

- Press the Next button as shown in Figure 6.

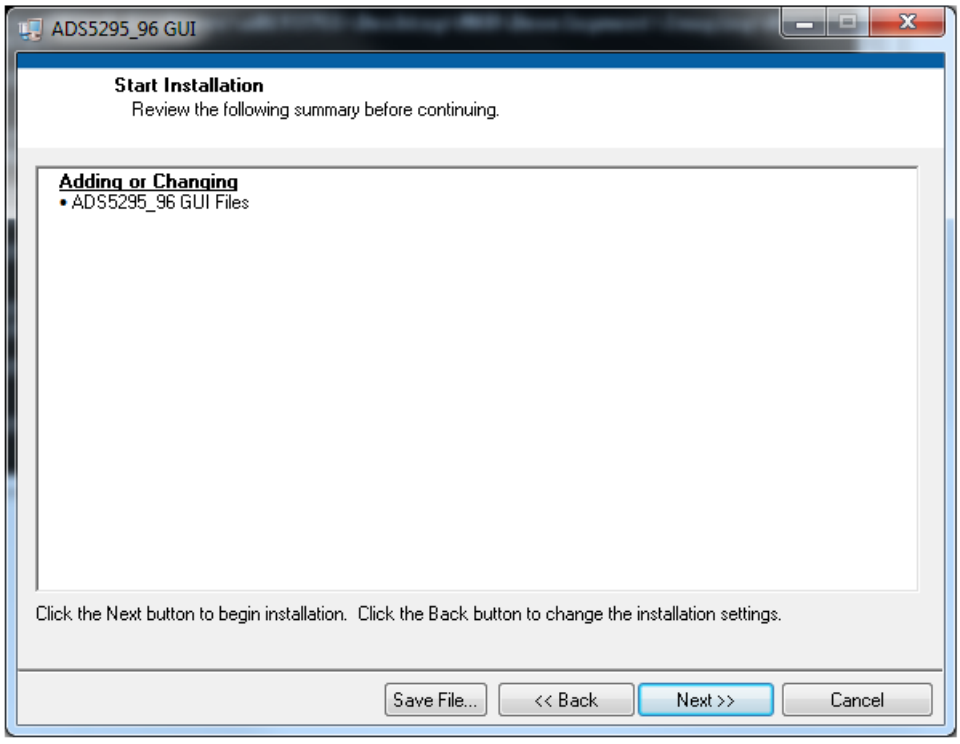

Figure 6. HSDCpro Install (e)

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- The window shown in Figure 7 should appear, indicating that installation is in progress.

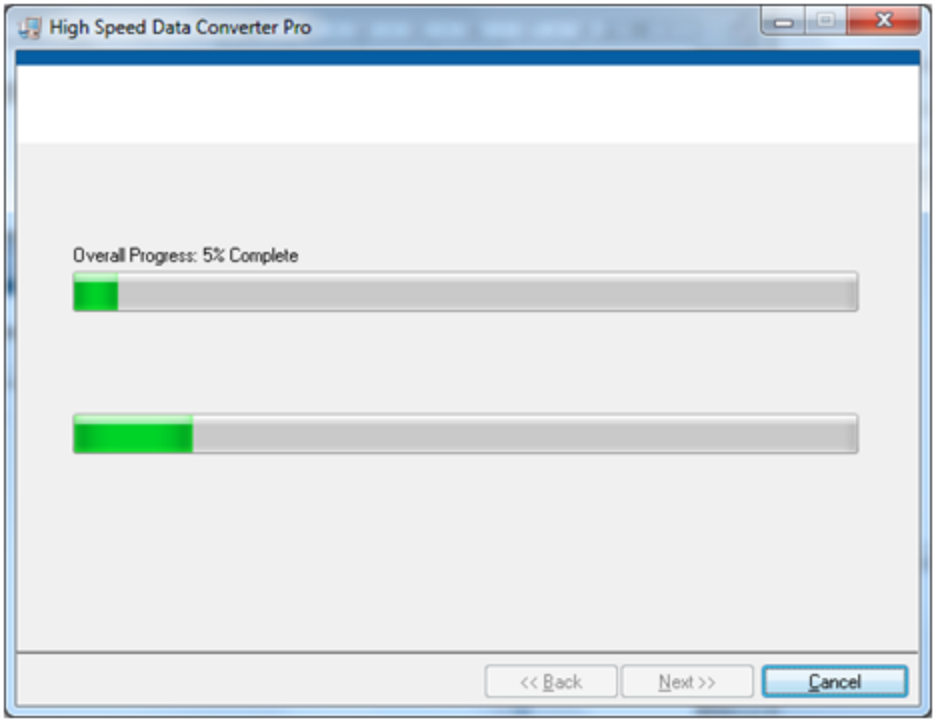

Figure 7. HSDCpro Install (f)

- The window shown in Figure 8 appears indicating *Installation Complete*. Press the *Next* button.

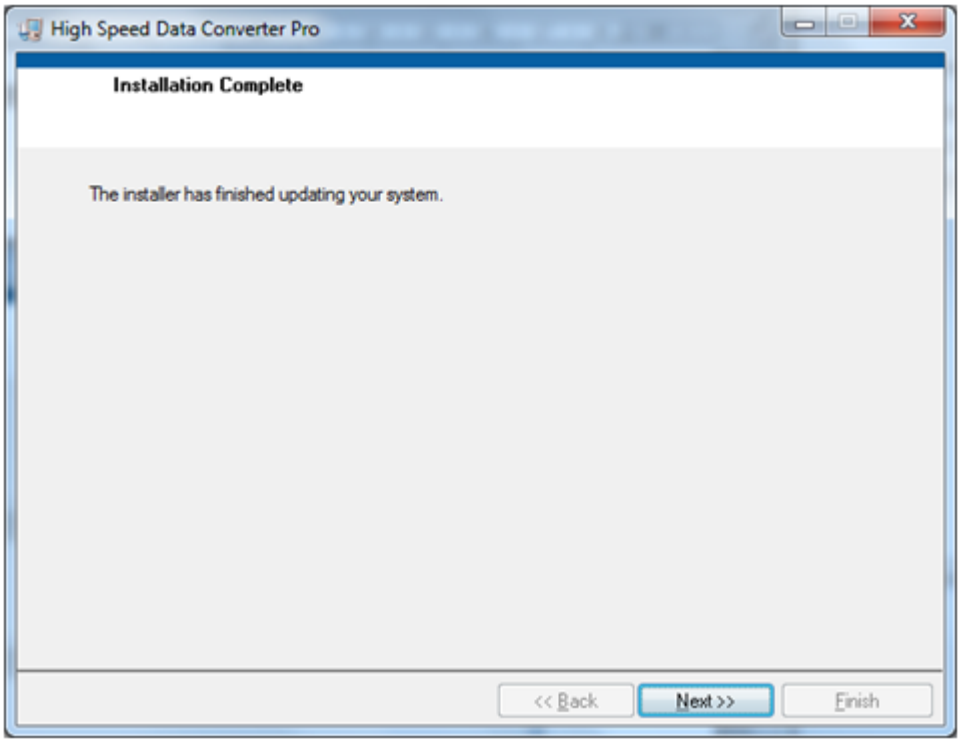

Figure 8. HSDCpro Install (g)

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- The window in Figure 9 appears briefly to complete the process.

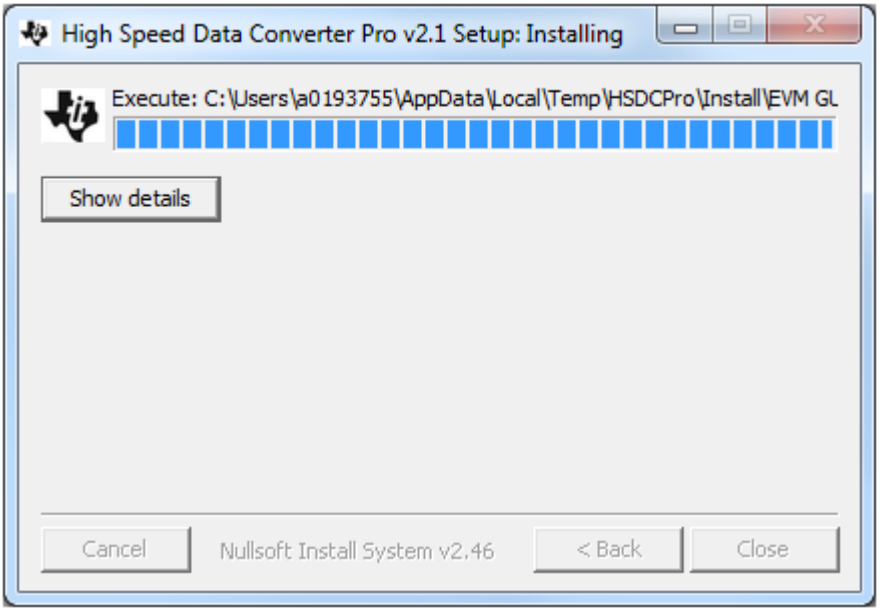

Figure 9. HSDCpro Install (h)

- As shown in Figure 10, a computer restart might be requested depending on whether or not the PC already has the National Instruments' MCR installer. If requested, hit the *Restart* button to complete the installation.

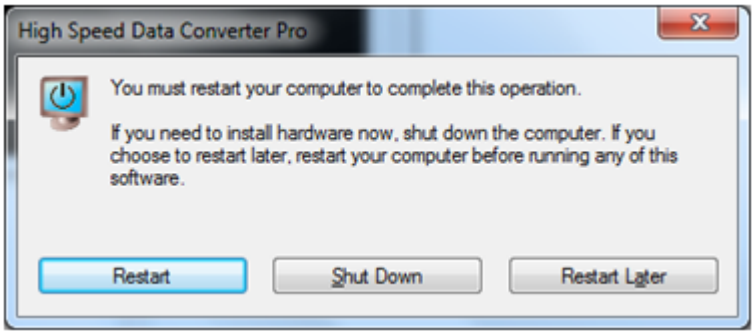

Figure 10. HSDCpro Install (i)

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2.2 ADS5296A EVM GUI Installation

Both the ADS5295 and ADS5296A ADCs from Texas Instruments share the same GUI installer. Thus, references to *ADS5295_96* during the installation exist. From the Texas Instruments website, www.ti.com, search for **ADS5296A EVM**. Clicking on the hyperlink in the table will lead to another link titled **ADS5295 and ADS5296 GUI Installer, v2.1 (Rev. B)**. Click on this link to download and save the zipped file (slac547b.zip).

- Unzip the folder and run the *Setup.bat* file as administrator by right clicking on it and selecting *Run as administrator* as shown in Figure 11.

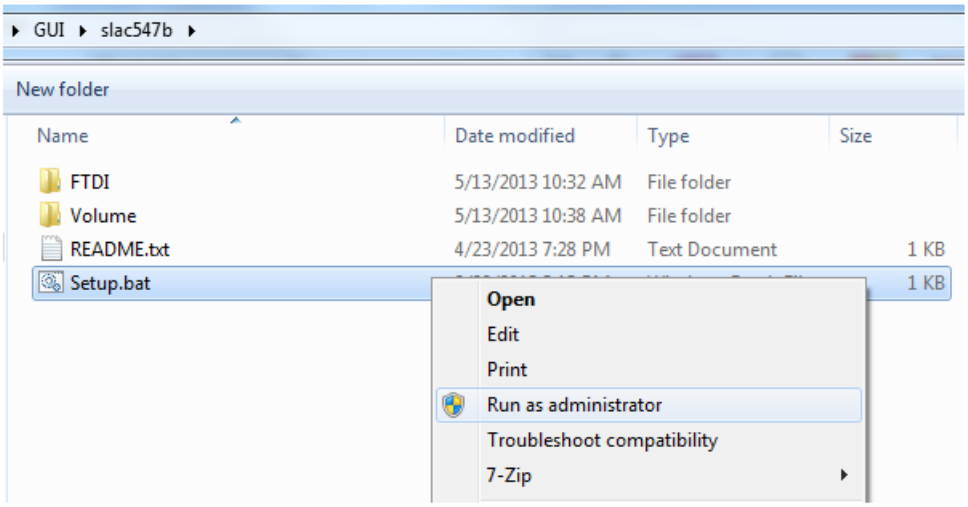

Figure 11. ADS5296 GUI Install (a)

- Set the destination directories for the ADS5295_96 GUI installation or leave as default and press the *Next* button as shown in Figure 12.

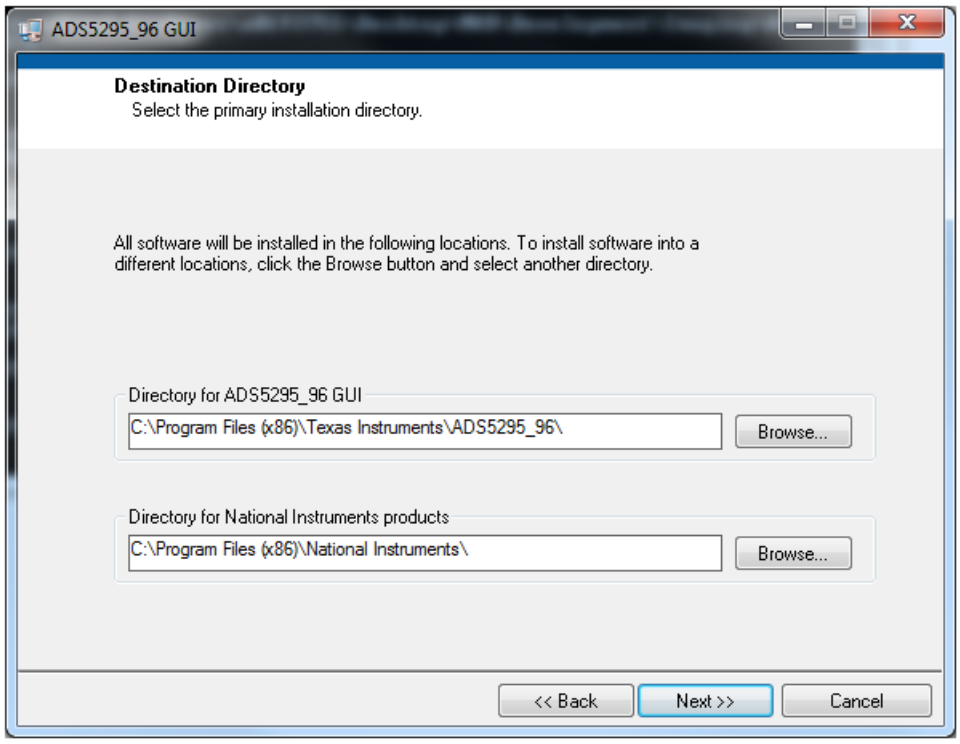

Figure 12. ADS5296 GUI Install (b)

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- Read the License Agreement from Texas Instruments and select the *I accept the License Agreement* button and then press the *Next* button as shown in Figure 13.

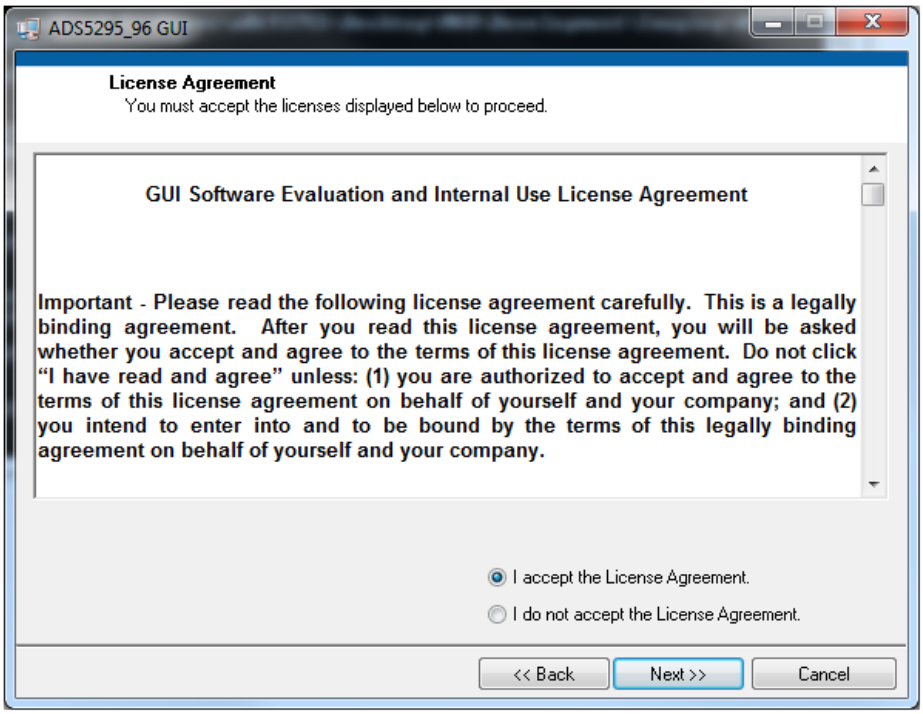

Figure 13. ADS5296 GUI Install (c)

- Read the License Agreement from National Instruments and select the *I accept the License Agreement* button and then press the *Next* button as shown in Figure 14.

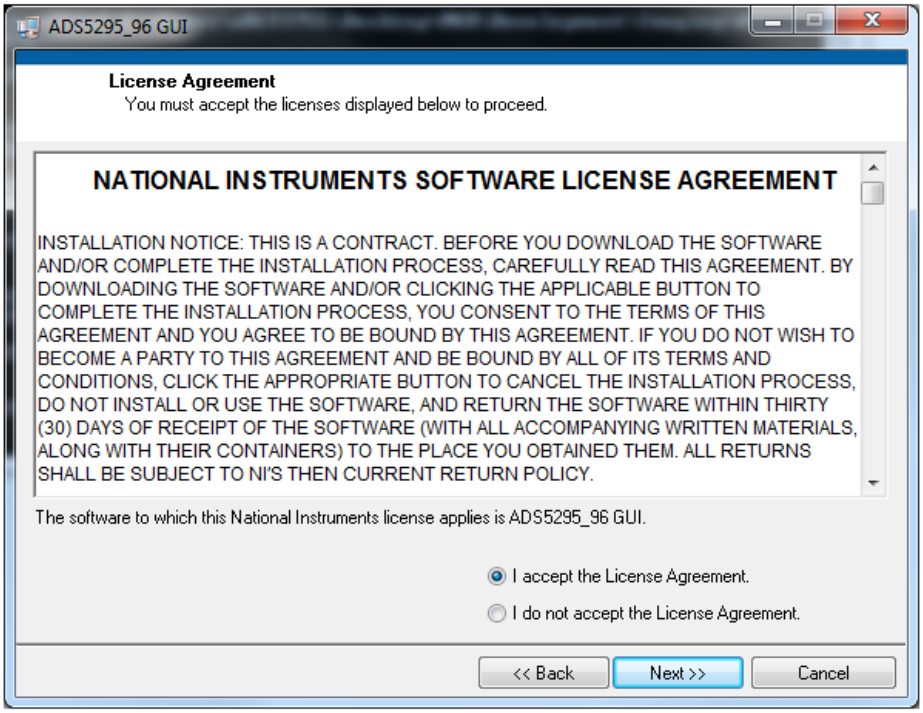

Figure 14. ADS5296 GUI Install (d)

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- To begin the installation, press the *Next* button as shown in Figure 15.

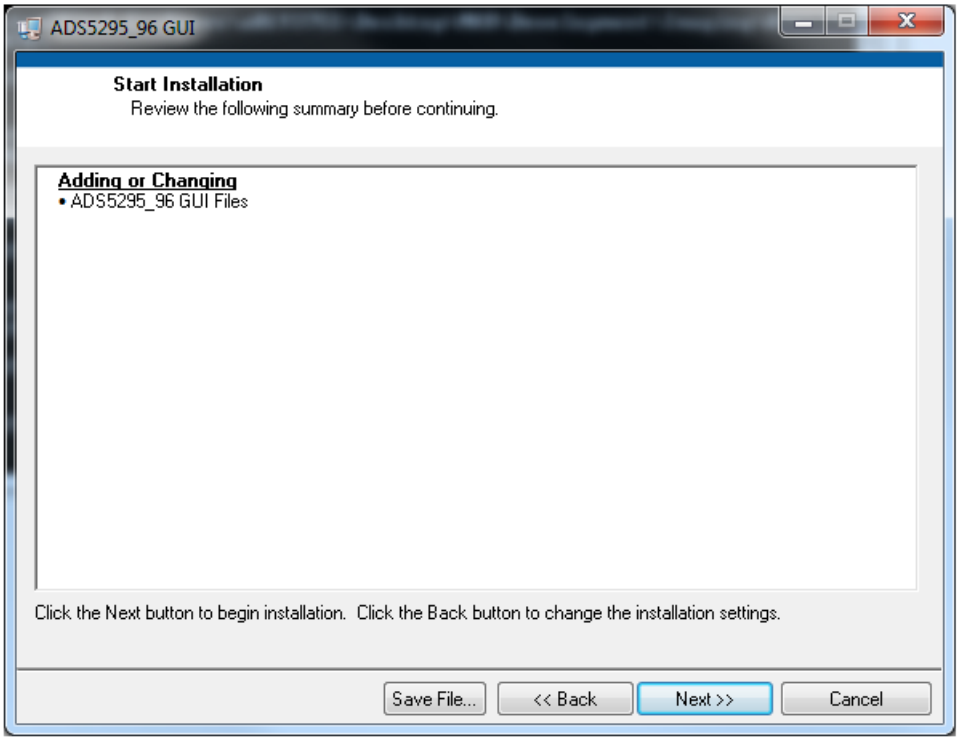

Figure 15. ADS5296 GUI Install (e)

- The window shown in Figure 16 should appear showing that installation is in progress.

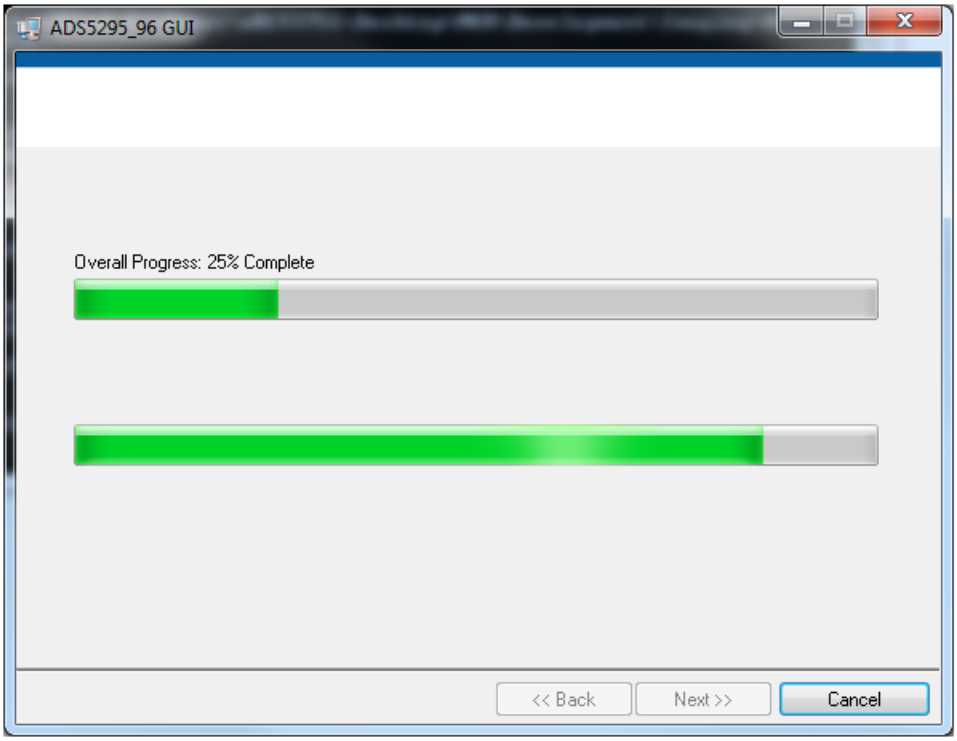

Figure 16. ADS5296 GUI Install (f)

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- Upon completion of the installation, the window in Figure 17 appears. Press the *Finish* button to continue.

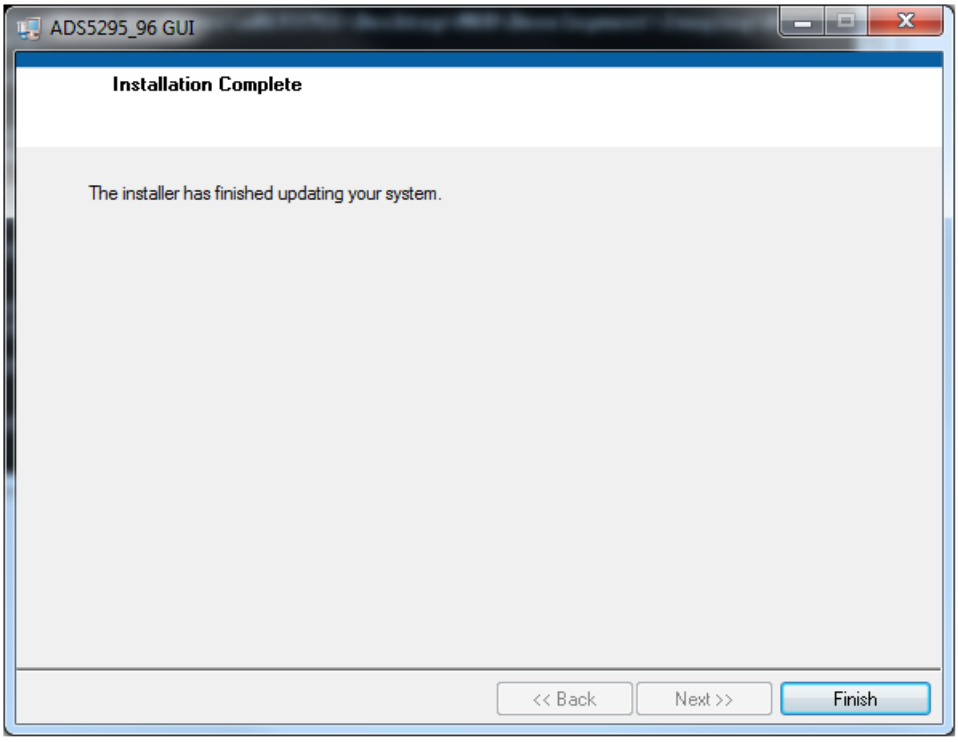

Figure 17. ADS5296 GUI Install (g)

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3 Hardware and EVM Setup for Testing ADS5296A

This section outlines the external connections required for ADS5296A EVM as well as the default configuration of the EVM's 3-pin headers and 0-Ω jumper resistors with an explanation of configuration options.

3.1 External Connections

The connections shown in Figure 18 should be made for proper hardware setup (*Note: Testing the LVDS interface between the ADS5296A EVM and the TSW1400 EVM can be performed using a RAMP function generated within the ADS5296A device in lieu of the signal source listed in item 7 below. Also, an on-board 80-MHz crystal oscillator (XTAL) can provide the ADC sampling clock in lieu of the signal source listed in item 6 below. This configuration is only recommended for testing the RAMP function as low phase noise filtered signal sources must be provided to both the ADC clock input and the ADC analog inputs for measuring device performance*).

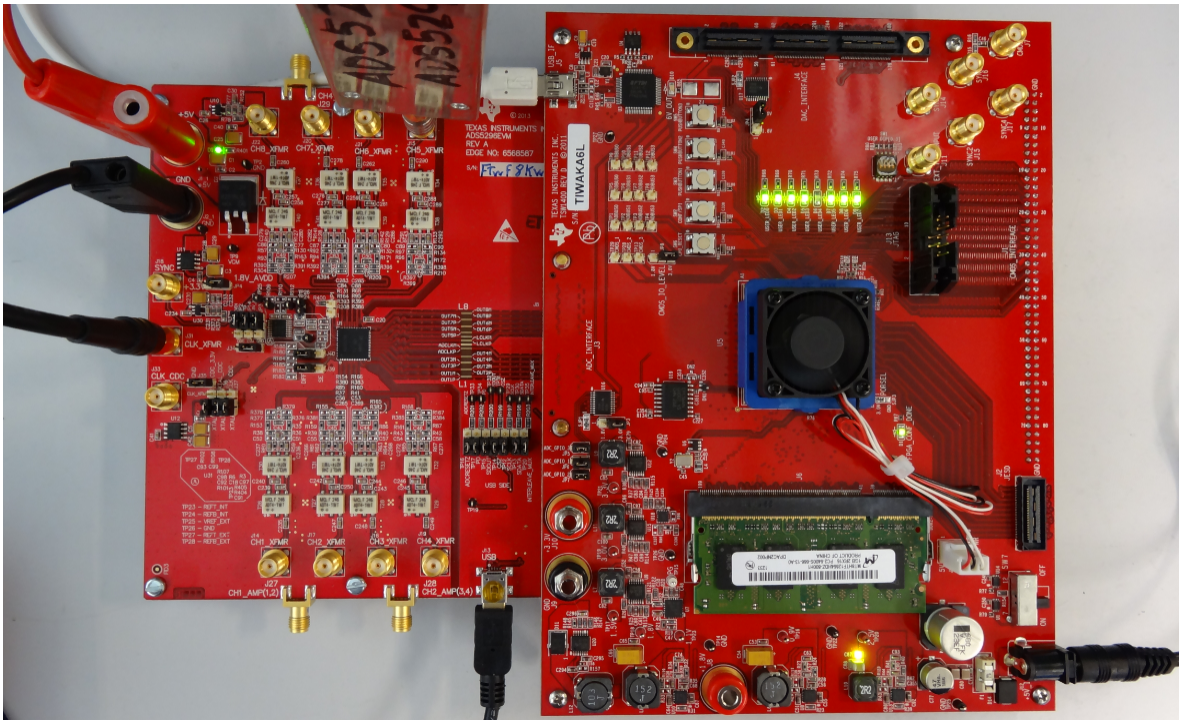

Figure 18. TSW1400 and ADS5296A EVM Setup

1. Mate the TSW1400 EVM at connector **J3** to the ADS5296A EVM at connector **J8** through the high speed ADC interface connector.
2. Connect the DC +5-V output of the provided AC-to-DC power supply to **J12 (+5V_IN)** of the TSW1400 EVM and the input of the power supply cable to a 110–230 VAC source.
3. Connect +5-V DC power supply leads to connectors **J1 (VCC)** and **J2 (GND)** of the ADS5296A EVM.
4. Connect the USB cable from PC to **J13 (USB)** of ADS5296A EVM
5. Connect the USB cable from PC to **J5 (USB_IF)** of the TSW1400 EVM. (*Note: it is recommended that the PC USB port be able to support USB2.0. If unsure, always chose the USB ports at the back of the PC chassis over ones located on the front or sides.*)
6. Supply an ADC clock signal to SMA **J31 (CLK_XFMR)** of the ADS5296A EVM (that is, +5 dBm, 80 MHz) but turn off the source as the on board 80-MHz crystal oscillator (XTAL) will be used as a clock source for the initial testing.
7. Supply an analog input signal to SMA **J15 (CH5_XFMR)** of the ADS5296A EVM (that is, +10 dBm, 10 MHz).

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3.2 ADS5296A EVM Header Configuration

The ADS5296A EVM is flexible in its configurability through the use of 3 pin headers. The default configuration of the EVM is set to facilitate initial testing requiring minimal bench equipment by providing an 80-MHz ADC sampling clock from an on-board crystal oscillator (XTAL). Table 1 describes the purpose of the 3-pin headers on the EVM while Figure 19 shows the default position. With this configuration, the XTAL, at reference designator **U2**, is powered and providing an 80-MHz signal to a transformer which, in turn, provides a differential sampling clock to the DUT. Table 1 also shows that the default method for selecting even or odd channels in interleaving mode is done through the ADS5296 GUI (**JP14**) as opposed to jumper **JP2** on the EVM.

Table 1. ADS5296A EVM Header Configuration

Jumper	Default Config	Pin 1 Silkscreen	Pin 3 Silkscreen	Circuit	Description
JP4	short pins 1-2	1.8V_AVDD	+3.3V	Power Supply	Power Supply for DUT: ALWAYS 1.8V_AVDD
J35	short pins 2-3	GND	CDC_3.3V	ADC Sampling Clock	Selects Power supply for CDC chip and on-board XTAL oscillator: (1) GND or (3) +3.3V
J38	short pins 1-2	XTAL	CLK_XFMR	ADC Sampling Clock	Selects ADC sampling clock source: (1) XTAL osc. or (3) external source input to SMA J31 CLK_XFMR
J36	short pins 1-2	XTAL	XTAL_CDC	ADC Sampling Clock	Selects path for XTAL osc. signal: (1) to transformer or (3) to CDC input
J37	short pins 1-2	XTAL	CLK_CDC	ADC Sampling Clock	Selects input source to CDC input: (1) XTAL osc. or (3) external source input to SMA J33 CLK_CDC
J39	short pins 2-3	SE	DIFF	ADC Sampling Clock	Selects ADC sampling clock configuration: (1) Single-ended (3) Differential (must match J40)
J40	short pins 2-3	SE	DIFF	ADC Sampling Clock	Selects ADC sampling clock configuration: (1) Single-ended or (3) Differential (must match J39)
JP2	short pins 1-2	EVEN	ODD	INTERLEAVE_MUX pin	Selects analog input channels to be interleaved: (1) EVEN channels or (3) ODD channels
JP14	short pins 1-2	FTDI	EVM	INTERLEAVE_MUX	Selects source of EVEN/ODD select: (1) GUI control or (3) INTERLEAVE_MUX pin control
JP3	short pins 1-2	1.8V_AVDD	GND	SYNC	SYNC (Note: JP3 and J34 share silkscreen "GND")
J34	short pins 2-3	5V	GND	EXT_REF AMP	Selects Power supply for EXT_REF AMP: (1) +5V or (3) GND (Note: JP3 and J34 share silkscreen "GND")
TP16	short pins 1-2	ADCRESETZ	n/a	SPI	Selects SPI control: (1) GUI control
TP17	short pins 1-2	PD	n/a	SPI	Selects SPI control: (1) GUI control
TP15	short pins 1-2	SDOUT	n/a	SPI	Selects SPI control: (1) GUI control
TP14	short pins 1-2	CSZ	n/a	SPI	Selects SPI control: (1) GUI control
TP12	short pins 1-2	SCLK	n/a	SPI	Selects SPI control: (1) GUI control
TP13	short pins 1-2	SDATA	n/a	SPI	Selects SPI control: (1) GUI control
TP20	short pins 1-2	INTERLEAVE_MUX	n/a	SPI	Selects SPI control: (1) GUI control

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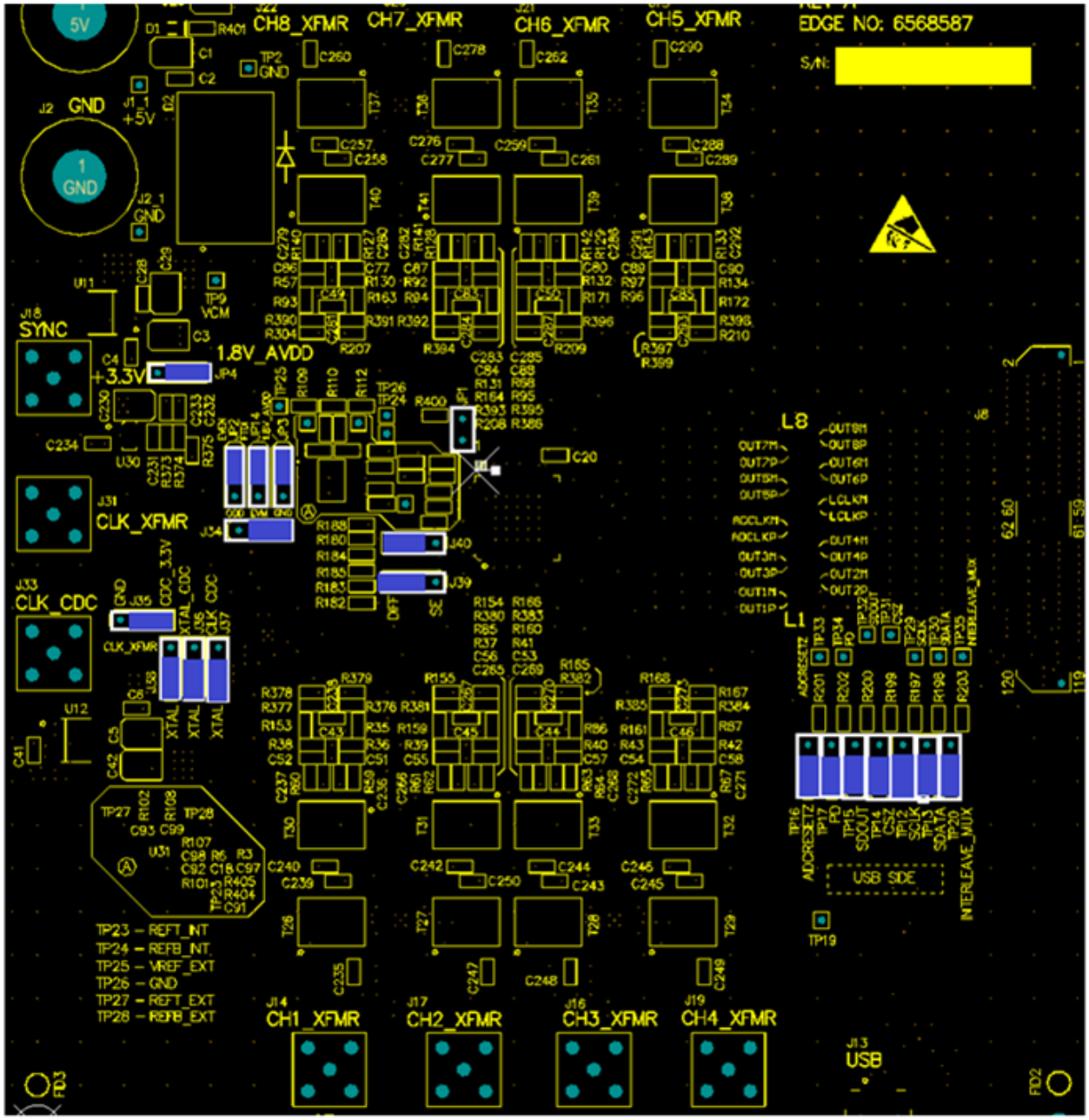

Figure 19. ADS5296A EVM Default Header Configuration

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3.3 ADS5296A EVM 0-Ω Jumper Configuration

The ADS5296A can be used an Octal-channel non-interleaving ADC or as a Quad-channel interleaving ADC. The ADS5296A EVM is delivered in a configuration that allows testing both modes without any changes required by the user, except through the software GUI.

The ADS5296A EVM has eight SMAs vertically mounted on the topside of the board corresponding to eight analog input channels labeled **CHx_XFMR**, where x = 1 to 8, as shown in colored boxes of Figure 20. Channels 5, 6, 7, and 8, highlighted by the yellow box, are configured for octal non-interleaving mode and are driven through the back-to-back transformers on the top side of the board, while channels 1, 2, 3, and 4, highlighted by the blue box, are disconnected from the DUT. This is evident by the installed 0-ohm jumper resistors at **R210**, **R399**, **R209**, **R386**, **R208**, **R394**, **R207**, and **R304** and by the uninstalled 0-ohm resistor jumpers at **R378**, **R379**, **R155**, **R154**, **R166**, **R165**, **R168**, and **R167**, respectively.

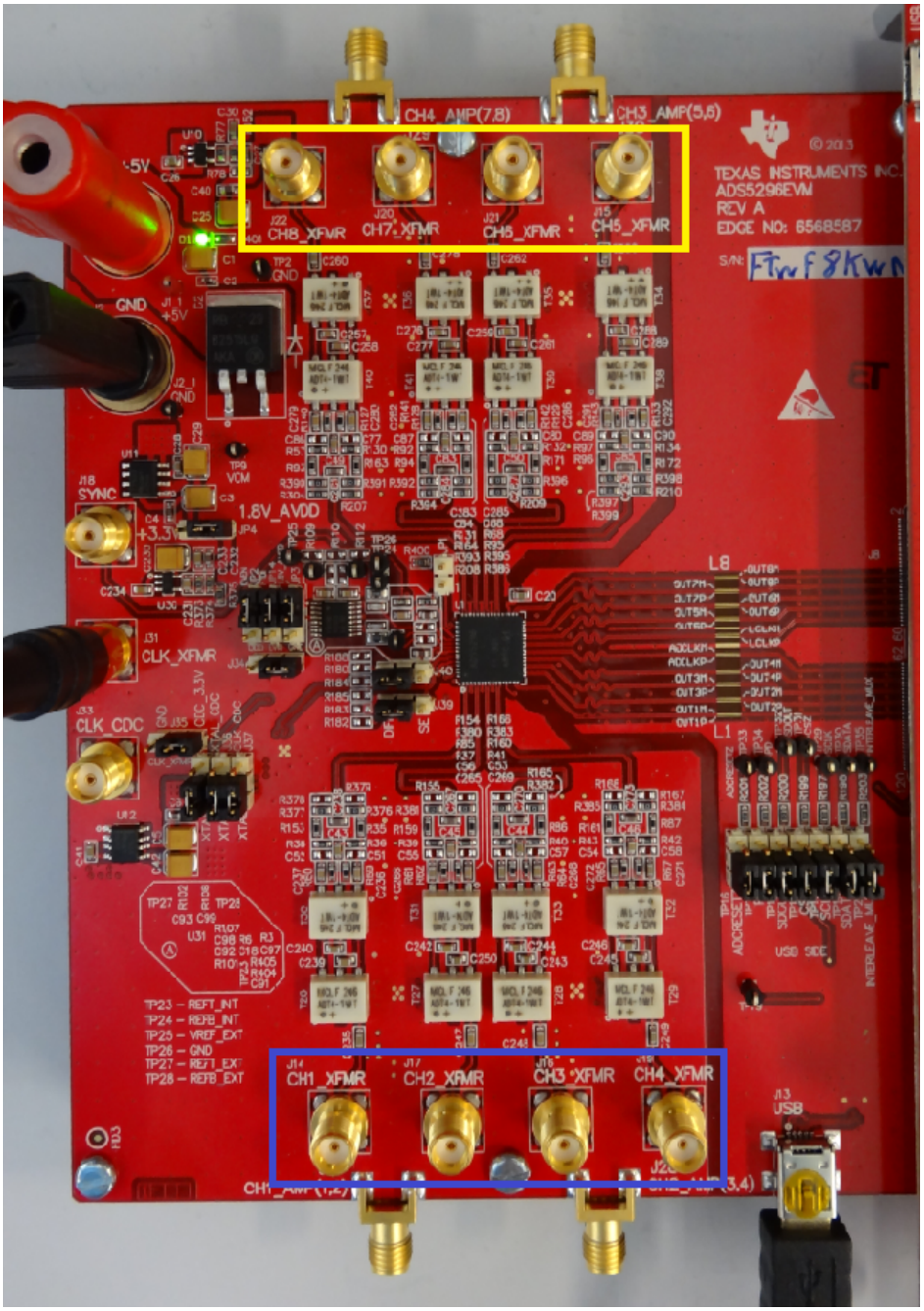

Figure 20. ADS5296A EVM Octal Non-Interleaving Mode Analog Input SMAs

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The ADS5296A EVM also has four side-mounted SMAs corresponding to four analog input channels labeled **CH1_AMP(1,2)**, **CH2_AMP(3,4)**, **CH3_AMP(5,6)**, **CH4_AMP(7,8)** as shown in colored boxes of Figure 21. Channels 1 and 2, highlighted by the yellow box, are configured for quad non-interleaving mode and are driven through the amplifiers on the back side of the board, while channels 3 and 4, highlighted by the blue box, are disconnected from the DUT. This is evident by the installed 0-ohm jumper resistors on the backside at **R80**, **R81**, **R324**, and ADS5296A, 4-Channel 200-MSPS, and 8-Channel 80-MSPS, Analog-to-Digital Converter Evaluation Module, and by the uninstalled 0-ohm resistor jumpers on the backside at **R346**, **R348**, **R368**, and **R370**, respectively. When an input signal is provided SMA **J27**, **CH1_AMP(1,2)**, a switch internal to the ADS5296A, selects whether ADC channel 1 or ADC channel 2 is sampled. The selection depends on the state of GUI control **ODD_EVEN_SEL** or on the position of header **JP2**.

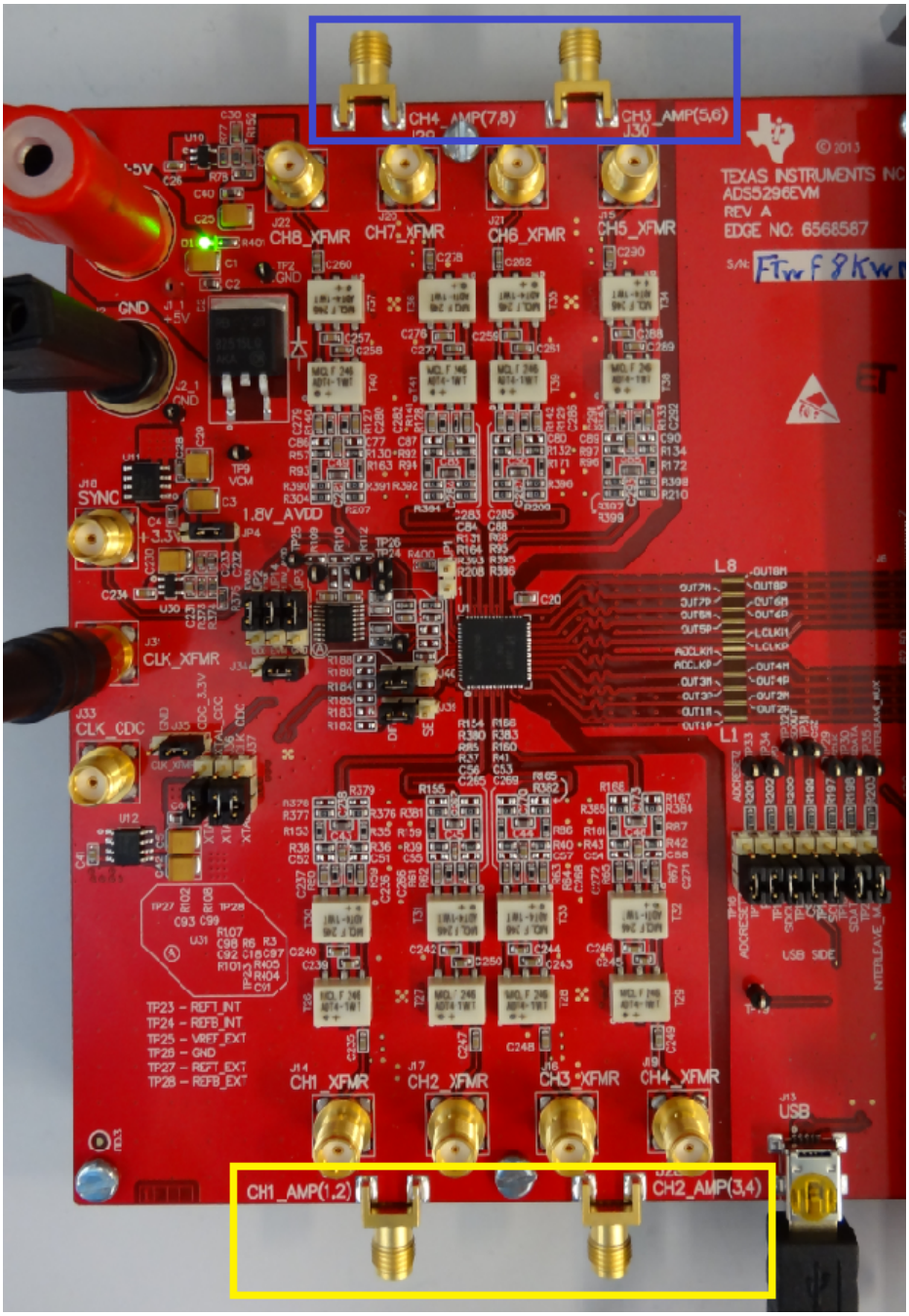

Figure 21. ADS5296A EVM Quad Interleaving Mode Analog Input SMAs

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4 Testing ADS5296A EVM

This section outlines the following three test cases with a sub-section dedicated to each case:

- Capturing a RAMP test pattern
- Capturing a Sinusoidal Input in Octal Non-Interleaving Mode
- Capturing a Sinusoidal Input in Quad Interleaving Mode

Only the minimal software GUI settings required to achieve the above tests will be described in this section. For a detailed explanation of the ADS5296 software GUI and all its features, please see Section 5. For a detailed explanation of the *High Speed Data Converter Pro* software GUI, please consult the TSW1400 User's Guide (SLWU079B), available on the Texas Instruments website.

4.1 TSW1400 and ADS5296 GUI Setup

1. With the setup outlined in Figure 18 established, launch the *High Speed Data Converter Pro* GUI. The GUI should automatically detect the serial number of the TSW1400 EVM, connected as shown in Figure 22. Click on *OK*.

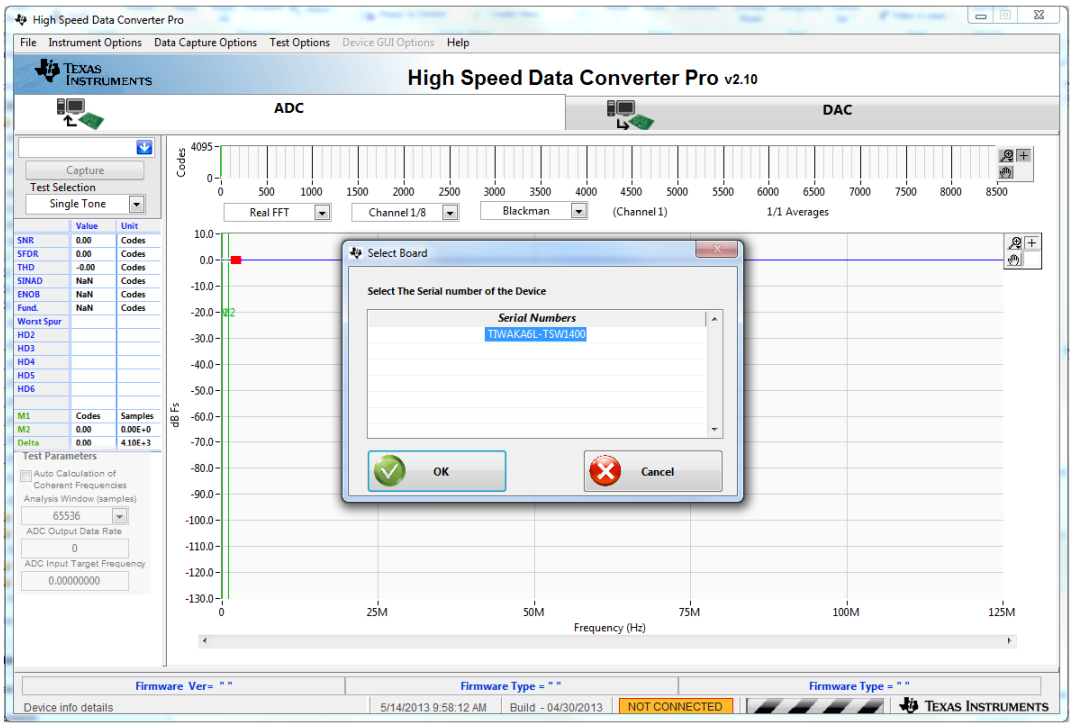

Figure 22. TSW1400 GUI Setup (a)

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The message shown in Figure 23 will appear. Click **OK.**

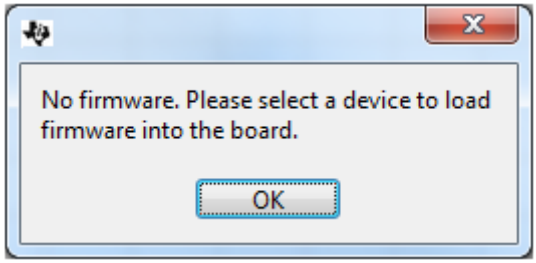

Figure 23. TSW1400 GUI Setup (b)

If instead, the message shown in Figure 24 appears, it indicates that the USB connection to the TSW1400 EVM is not present. Click *OK*, then establish a USB connection and repeat step 1.

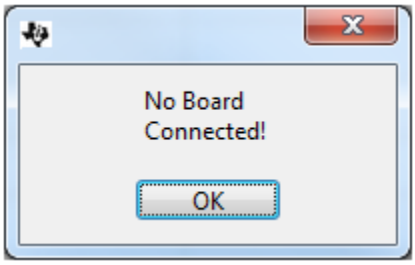

Figure 24. TSW1400 GUI Setup (c)

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2. Select a device by clicking on the Blue arrow in the upper left corner of the *HSDCpro* GUI. Scroll down and select *ADS5296* as shown in Figure 25.

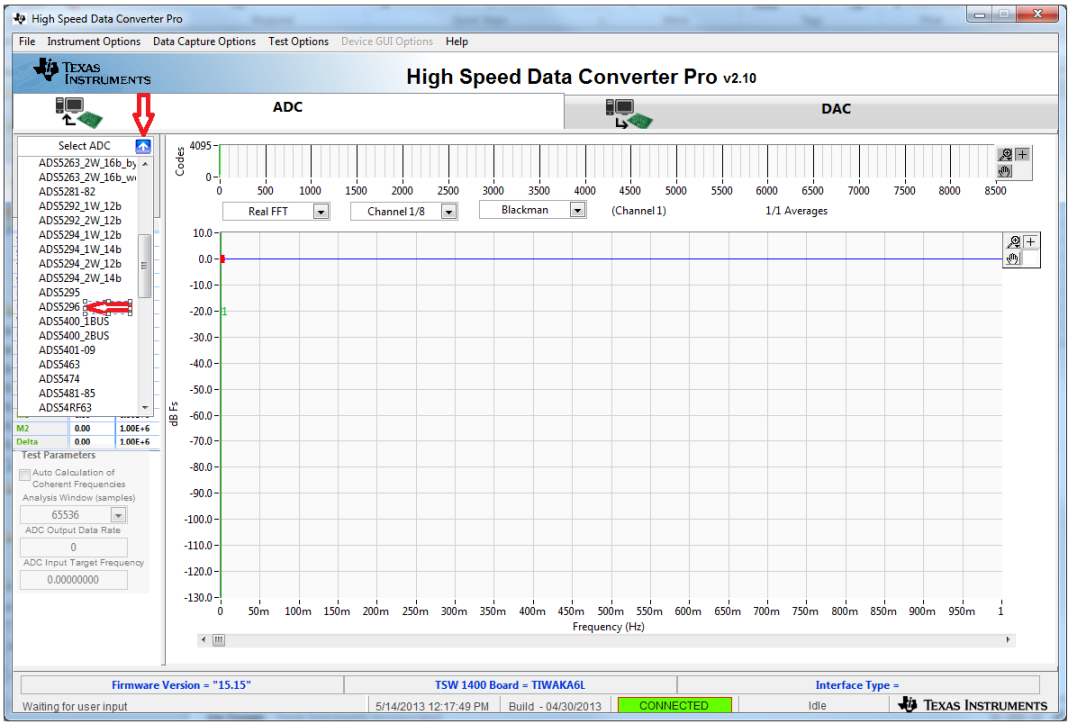

Figure 25. TSW1400 GUI Setup (d)

Click the *Yes* button to update the ADC firmware on the TSW1400 FPGA as depicted in Figure 26.

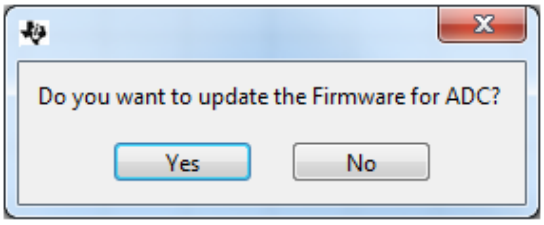

Figure 26. TSW1400 GUI Setup (e)

While the firmware is being loaded into the TSW1400 FPGA, the menu shown in Figure 27 will appear.

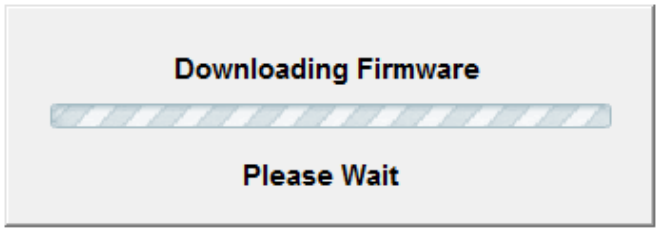

Figure 27. TSW1400 GUI Setup (f)

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Once loaded, the plug-in ADS5296 GUI will appear as a new tab within the *HSDCpro* GUI as shown in Figure 28.

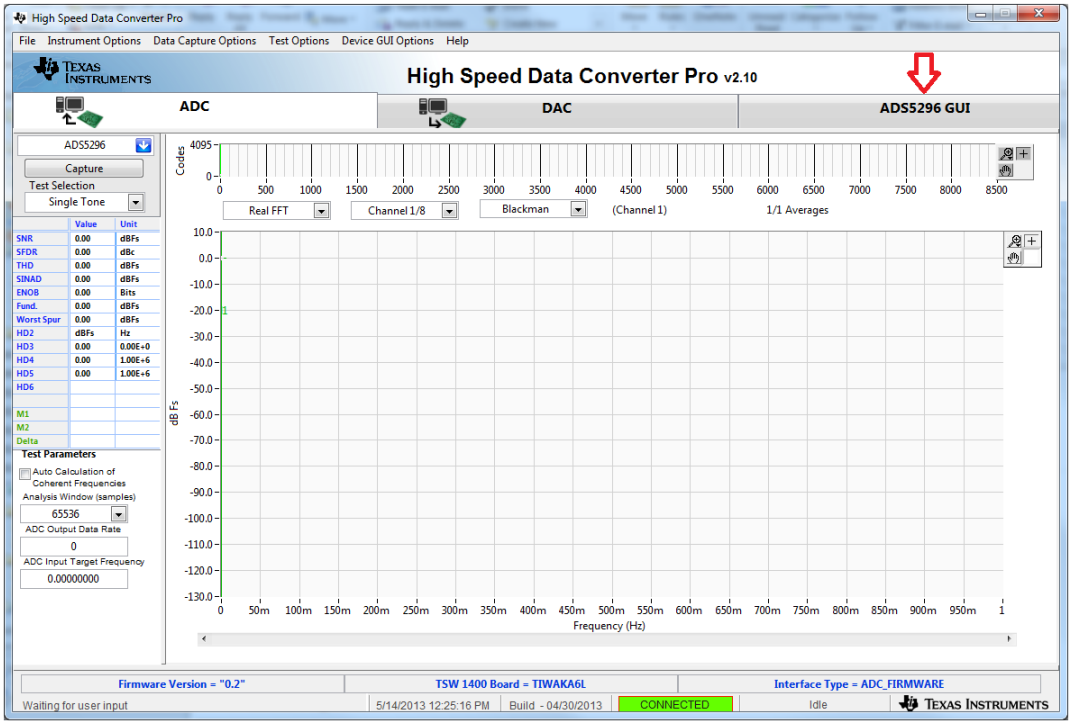

Figure 28. ADS5296 Plug-in GUI Setup (a)

3. Click on the tab *ADS5296 GUI* to view the software GUI for the ADS5296A. The GUI consists of two tabs: *Read Me First* and *High Level Test* as shown in Figure 29.

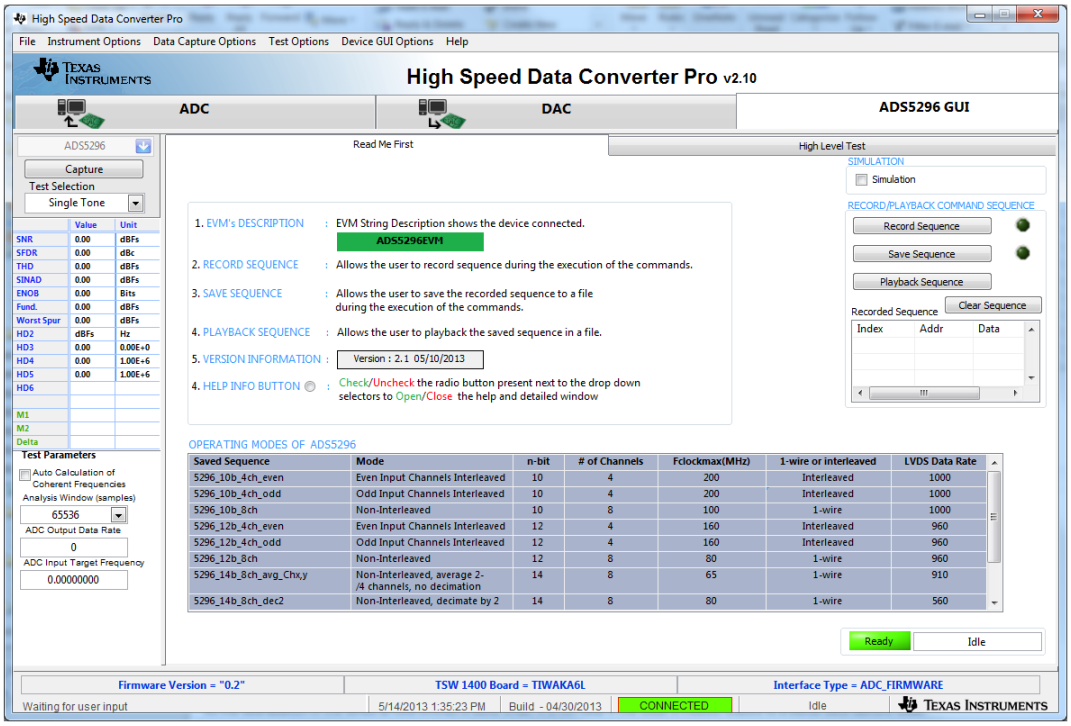

Figure 29. ADS5296 Plug-in GUI Setup (b)

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Clicking on the *High Level Test* tab shows four sub-tabs: *Top Level*, *Test Pattern*, *Digital Signal Processing*, and *Channel Filter* as shown in Figure 30.

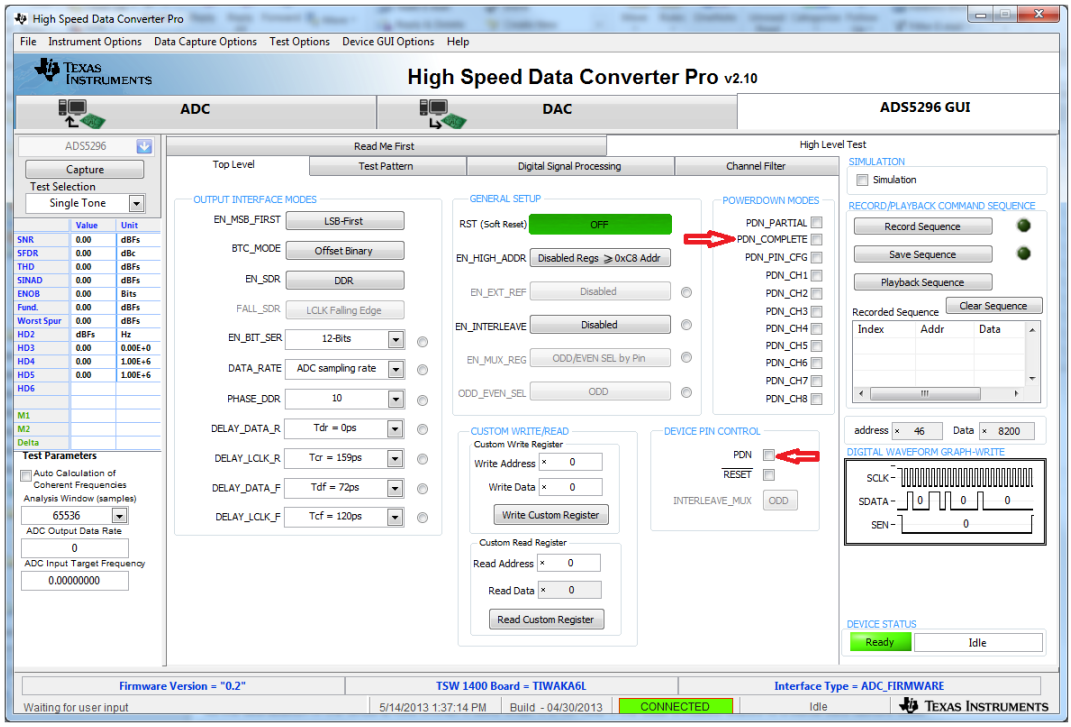

Figure 30. ADS5296 Plug-in GUI Setup (c)

4. Verify that communication between the ADS5296A EVM and the ADS5296 GUI is established by toggling either **PDN_COMPLETE** checkbox or the **PDN** checkbox highlighted on Figure 30. Checking either box should make +5-V power supply current drop from ~850 mA to ~563 mA. If the DC current is approximately 600 mA with both power down boxes unchecked, it indicates that the ADS5296A is not receiving the sampling clock. Please ensure that the 3-pin headers are configured as described in Section 3.2. Before continuing, ensure that both power down boxes are left unchecked. At this point, the GUI is confirmed to be communicating correctly with the EVM and testing can begin.

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4.2 Capturing a RAMP Test Pattern

As described in Section 3.1, the LVDS interface between the ADS5296A EVM and the TSW1400 EVM can be tested using the default EVM configuration and minimal bench equipment.

1. Press on the sub-tab labeled *Test Pattern* and select **RAMP PATTERN** within the **TEST_PATT** menu as shown in Figure 31.

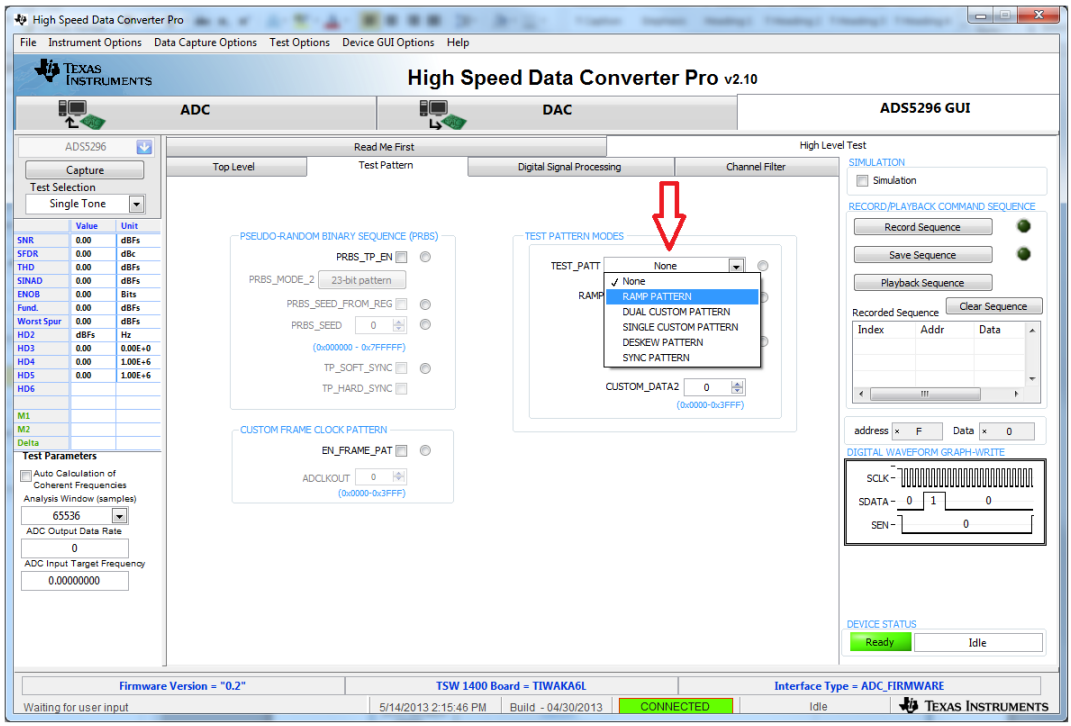

Figure 31. ADS5296 GUI Setup for RAMP Test

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2. Perform the following steps highlighted in Figure 32:
   (a) Press the *ADC* tab in *HSDCpro*
   (b) Change the plot type from *Real FFT* to *Codes*
   (c) Enter *80M* in the field labeled *ADC Output Data Rate*
   (d) Press the *Capture* button

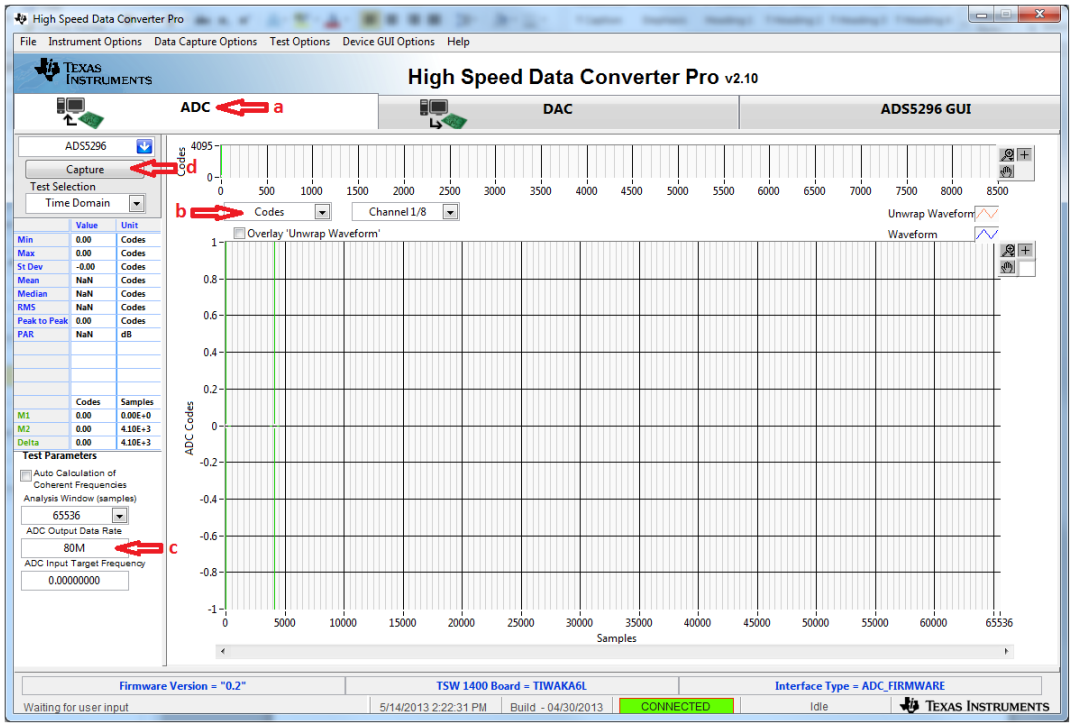

Figure 32. HSDCpro GUI Setup for RAMP Test

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3. The saw tooth waveform should be captured and displayed as in Figure 33.

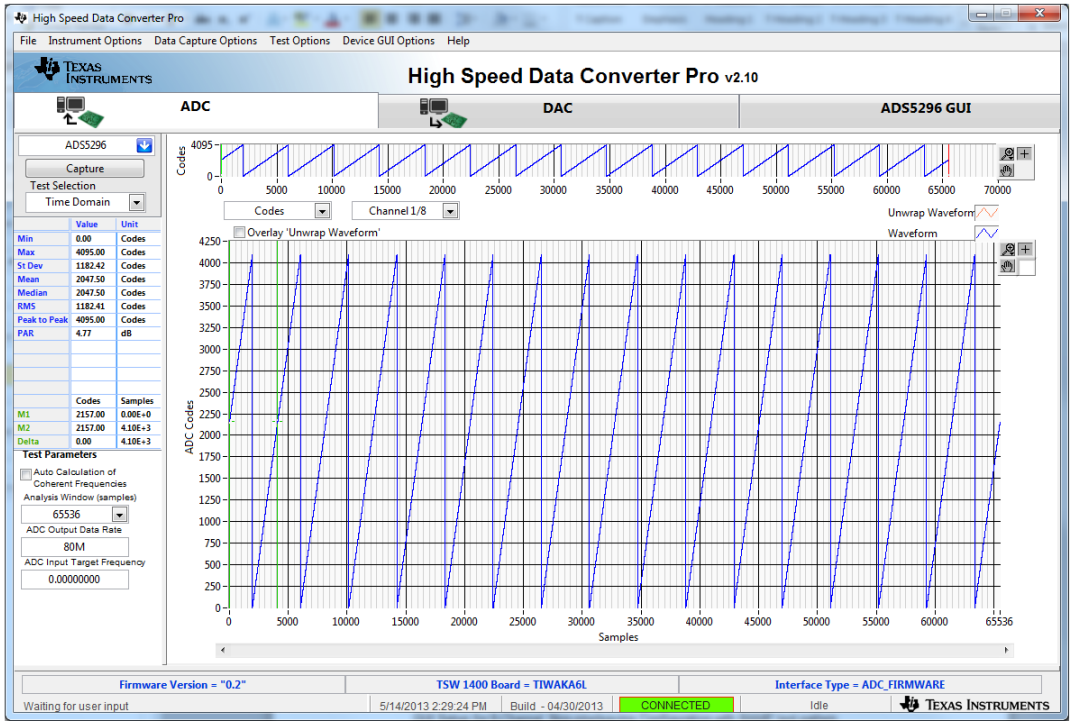

Figure 33. RAMP Capture

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4. By default, *Channel 1/8* is the first channel displayed. Use the drop-down menu shown in Figure 34 to view all 8 channels and confirm that a saw tooth waveform has been captured. Also confirm, in the menu to the left side, that the min code is 0 and the max code is 4095, corresponding to a 12-bit ADC.

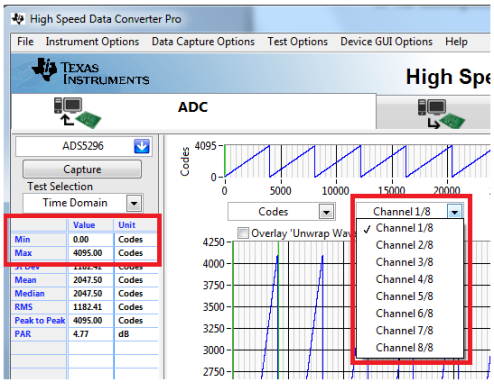

Figure 34. RAMP Capture by Channel

5. Zooming into the waveform, as shown in Figure 35, is recommended to ensure that the RAMP waveform increments 1 ADC code for each subsequent sample.

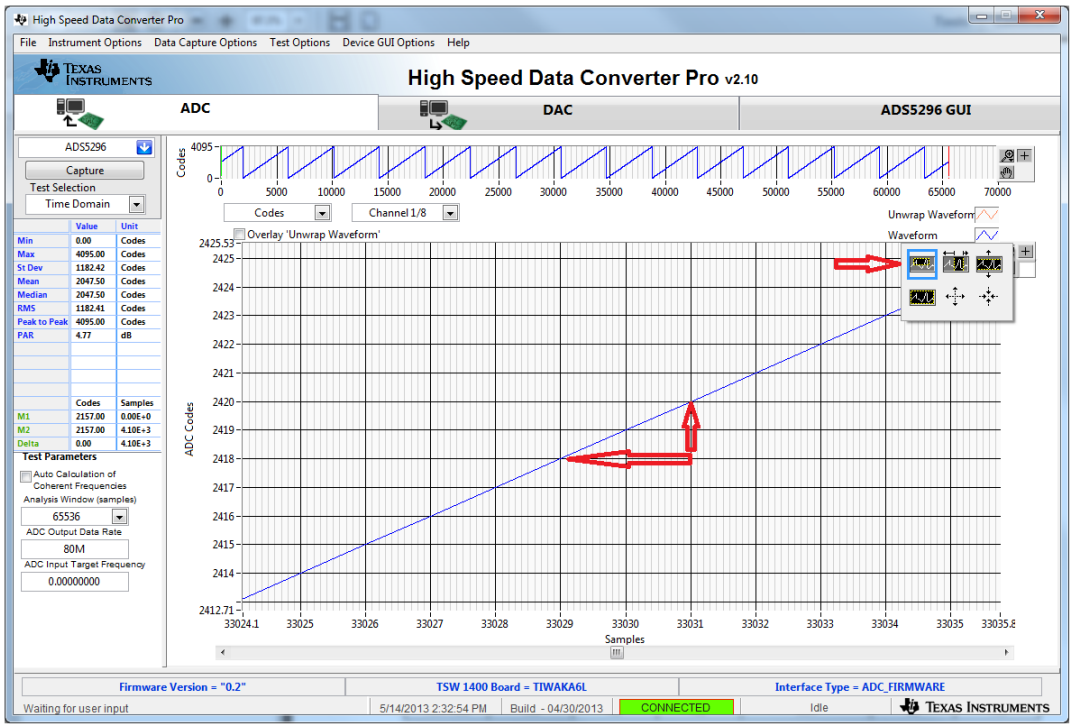

Figure 35. Zoom on RAMP Capture

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4.3 Capturing Sinusoidal Input in Octal Non-Interleaving Mode

This section describes the necessary steps to reconfigure the EVM and test setup for capturing a sinusoidal input with the ADS5296A in octal non-interleaving mode.

1. The RAMP test described in Section 4.2 was performed using an 80-MHz on-board crystal oscillator (XTAL) for the sampling clock. This clock cannot be used to measure performance of the device as it is not phase locked to the input signal. The XTAL should be disabled by moving jumper **J35** from the position labeled **CDC_3.3V** to the position labeled **GND** in the silkscreen. Also, **J38** must change position from **XTAL** to **CLK_XFMR** in the silkscreen to enable the SMA **J31 CLK_XFMR**. Figure 36 and Figure 37 show the jumper positions before and after this change, respectively.

Figure 36. Jumper J35 and J38 positions for Enabled XTAL (default)

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Figure 37. Jumper J35 and J38 positions for Disabled XTAL

2. With the setup established in Figure 37 and Figure 38, perform the following steps:
   (a) Enable the signal generator providing the sampling clock to SMA **J31** labeled **CLK_XFMR** (+5 dBm, 80 MHz)
   (b) Enable the signal generator providing the input signal to SMA **J15** labeled **CH5_XFMR** (+15 dbm, 10 MHz). For high-performance results the instrument should have low phase noise and low harmonic distortion. In addition, a filter is recommended on the input as shown in Figure 38.
   (c) The two signal generators in items (a) and (b) above should be phase locked so that coherency is established. This is achieved connecting the two via a BNC cable. One instrument will provide 10-MHz output while the other instrument will receive 10-MHz input.

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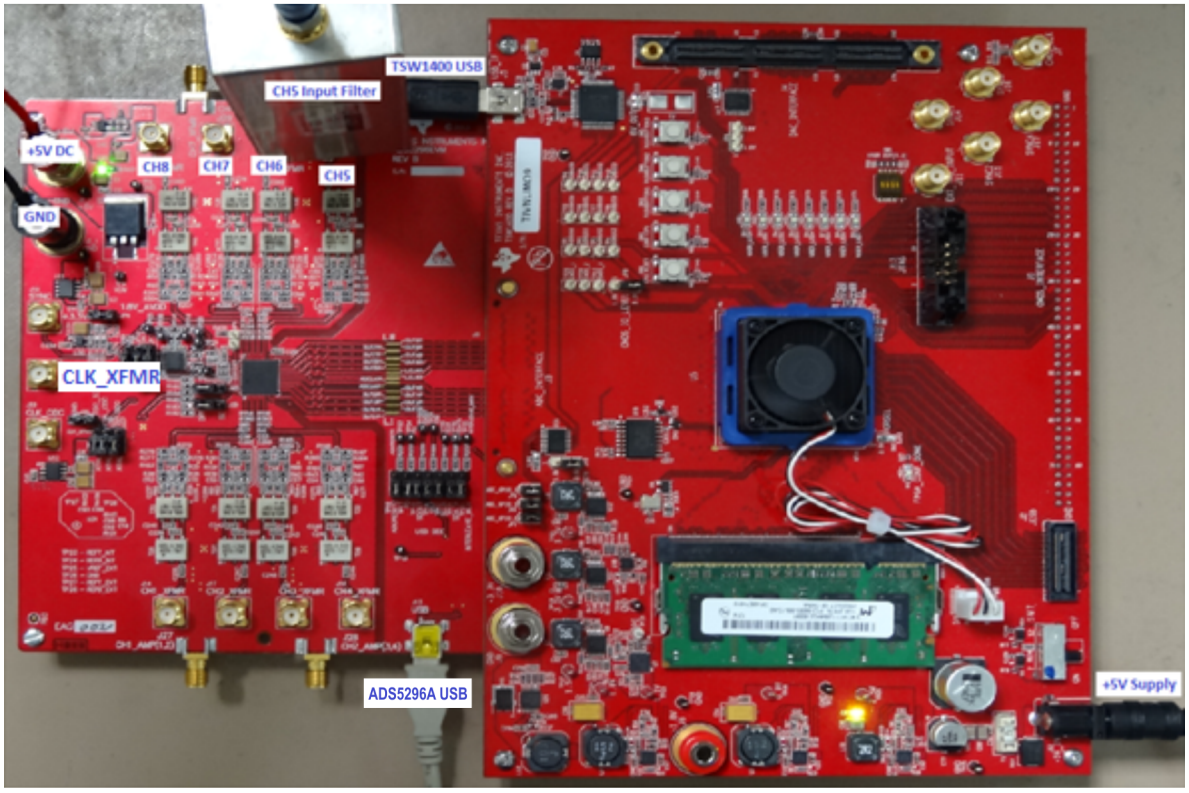

Figure 38. Octal Non-interleaving Mode Hardware Setup

3. Click on *ADS5296 GUI* tab and ensure that the **TEST_PATT** field is set to **None**, as shown in Figure 39.

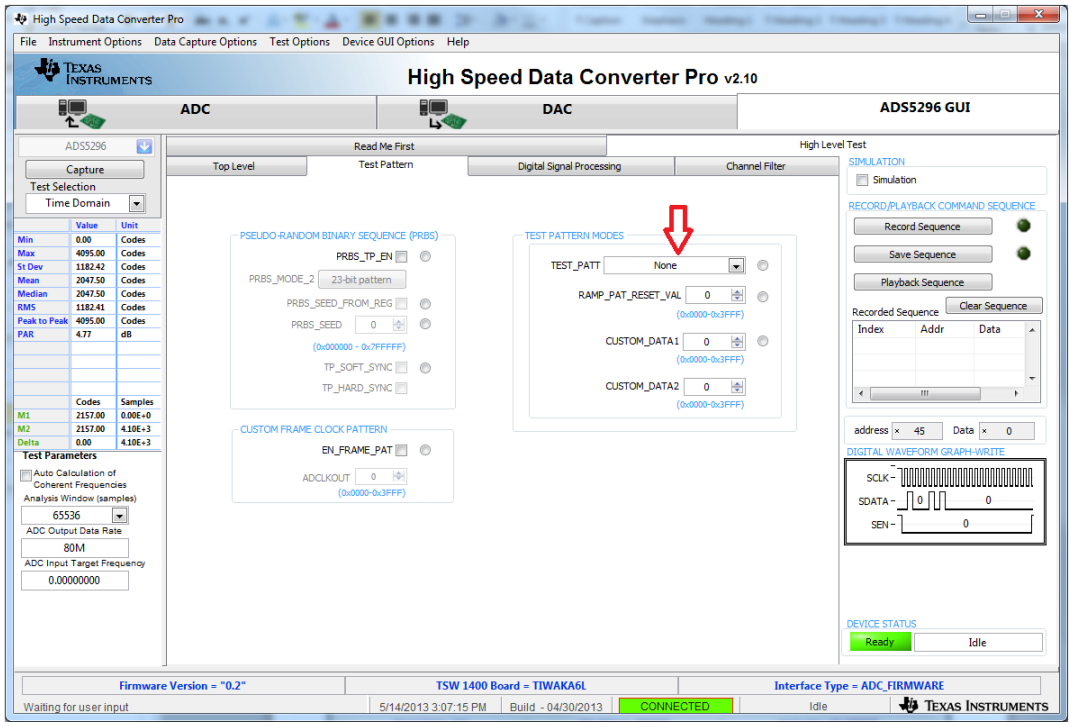

Figure 39. ADS5296 GUI Setup for Octal Non-Interleaving Mode

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4. Click on the *ADC* tab and perform the following steps as illustrated in Figure 40.
   (a) In the box labeled *ADC Input Target Frequency* input **10M**
   (b) In the drop down menus set *Real FFT*, *Channel 5/8*, *Rectangular*
   (c) Check the box labeled *Auto Calculation of Coherent Frequencies* (Note: the *ADC Input Target Frequency* box will automatically be updated with the required coherent frequency)
   (d) Change the frequency on the signal generator providing the analog input signal to match the value shown in the *ADC Input Target Frequency* box (**9.99877930 MHz**)
   (e) Press the *Capture* button

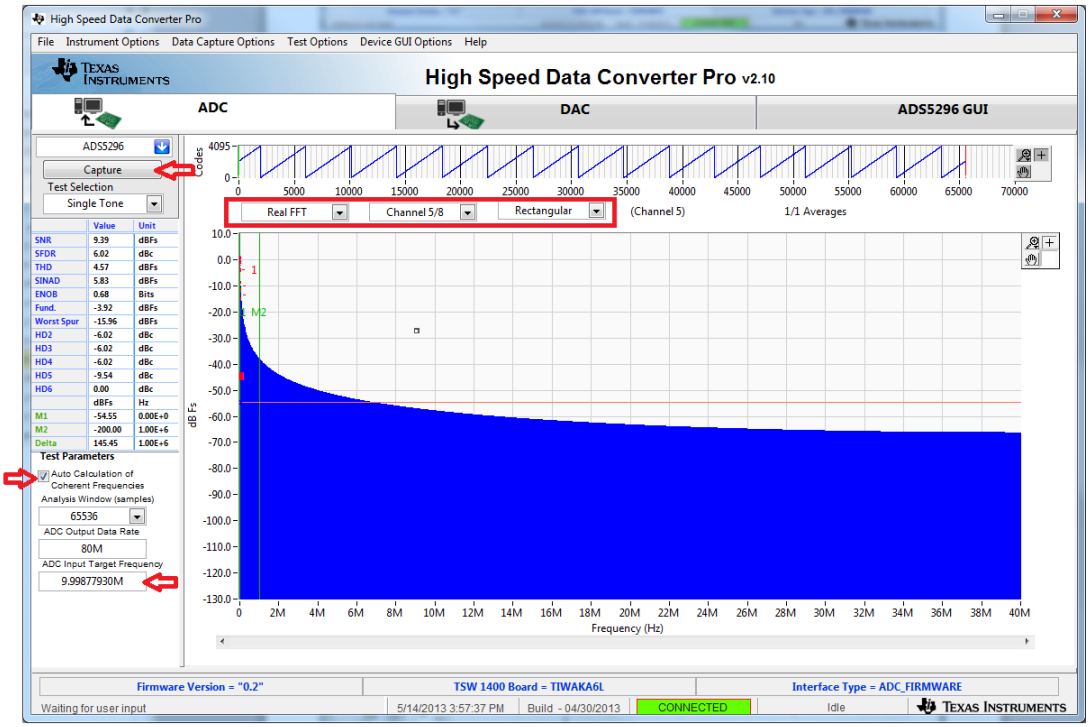

Figure 40. HSDCpro GUI Setup for Octal Non-Interleaving Mode (b)

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5. The plot will update as shown in Figure 41. Take note of the *Fund.* value in the left panel highlighted in RED in Figure 41. This value is dependent on the signal level set on the signal generator feeding the input signal to **J15**. It also depends on cable loss and filter insertion loss which can vary among parts. If needed, reset the signal amplitude (level) until the *Fund.* value is approximately –1.0 dBFs, as this is the condition for which the datasheet specifications are set. In the example shown here, the input level should be changed from 15.0 dBm to 15.1 dBm and then a capture retaken.

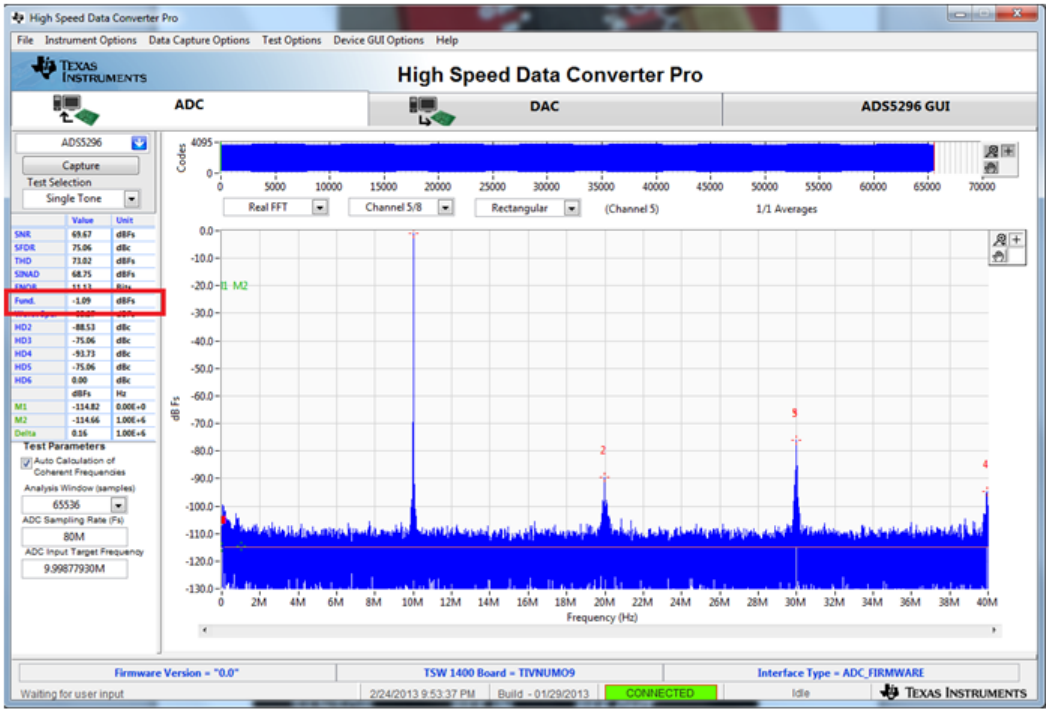

Figure 41. Octal Non-Interleaving Mode Capture 1

6. After re-capturing, the *Fund.* value is now closer to –1.0 dBFs as shown in Figure 42.

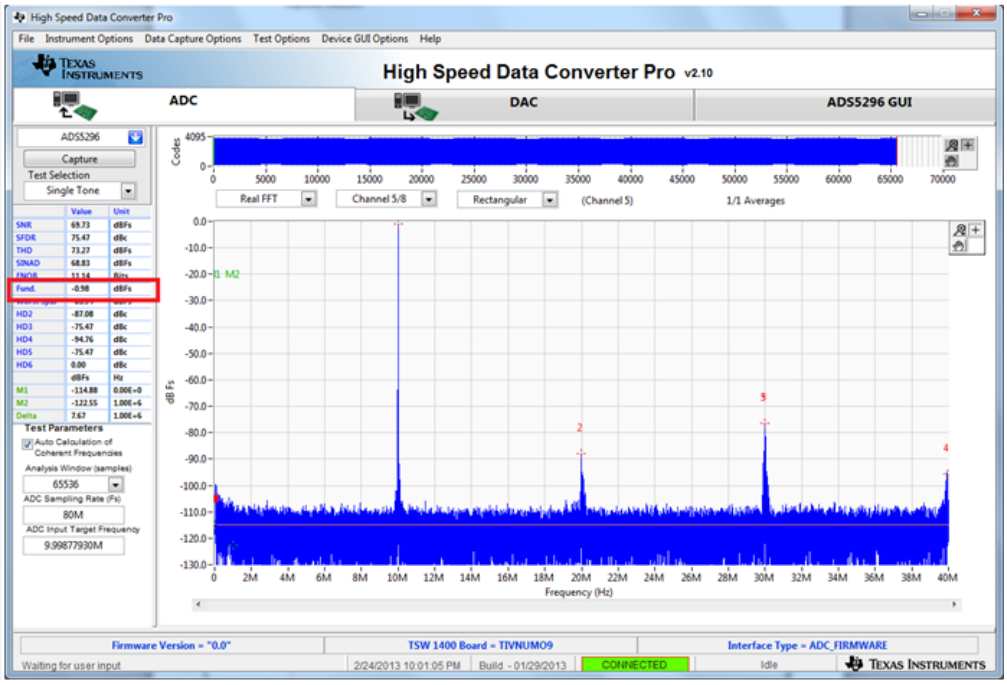

Figure 42. Octal Non-Interleaving Mode Capture 2

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The SNR computed is highly dependent on the phase noise of the input signal source. Figure 42 and Figure 43 are with the exact same configuration, the only difference being the instrument used to provide the 10-MHz input signal. A 4.5 dB difference in the computed SNR is observed and is attributed solely to the integrity of the input signal, specifically the close-in phase noise.

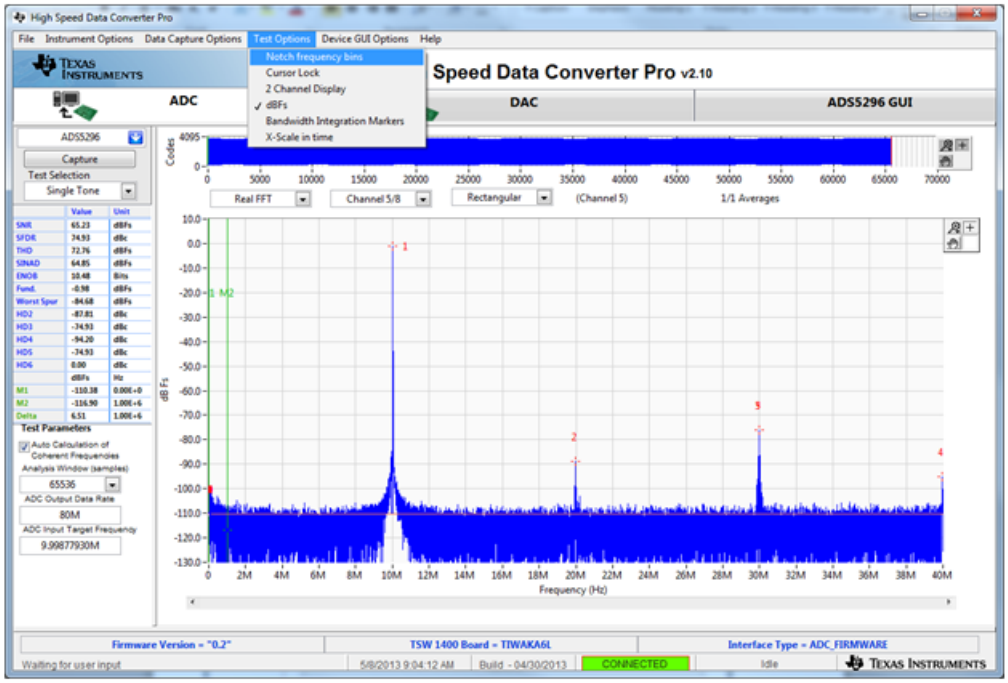

Figure 43. Octal Non-Interleaving Mode Capture 3

A software filter can be used to remove the contribution of phase noise using the *HSDCpro* menu *Test Options => Frequency Bins* as shown in Figure 44.

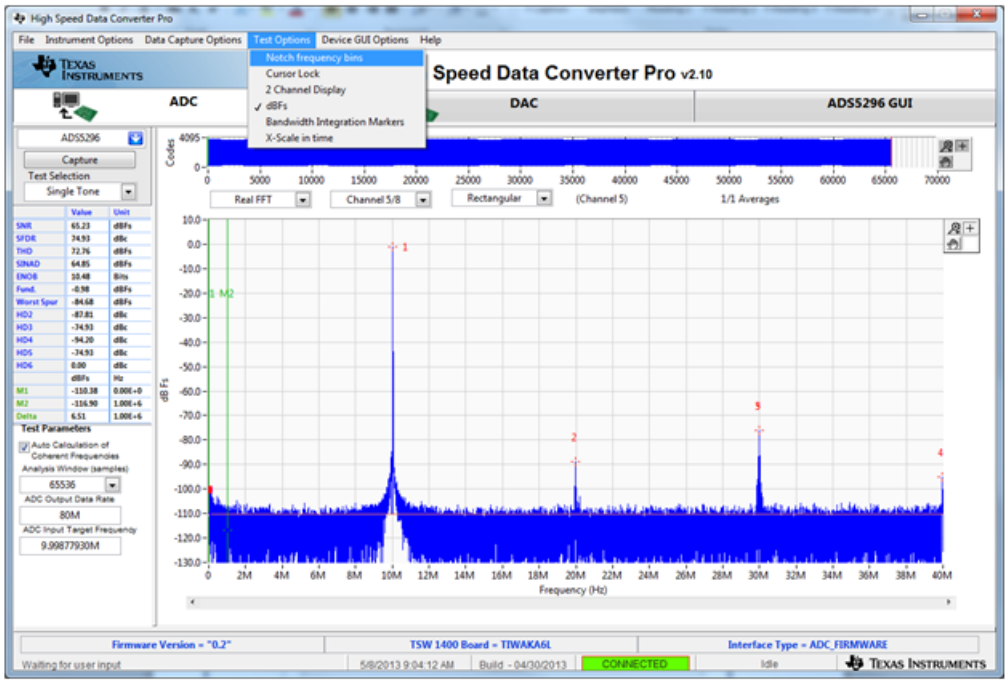

Figure 44. HSDCpro Software Filtering

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Change the default values from 0 to 500 as shown in Figure 45.

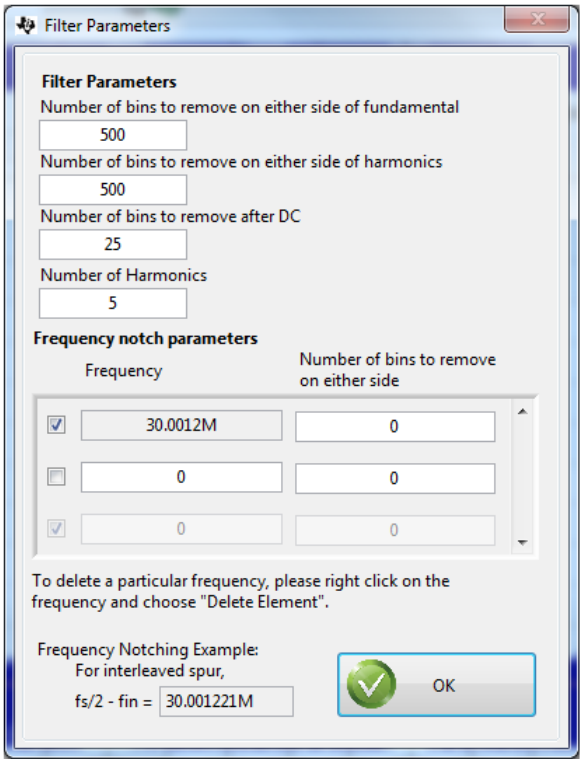

Figure 45. HSDCpro Software Filtering Menu

The plot and all calculations will be updated accounting for these removed bins as shown in Figure 46. The SNR is now very close to the Software Filtering Menu SNR shown in Figure 43 using a superior instrument.

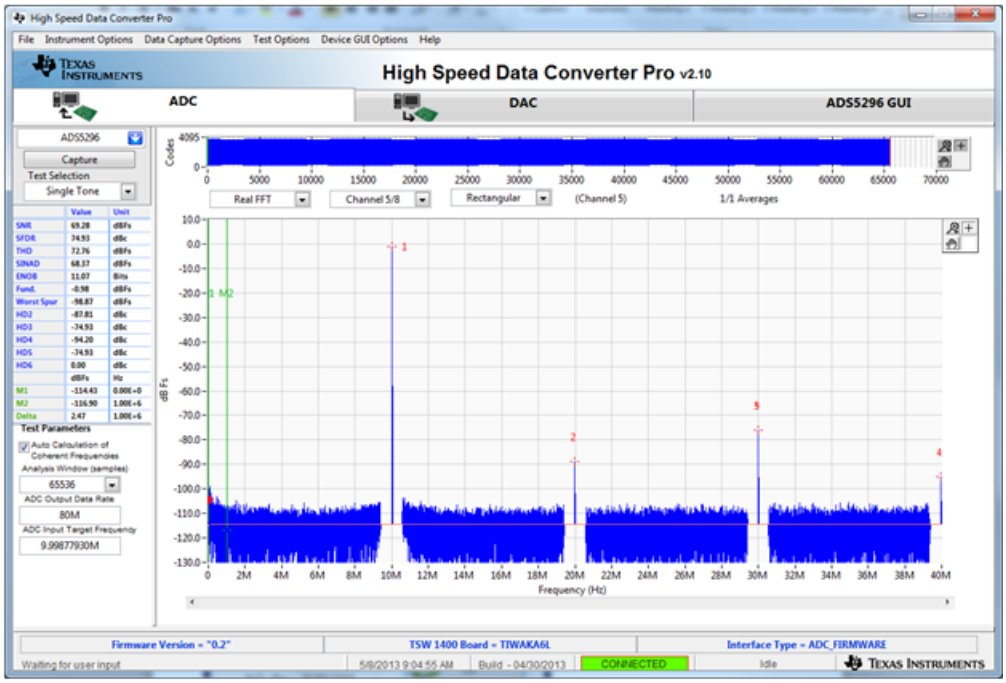

Figure 46. HSDCpro Capture with Software Filtering

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4.4 Capturing Sinusoidal Input in Quad Interleaving Mode

This section describes the necessary steps to reconfigure the EVM and test setup for capturing a sinusoidal input with the ADS5296A in quad interleaving mode.

1. Setup the EVM as shown in Figure 47 by performing the following steps:
   (a) The signal generator providing the sampling clock to SMA **J31** labeled **CLK_XFMR** should be changed from 80 MHz to 200 MHz. (+5 dBm, 200 MHz)
   (b) Provide the input signal to SMA **J27** labeled **CH1_AMP(1,2)** (+15.1 dbm, 10 MHz). For high-performance results the instrument should have low phase noise and low harmonic distortion. In addition, a filter is recommended on the input as shown in Figure 47.
   (c) The two signal generators in items (a) and (b) above should be phase locked. This is achieved connecting the two via a BNC cable. One instrument will provide 10-MHz output while the other instrument will receive 10-MHz input.

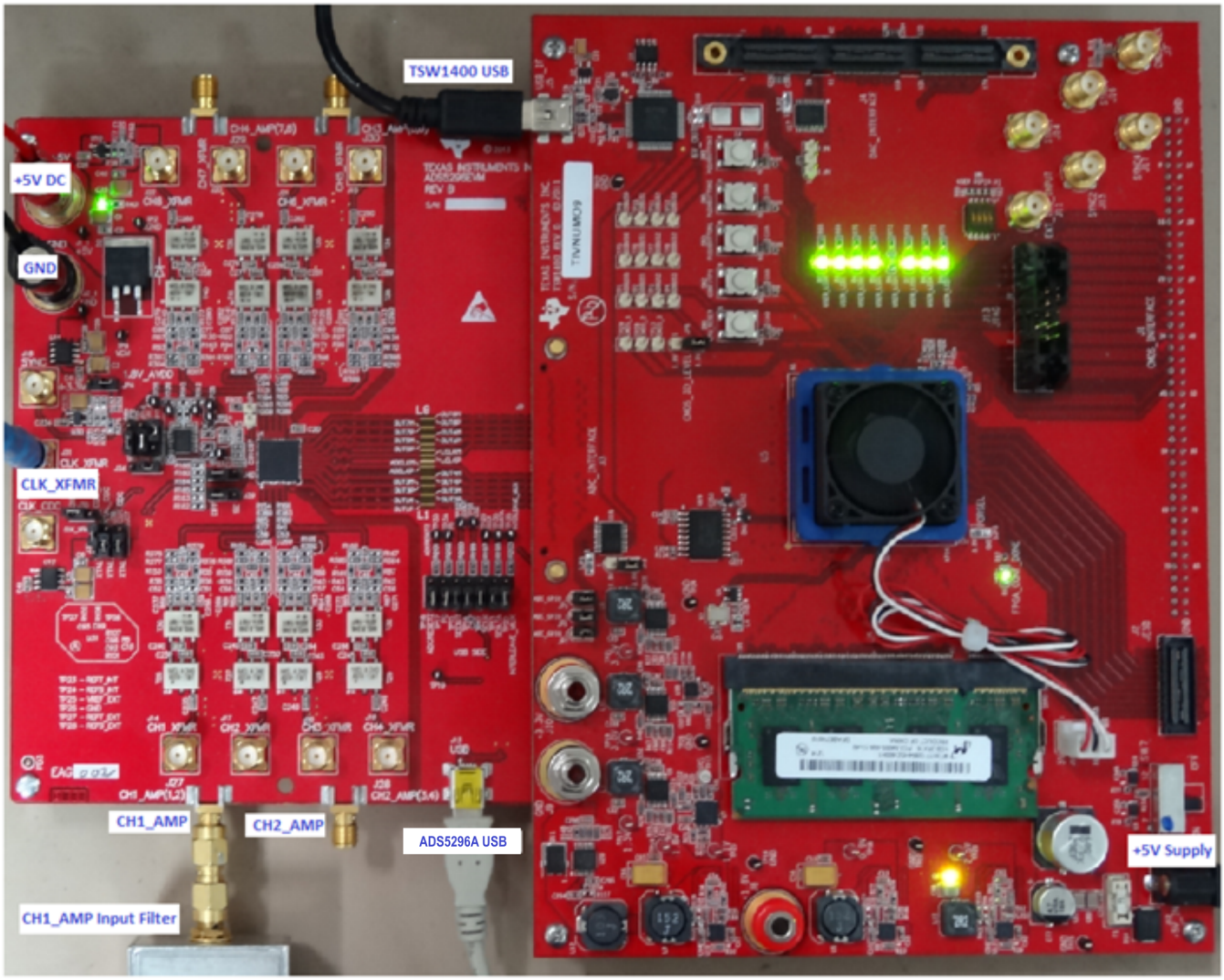

Figure 47. Quad-Interleaving Mode Hardware Setup

2. From the *ADS5296 GUI*, *Top Level* tab, make the following changes as shown in Figure 48. With this configuration the ADS5296A will be sampling channel 1 since the **ODD_EVEN_SEL** is set to **ODD** in the software GUI.
   (a) Change **EN_BIT_SER** to **10-bits**
   (b) Change **EN_INTERLEAVE** to **Enabled**

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(c) Change *ADC Output Data Rate* to **200M**

(d) Reset the signal generator providing the analog input signal to the new coherent frequency shown in the *ADC Input Target Frequency* box (9.98229980 MHz)

(e) Return to *ADC* tab and hit **Capture**.

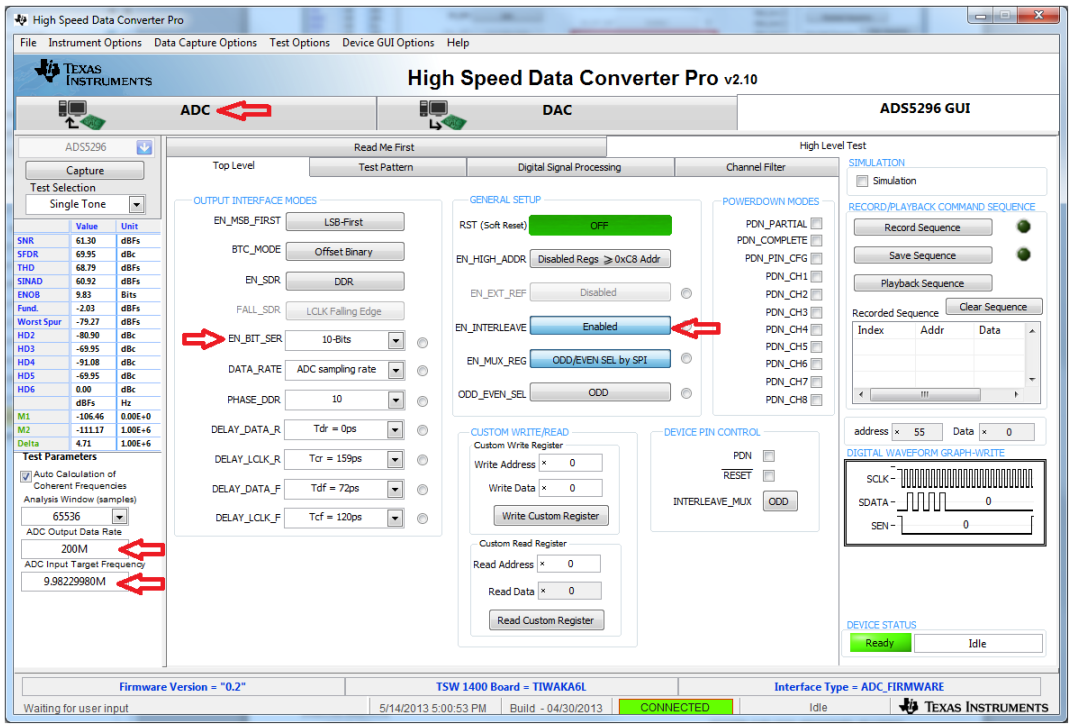

Figure 48. Quad-Interleaving Mode GUI Setup

Figure 49 shows that the *Fund.* value is ~0.8 dB low.

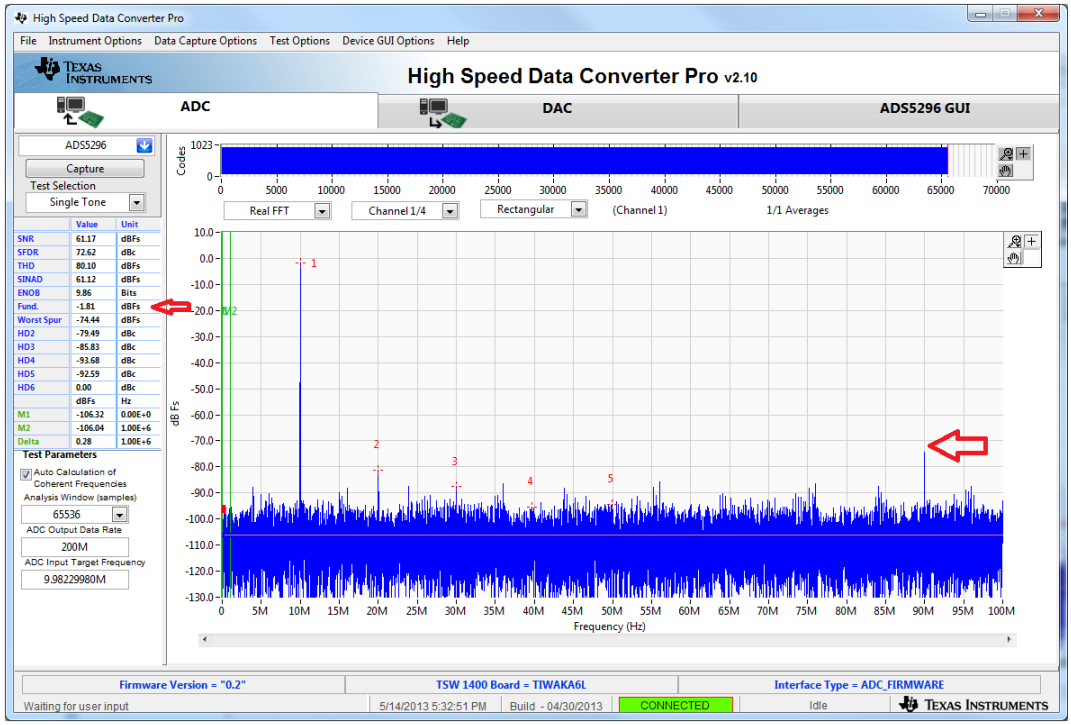

Figure 49. Quad-Interleaving Mode Capture 1

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Increasing the output power from the signal generator by +0.8 dB and re-capturing results in Figure 50.

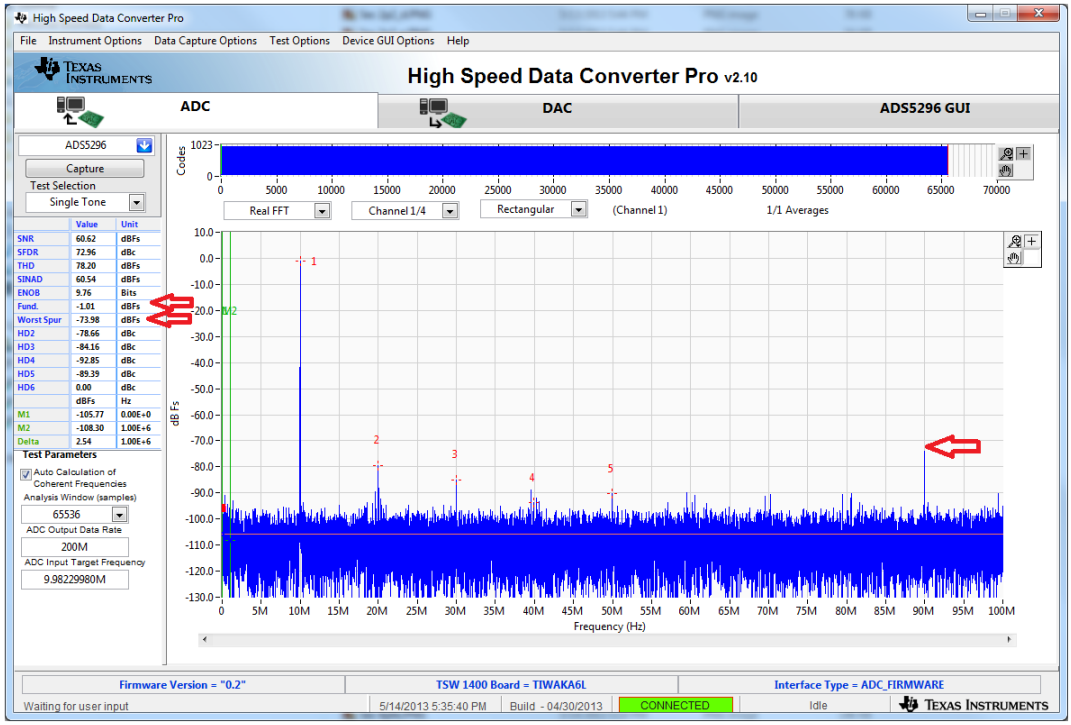

Figure 50. Quad-Interleaving Mode Capture 2

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For an interleaving ADC, there exists a spur at *Fs/2-Fin*, which is commonly referred to as the interleaving spur. As seen in the previous capture, this spur is the *Worst Spur* in the Nyquist band. The *HSDCpro GUI* auto-calculates the location of this spur in the menu *Test Options → Notch Frequency Bins* and allows for removal this bin from the plot if desired as shown in Figure 51.

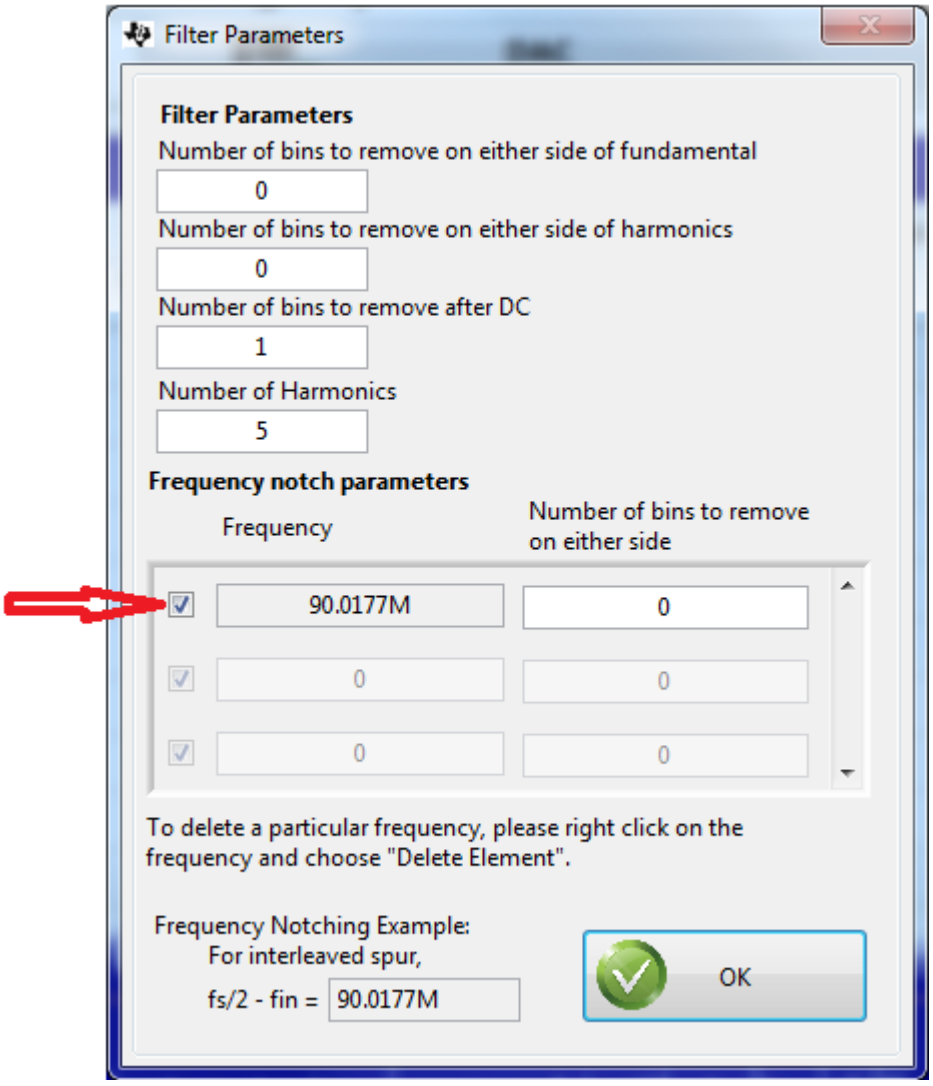

Figure 51. Quad-Interleaving Mode Fs/2 - Fin Software Filtering

5 ADS5296 GUI in Detail

This section is dedicated to explaining the ADS5296 GUI, and all its features, in depth. There is a section dedicated to each tab of the ADS5296 software GUI: *Read Me First*, *Top Level*, *Test Pattern*, *Digital Signal Processing*, and *Channel Filter*.

After launching *HSDCpro*, the ADS5296 GUI can be invoked in two ways: normal mode or simulation mode. Simulation mode is used in the event that no ADS5296A EVM is available. When this is the case, the message shown in Figure 52 appears shortly after choosing the ADS5296A device in *HSDCpro*.

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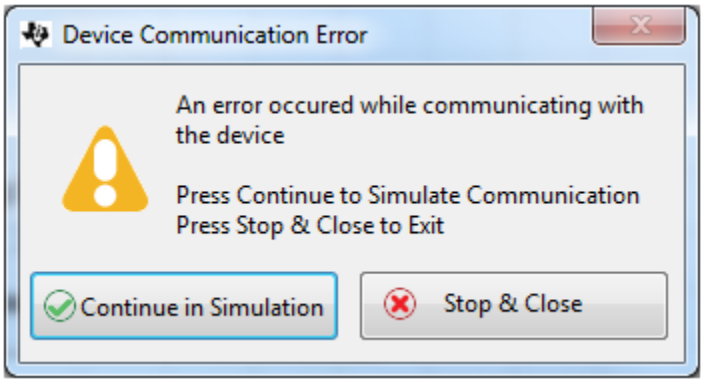

Figure 52. ADS5296 GUI Simulation Mode

The user is given the choice to *Continue in Simulation* or *Stop & Close*. If *Continue in Simulation* is selected the ADS5296 GUI will install and all controls will "*appear*" to function as normal including the *DIGITAL WAVEFORM GRAPH-WRITE* which shows what is being written to the serial interface. When in *Simulation* mode the checkbox at the top right corner of the GUI will remain checked as shown in Figure 53.

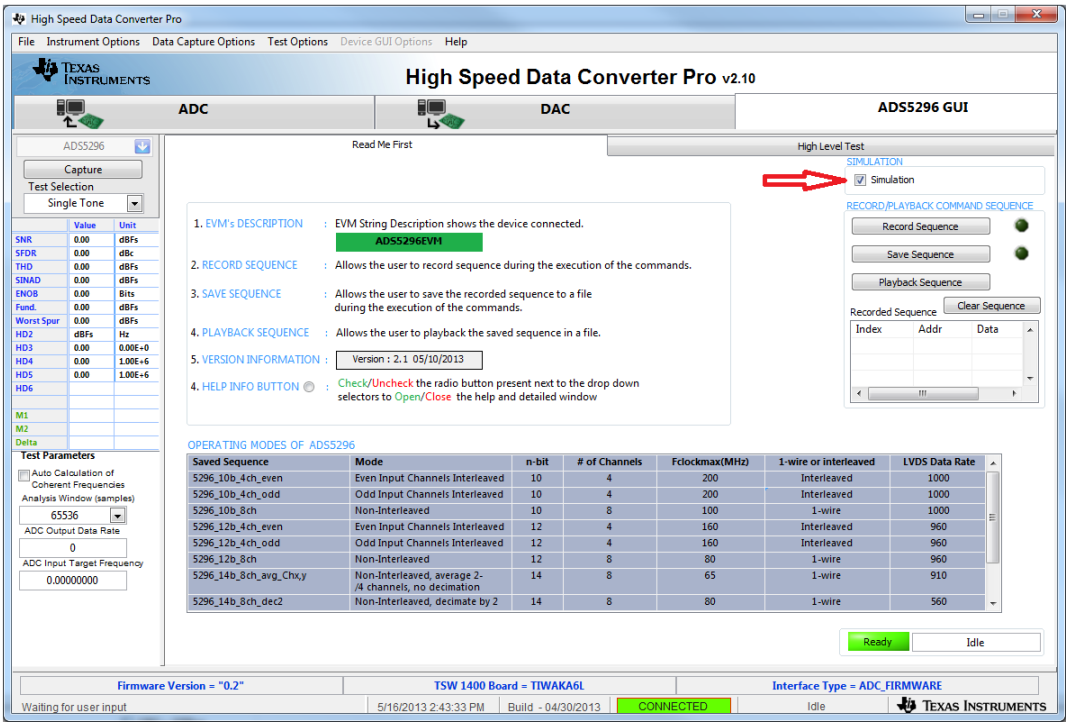

Figure 53. ADS5296 GUI Simulation Mode Checkbox Indicator

As Figure 53 shows, within the ADS5296 GUI tab there are two high level tabs called *Read Me First* and *High Level Test*. The *Read Me First* tab contains general information while the *High Level Test* tab holds four sub-tabs containing all SPI controls.

5.1 Read Me First Tab

After launching *HSDCpro* and selecting the ADS5296 firmware to load, as depicted in Figure 22 through Figure 27, the ADS5296 GUI presents the *Read Me First* tab initially as shown in Figure 53 (*Simulation* checkbox will be unchecked if EVM is connected).

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The two sections in the upper right corner of this tab, *SIMULATION* and *RECORD/PLAYBACK COMMAND SEQUENCE*, are common to all tabs within the ADS5296 GUI. The *RECORD/PLAYBACK COMMAND SEQUENCE* section allows the user to:

- Record a sequence of commands
- Save the sequence that was recorded to a file
- Playback a sequence that was saved from a file

Once the *Record Sequence* button is pressed, the sequence of commands, or SPI writes, will appear chronologically in the Recorded Sequence box at the bottom of this section as depicted in Figure 54.

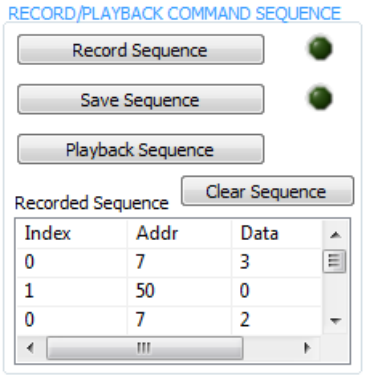

Figure 54. RECORD/PLAYBACK COMMAND SEQUENCE (a)

Hitting the *Save Sequence* button brings up dialog box to save the sequence to the GUI install path:

`C:\Program Files (x86)\Texas Instruments\ADS5295_96\Recorded Sequences\ADS5296 Recorded Sequences`

To playback a saved sequence, hit the *Playback Sequence* button and choose the sequence to execute. As shown in Figure 55, there are nine sequences pre-defined in this folder corresponding to the nine *OPERATING MODES OF ADS5296* shown in the table at the bottom of the tab. The table includes the maximum sampling clock speed supported for each mode. Ensure that the clock source is within this limit for a particular mode.

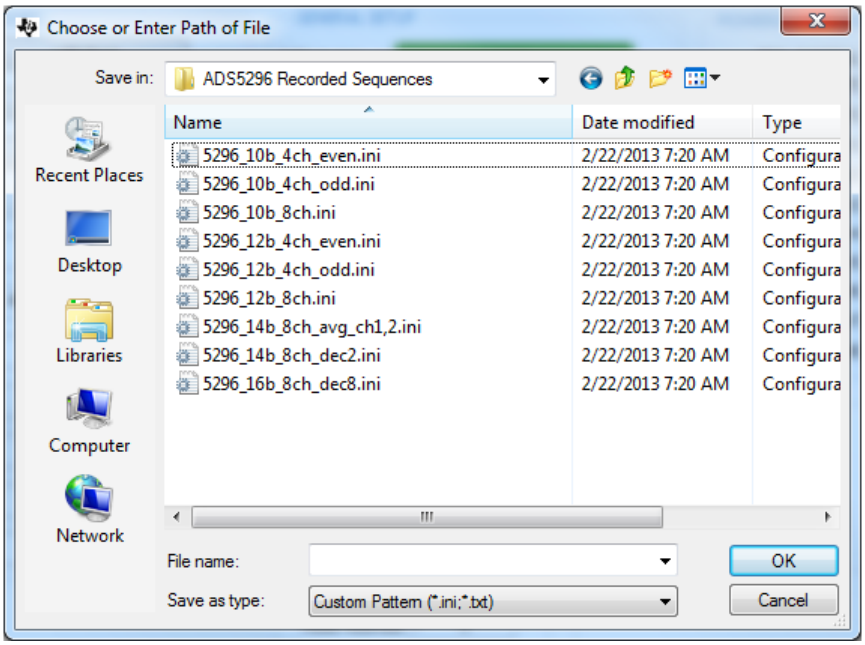

Figure 55. RECORD/PLAYBACK COMMAND SEQUENCE (b)

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5.2 Top Level Tab

The left-most sub-tab within the *High Level Test* tab is *Top Level*. As shown in Figure 56, this tab contains five sections which are highlighted in red: *OUTPUT INTERFACE MODES*, *GENERAL SETUP*, *POWERDOWN MODES*, *CUSTOM WRITE/READ* and *DEVICE PIN CONTROL*. In the right border of this tab is a section called *DIGITAL WAVEFORM GRAPH-WRITE*.

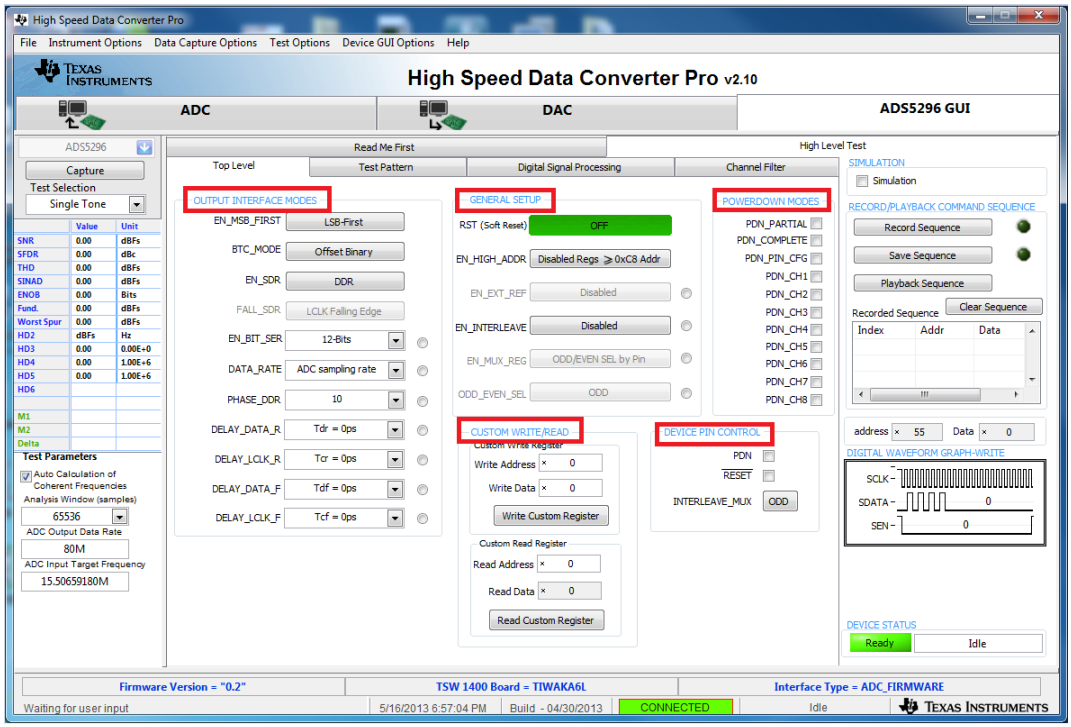

Figure 56. RECORD/PLAYBACK COMMAND SEQUENCE (c)

This section, like *Simulation* and *RECORD/PLAYBACK COMMAND SEQUENCE* above it, remains fixed in the border when switching among the sub-tabs within the *High Level Test* tab. The *DIGITAL WAVEFORM GRAPH-WRITE* section, shown in Figure 57, tracks all SPI writes from the GUI and displays them here.

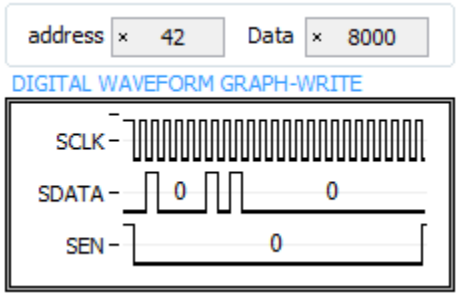

Figure 57. DIGITAL WAVEFORM GRAPH-WRITE

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The *OUTPUT INTERFACE MODES* section contains all device controls related to the format of the data to be output across the LVDS interface. Figure 58 shows the drop-down menu for **EN_SER_BIT** which selects the resolution of he ADC. The button to the right of this menu, and seen throughout the GUI, is an info button and displays relevant information from the datasheet.

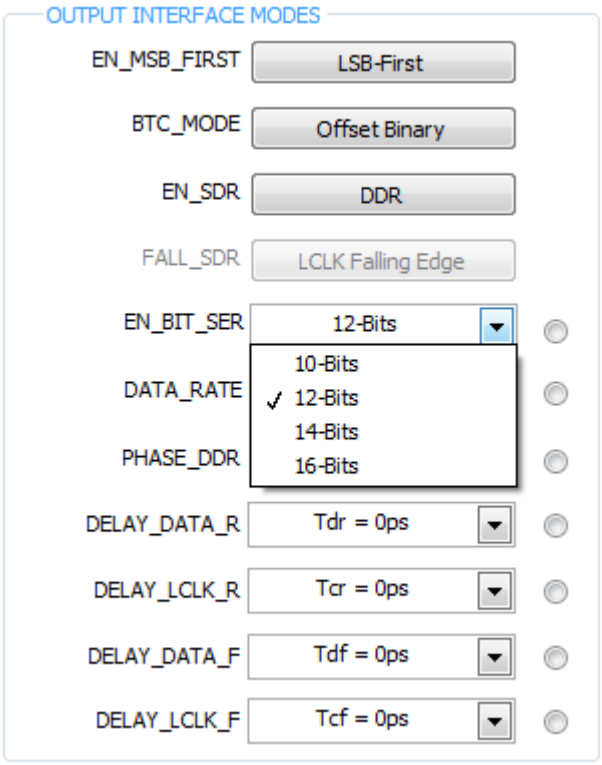

Figure 58. EN_SER_BIT Drop-Down Menu

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When the info button next the **EN_SER_BIT** control is selected with **12-bits** selected the information shown in Figure 59 is presented.

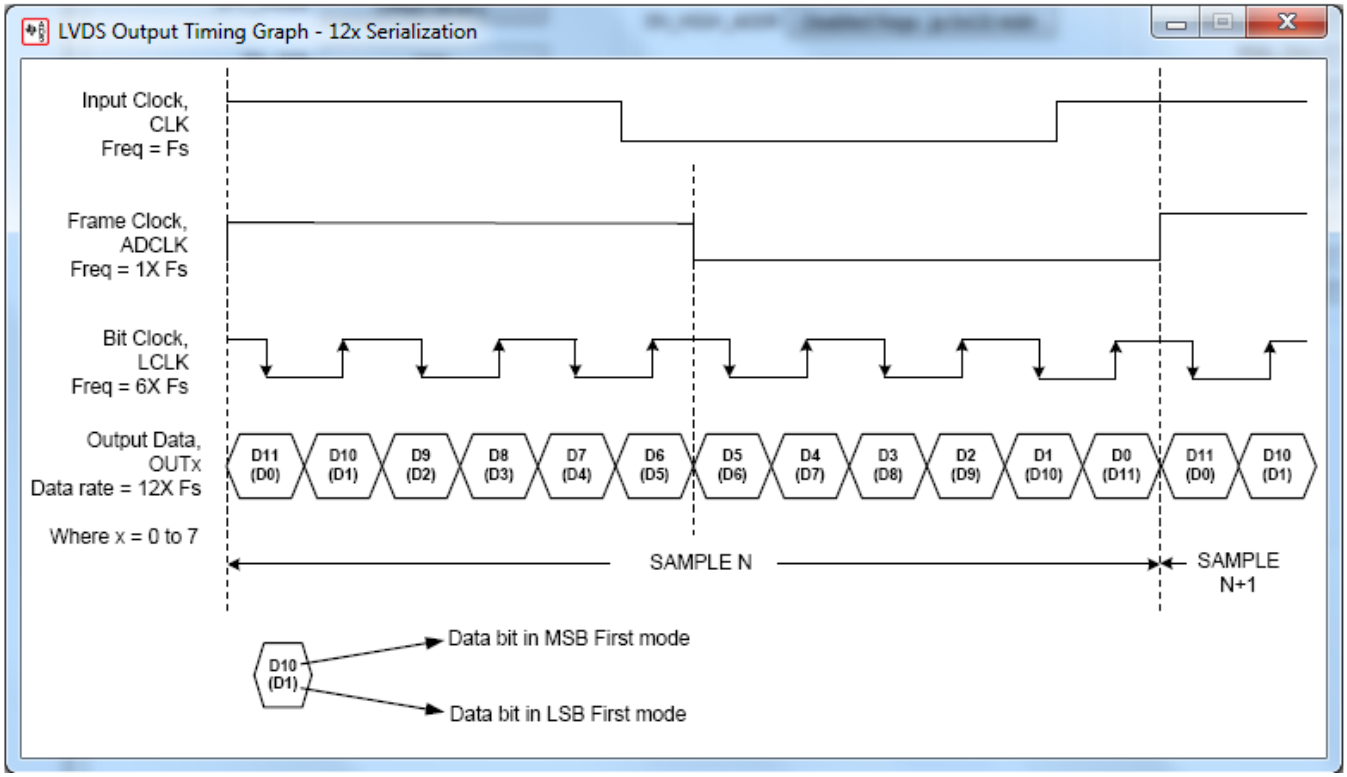

Figure 59. EN_SER_BIT Info Button

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The *GENERAL SETUP* section shown in Figure 60 contains several controls, the top most being the **RST** button, or software reset. When this button is pressed all serial registers are updated to their default state and the bit is reset automatically. The button **EN_HIGH_ADDR** is required to enable the **EN_EXT_REF** button below it. This dependency represents the implementation in the design itself. The ADS5296A device supports both internal and external reference mode to set the full-scale of the ADC. The **EN_INTERLEAVE** button is used to enable and disable the interleaving mode, thus, switching the device between a quad channel ADC and an octal ADC, respectively. When **EN_INTERLEAVE** is enabled, the **EN_MUX_REG** button becomes active (ungreyed) and determines whether the selection to sample odd numbered channels or even numbered channels in interleave mode comes from the SPI or from the **INTERLEAVE_MUX** pin of the device. If *ODD/EVEN SEL* by SPI is selected, the last button of this section, **ODD_EVEN_SEL**, becomes active and determines this. If *ODD/EVEN SEL* by Pin is selected instead, the selection to sample odd numbered channels or even numbered channels in interleave mode comes from the state of the **INTERLEAVE_MUX** button in the *DEVICE PIN CONTROL* section of this tab.

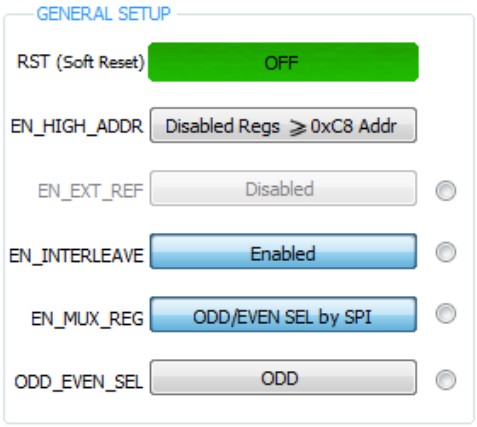

Figure 60. GENERAL SETUP Section of Top Level Tab

The *CUSTOM WRITE/READ* section of the *Top Level* tab allows for custom writing to the serial interface of the ADS5296A as well as reading back register values. When a valid register address and value is provided the corresponding control will automatically update to reflect the current state of the device. In the example in Figure 61, the value of **PHASE_DDR** updated as a result of writing x8000 to reg42.

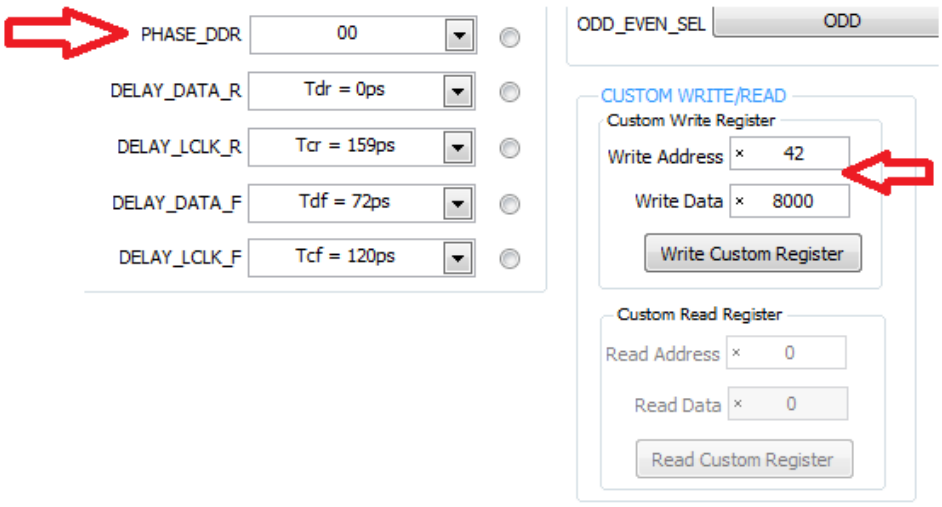

Figure 61. Custom WRITE/READ Example

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5.3 Test Pattern Tab

The second sub-tab, shown in Figure 62, is *Test Pattern*. Within this tab, the user has the control of all the test patterns intrinsic to the device as described in the three sections of this tab: *PSEUDO-RANDOM BINARY SEQUENCE (PRBS)*, *CUSTOM FRAME CLOCK PATTERN*, *TEST PATTERN MODES*.

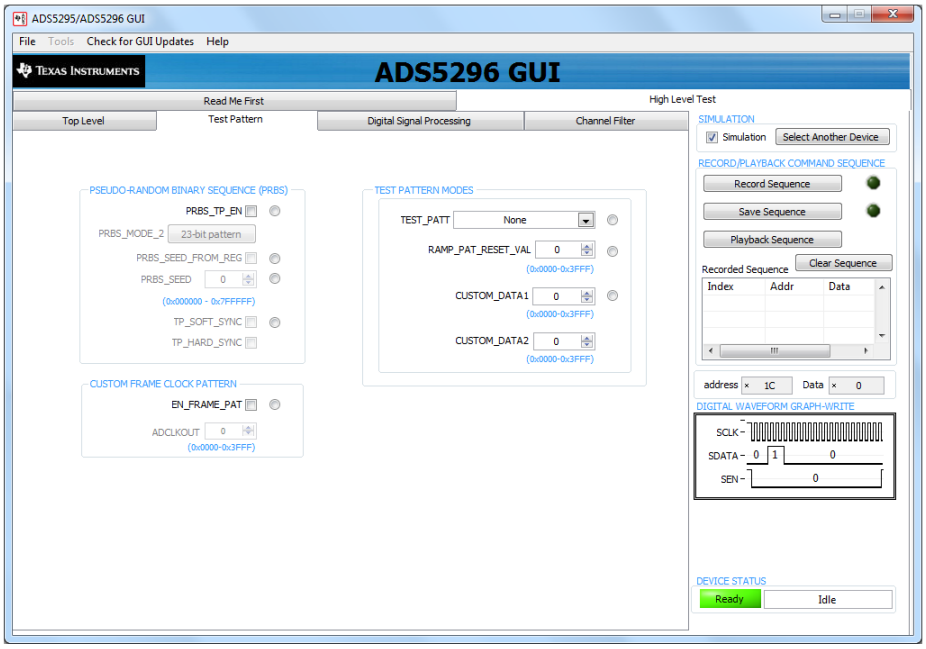

Figure 62. Test Pattern Tab

The *PRBS* section shows all its controls to be greyed an unselectable except for **PRBS_TP_EN** checkbox. Once this box is checked all the remaining controls are accessible as shown in Figure 63. The info buttons provide details on the definition of each control.

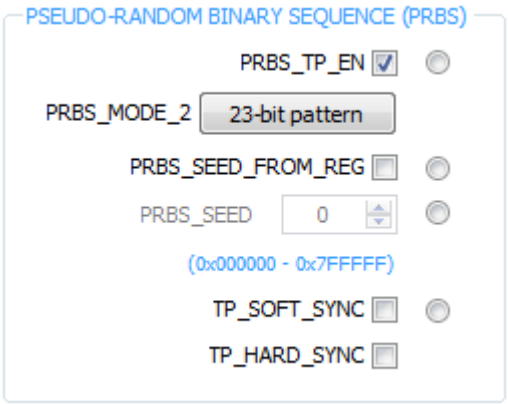

Figure 63. PRBS Section Enabled

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The *TEST PATTERN MODES* section contains commonly used test patterns under the **TEST_PATT** drop-down menu as shown in Figure 64. All of these patterns are generated internal to the ADS5296A device and provided on all channels simultaneously.

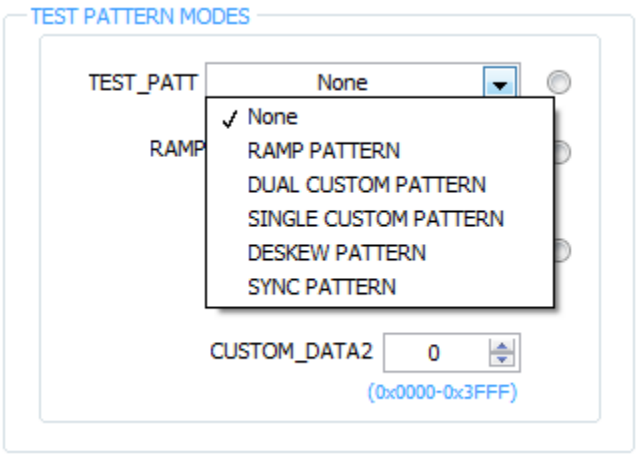

Figure 64. TEST PATTERN MODES Section

5.4 Digital Signal Processing Tab

The *Digital Signal Processing* tab contains five sections as shown in Figure 65: *CHANNEL AVERAGING*, *CHANNEL_GAIN*, *LOW FREQUENCY NOISE SUPPRESSION*, *SWAP ANALOG INPUTS*, and *INPUT/OUTPUT MAPPING*.

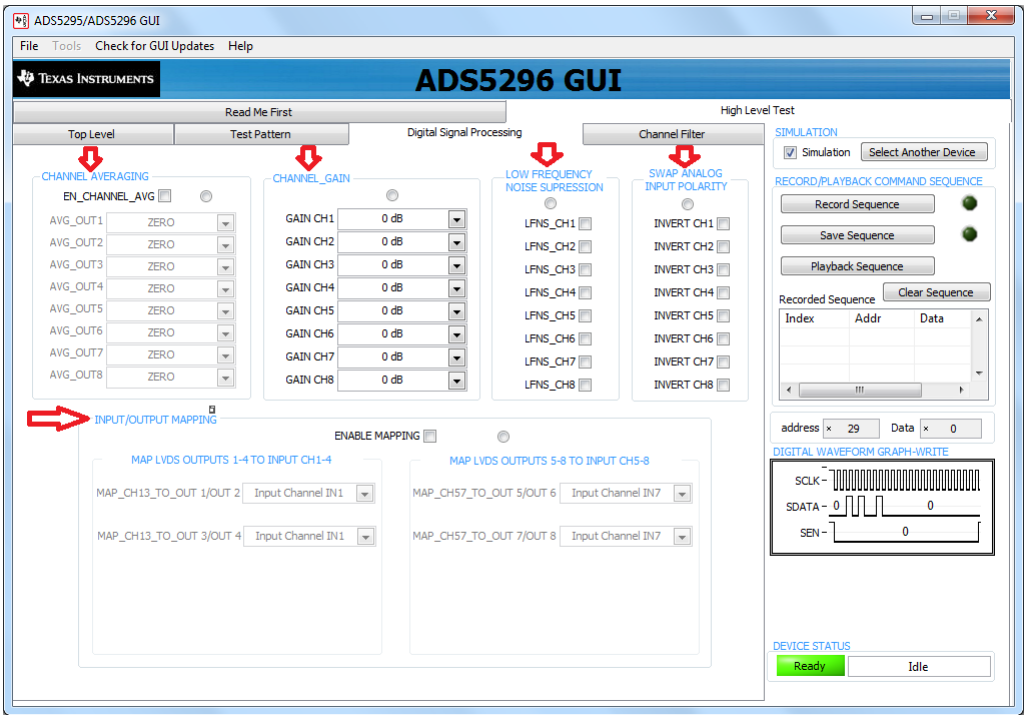

Figure 65. Digital Signal Processing Tab

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The *CHANNEL AVERAGING* function is enabled by the checkbox labeled **EN_CHANNEL_AVG** as shown in Figure 66. Once checked, the drop-down menus within the section become un-greyed and active as shown. The drop-down menu shown in Figure 66 corresponds to the choices available to output onto OUT1 of the device.

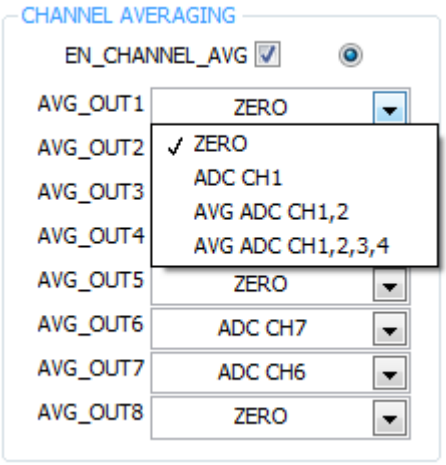

Figure 66. Digital Signal Processing Tab

With Zero selected from the drop-down menu, the output to Channel 1 is fixed at maximum ADC code. With *ADC CH1* selected, the normal Channel 1 output is captured as in the case when channel averaging is disabled. With *AVG ADC CH1,2* selected, the Channel 1 output now contains the averaged output Channel 1 and Channel 2 which improves SNR by approximately 4.6 dB. Finally, with *AVG ADC CH1,2,3,4* selected the output of Channel 1 contains the average of the four channels which improves SNR by 5.4 dB typically. (*Note: pressing the info button in this section shows the graphic in Figure 67. This table, from the datasheet, shows only the averaging options for each output, which is either a two-channel average or a four-channel average. Not shown in the table are the two other options appearing the GUI drop-down menus, ZERO and ADC CHx, which represents the actual design implementation*.)

PRBS Enable Help

Table 12. Using Channel Averaging

AVERAGED CHANNELS	OUTPUT WHERE AVERAGED DATA ARE AVAILABLE AT	REGISTER SETTINGS
1, 2	OUT1	Set AVG_OUT1 = 10 and EN_CHANNEL_AVG = 1
1, 2	OUT3	Set AVG_OUT3 = 11 and EN_CHANNEL_AVG = 1
3, 4	OUT4	Set AVG_OUT4 = 10 and EN_CHANNEL_AVG = 1
3, 4	OUT2	Set AVG_OUT2 = 11 and EN_CHANNEL_AVG = 1
1, 2, 3, 4	OUT1	Set AVG_OUT1 = 11 and EN_CHANNEL_AVG = 1
1, 2, 3, 4	OUT4	Set AVG_OUT4 = 11 and EN_CHANNEL_AVG = 1
5, 6	OUT5	Set AVG_OUT5 = 10 and EN_CHANNEL_AVG = 1
5, 6	OUT7	Set AVG_OUT7 = 11 and EN_CHANNEL_AVG = 1
7, 8	OUT8	Set AVG_OUT8 = 10 and EN_CHANNEL_AVG = 1
7, 8	OUT6	Set AVG_OUT6 = 11 and EN_CHANNEL_AVG = 1
5, 6, 7, 8	OUT5	Set AVG_OUT5 = 11 and EN_CHANNEL_AVG = 1
5, 6, 7, 8	OUT8	Set AVG_OUT8 = 11 and EN_CHANNEL_AVG = 1

Figure 67. Channel Averaging Info Button

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The *INPUT/OUTPUT MAPPING* section allows the user to remap the analog input channels to any of the digital output channels. The implementation in silicon allows for all combinations of mapping. However, because each combination requires a unique firmware or DLL configuration, the GUI limits the number of combinations available in mapping. To un-grey and enable this section check the **ENABLE MAPPING** checkbox as shown in Figure 68.

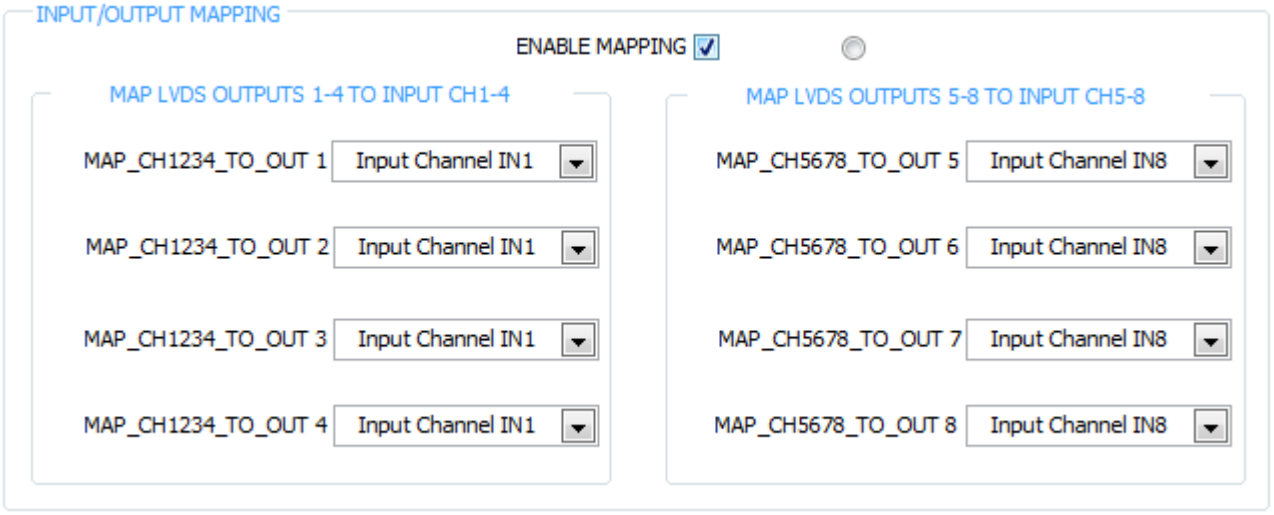

Figure 68. INPUT/OUTPUT MAPPING with EN_INTERLEAVE = 0

The default state of this section shows that output channels 1–4 have mapped the signal that is sampled at analog input channel 1, while channels 5–8 have mapped the signal that is sampled at analog input channel 8. This menu applies if interleaving is disabled. If interleaving is enabled on the *Top Level* tab, then the mapping options reflects this as shown in Figure 69.

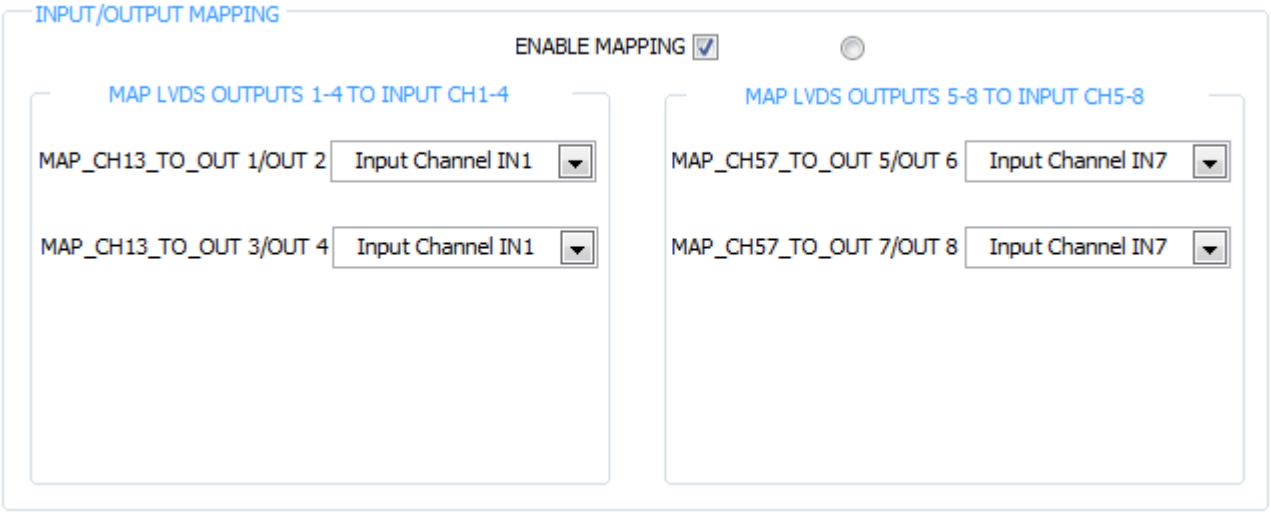

Figure 69. INPUT/OUTPUT MAPPING with EN_INTERLEAVE = 1

The remaining sections of the *Digital Signal Processing* tab are straightforward and explained by the info buttons provided.

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5.5 Channel Filter Tab

The last tab is *Channel Filter* and contains the controls for the decimation filters as well as the integrated high pass filters. As shown in Figure 70, the controls have interdependencies, reflecting the actual silicon implementation.

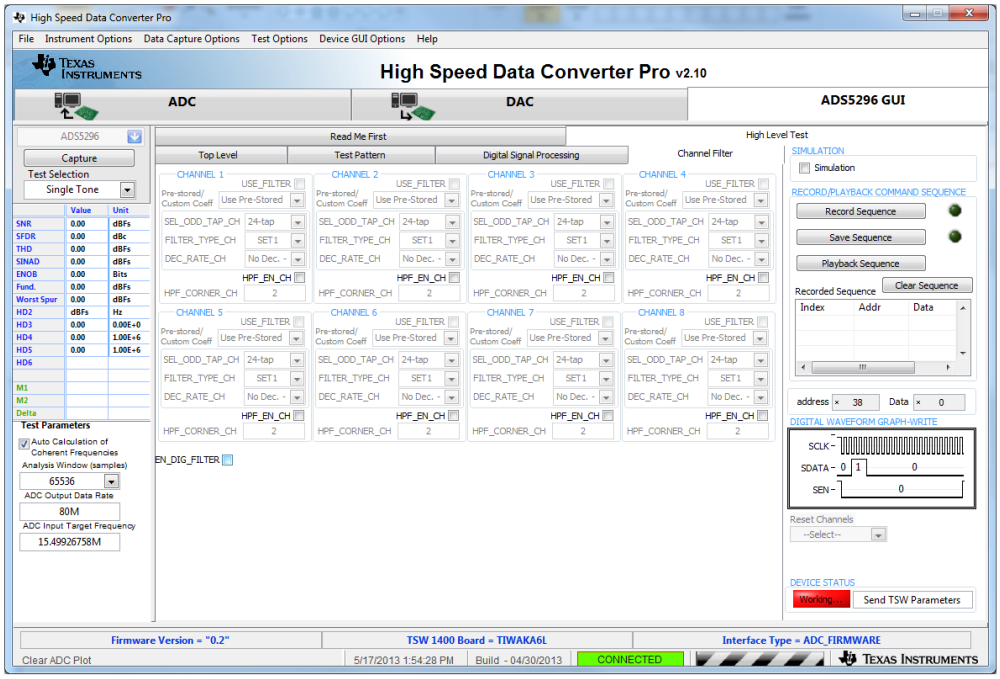

Figure 70. Channel Filter Tab

Checking the **EN_DIG_FILTER** box causes the **USE_FILTER** control to become un-greyed and enabled for all eight channels as shown in Figure 71.

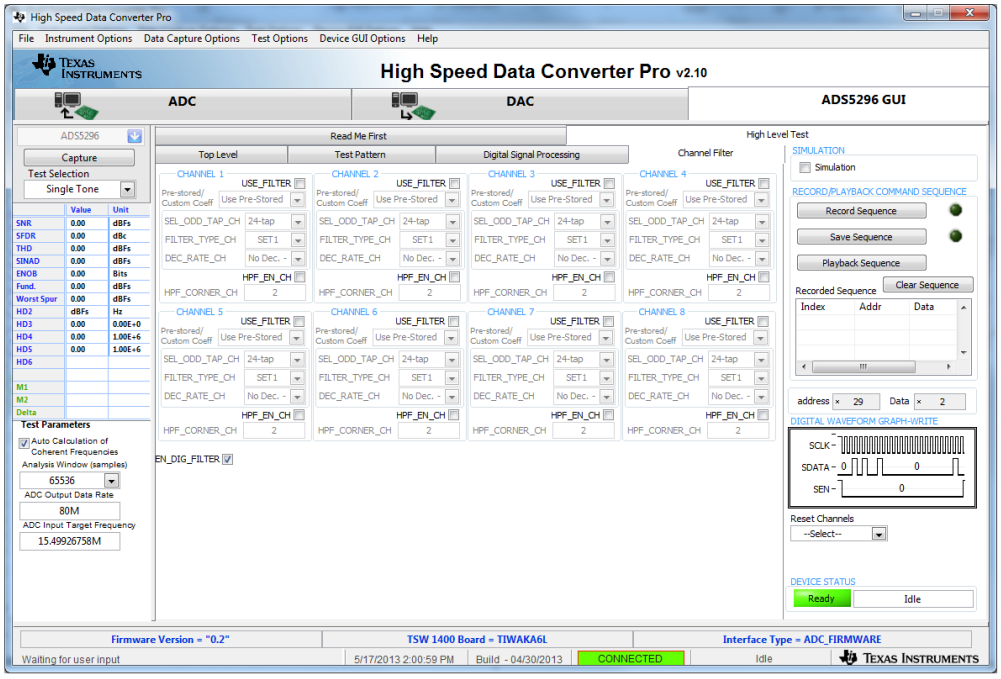

Figure 71. EN_DIG_FILTER = 1

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At this point, the user can invoke the high pass filter for any channel by checking the box **HPF_EN_CH**. The box just below labeled **HPF_CORNER_CH** becomes active, as shown in Figure 72, and the corner frequency can be set to one of sixteen values, with zero being the highest corner frequency available.

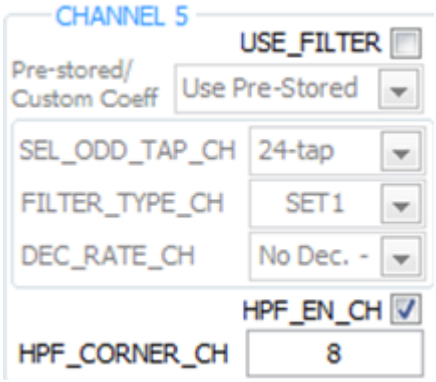

Figure 72. Channel 5 High Pass Filter Enabled

The ADS526's digital processing block includes the option to filter and decimate the ADC outputs digitally. Various decimation rates and filters are supported including decimation by 2, 4, or 8, low-pass, high-pass, and band-pass filters. To invoke this block the **USE_FILTER** box must be checked, thus, enabling all controls associated with the digital and decimation filters as shown in Figure 73.

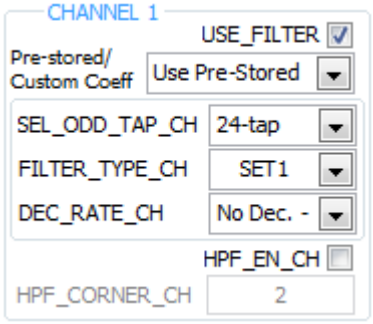

Figure 73. Channel 1 Digital Filter Enabled

The user has the option to use pre-defined filter coefficients or define custom coefficients. When *Use Pre-Stored Filter Coeff* is selected, one of six pre-defined filter types, depending on the state of **FILTER_TYPE_SEL**, will be configured. The Digital Filters Table of the datasheet describes these configurations and is available through the info button on this tab. In addition, the six pre-defined filters are presented graphically at the bottom of the *Channel Filter* tab when the channel chosen to view (from *View Pre-Stored/Custom Filter Coeff* section at bottom left) has *Use Pre-Stored* selected.

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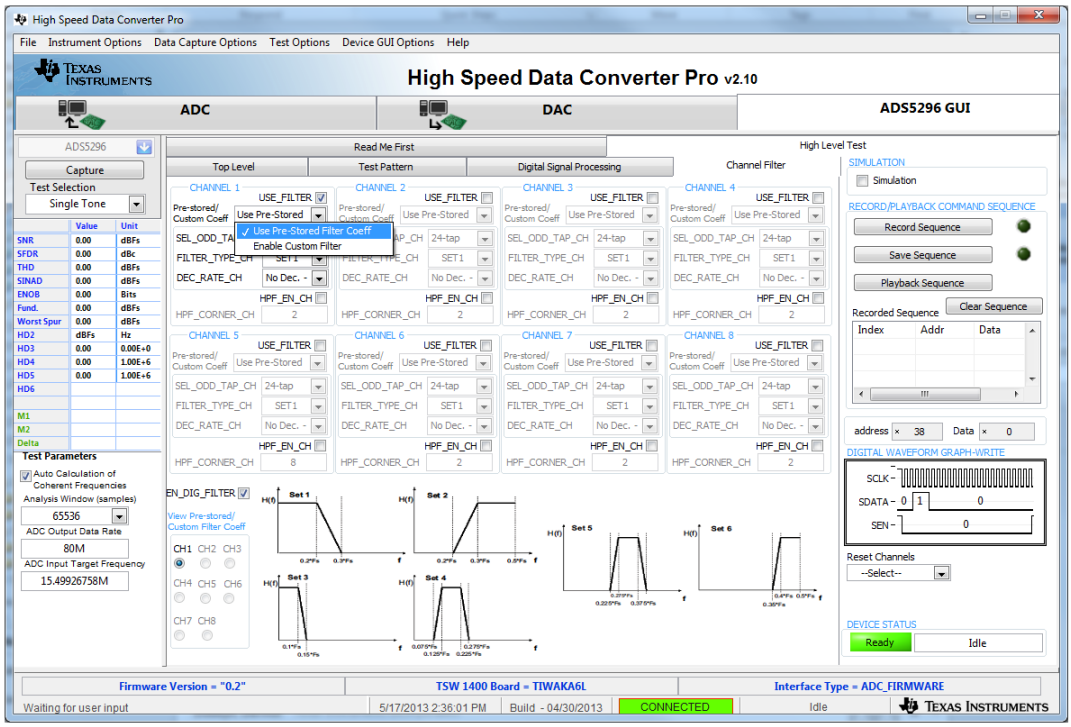

Figure 74. Channel 1 Pre-Stored Digital Filter Enabled

If, instead, *Enable Custom Filter* is selected, then all controls associated with the pre-defined filters become inactive as shown in Figure 75. In addition, the graphs of the pre-stored filters are replaced with the twelve registers that hold the twelve, 12-bit, signed coefficients for one custom filter.

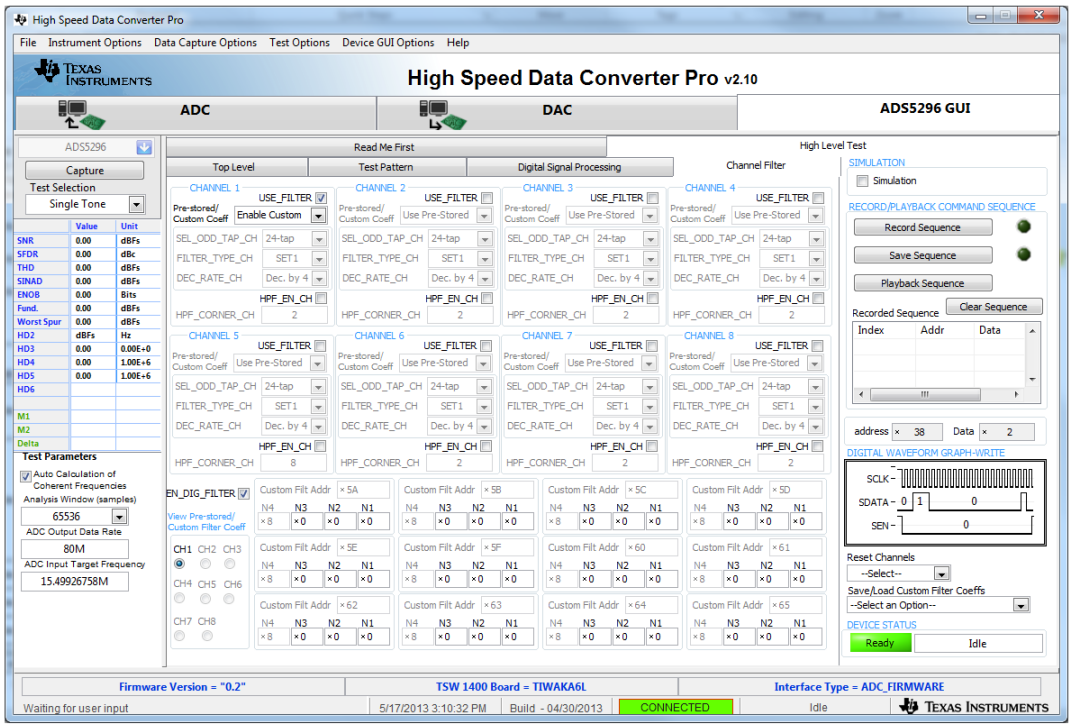

Figure 75. Channel 1 Custom Digital Filter Enabled

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Because of the large number of inputs required to define all eight custom filters (8 × 12 = 96 coefficients), the GUI provides a means for loading coefficients from a text file, saving coefficients to a text file, and resetting filter coefficient values.. This control is located in the bottom right corner of *Channel Filter* tab. As shown in Figure 76, *Reset Channels* can be applied to only Pre-stored Filters, only Custom Filters, or to all filters.

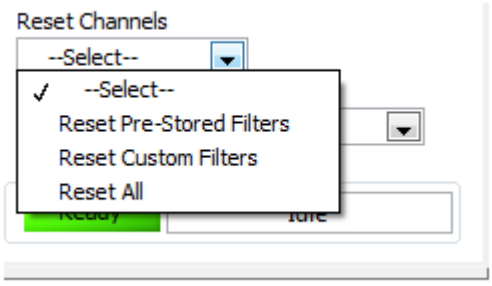

Figure 76. Reset Channels on Channel Filter Tab

The *Save/Load Custom Filter Coeffs* drop-down menu, as shown in Figure 77, can be used to save the currently displayed channel's custom coefficients to a file or all channels' custom coefficients to a file.

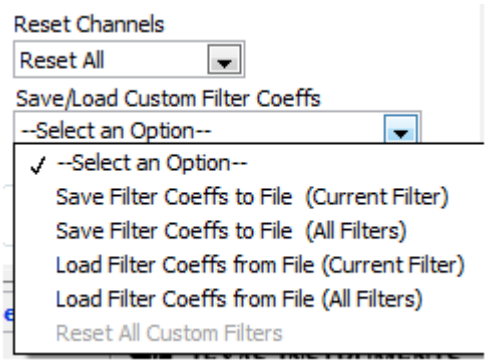

Figure 77. Save/Load Custom Filter Coeffs on Channel Filter Tab

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Likewise, one can load the custom coefficients for the current channel or for all channels. The current channel is indicated on the lower left corner in the *View Pre-stored/Custom Filter Coeff* section shown in Figure 78. Only those channels whose **USE_FILTER** bit are enabled are active, and thus, available for viewing.

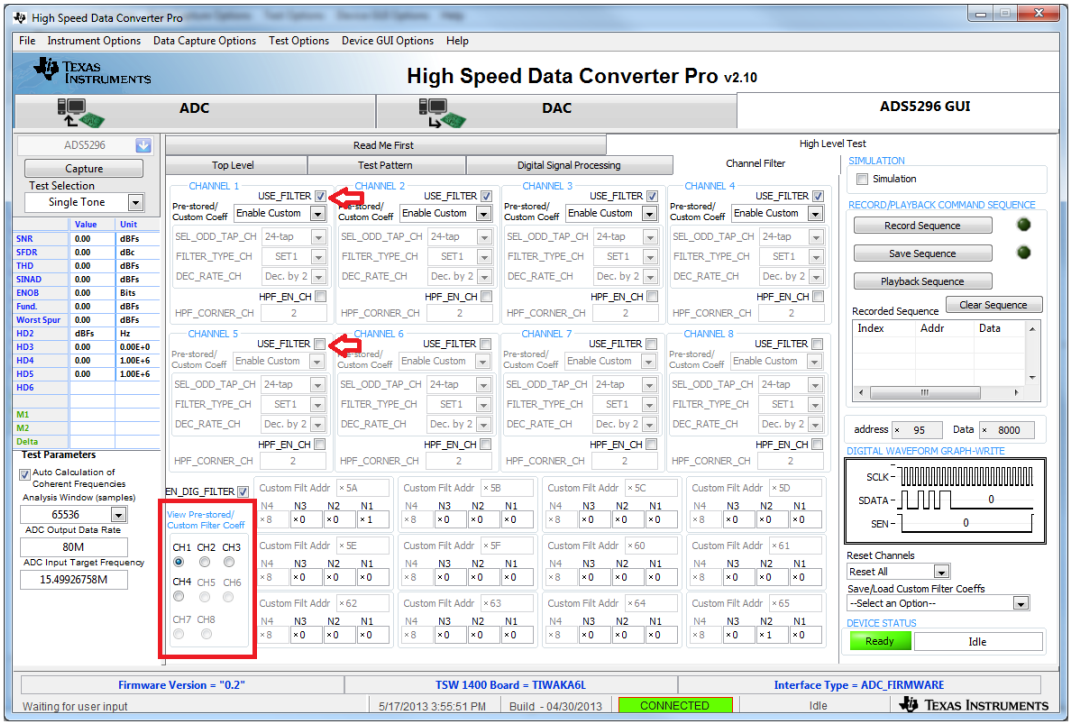

Figure 78. View Filter Coeffs

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6 ADS5296A EVM Schematics

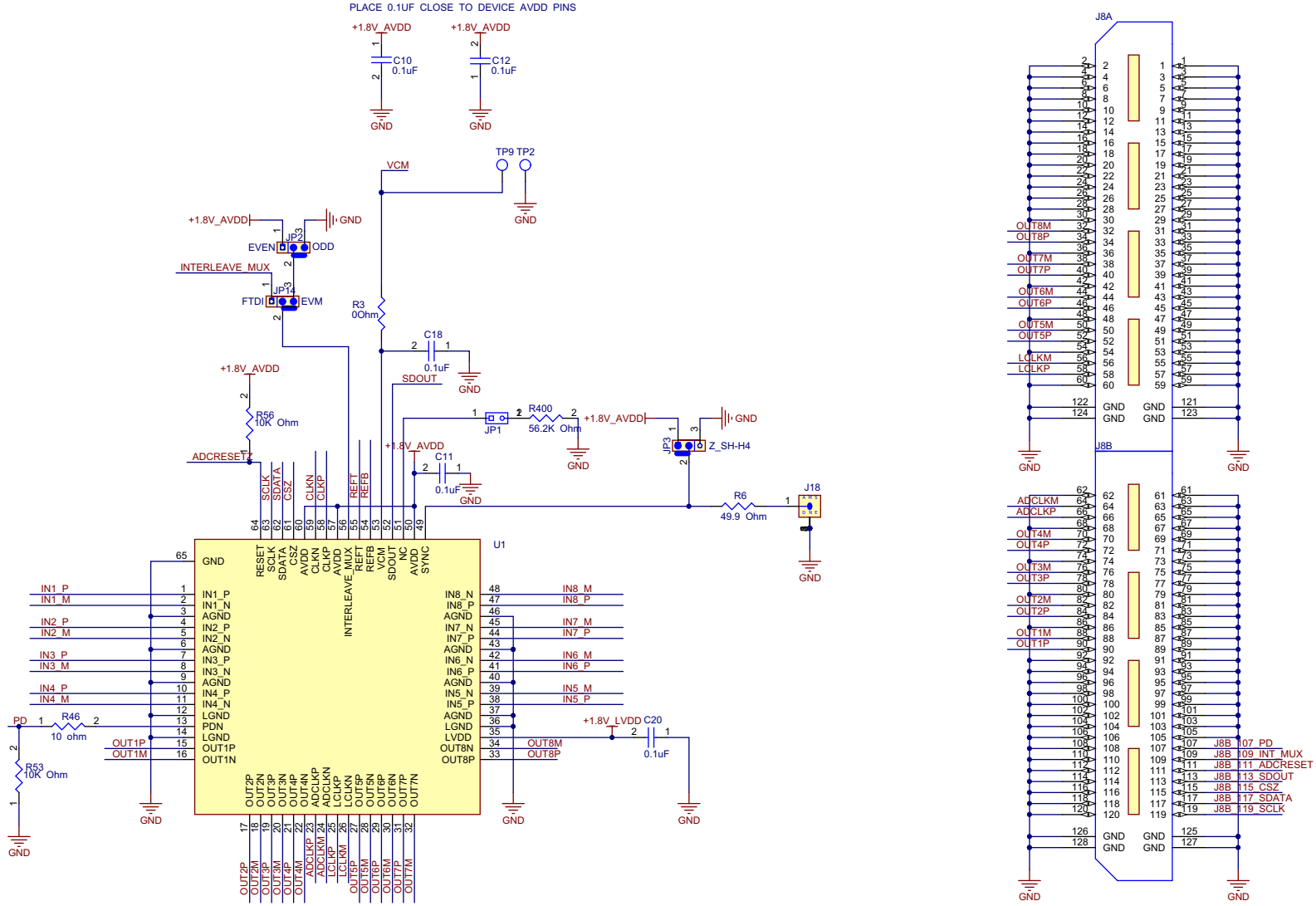

Figure 79. ADS5296A Schematic, Sheet 1 of 9

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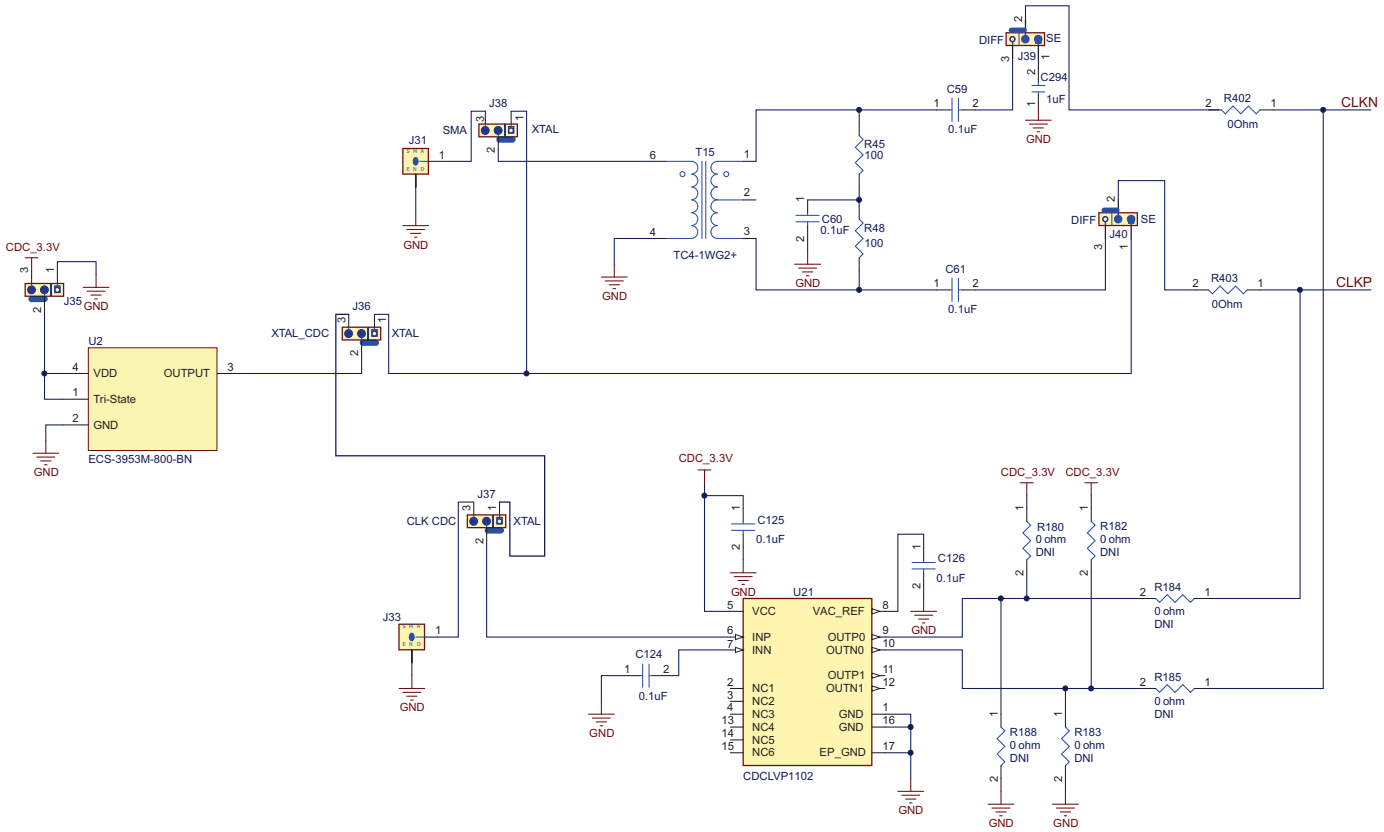

Figure 80. ADS5296A Schematic, Sheet 2 of 9

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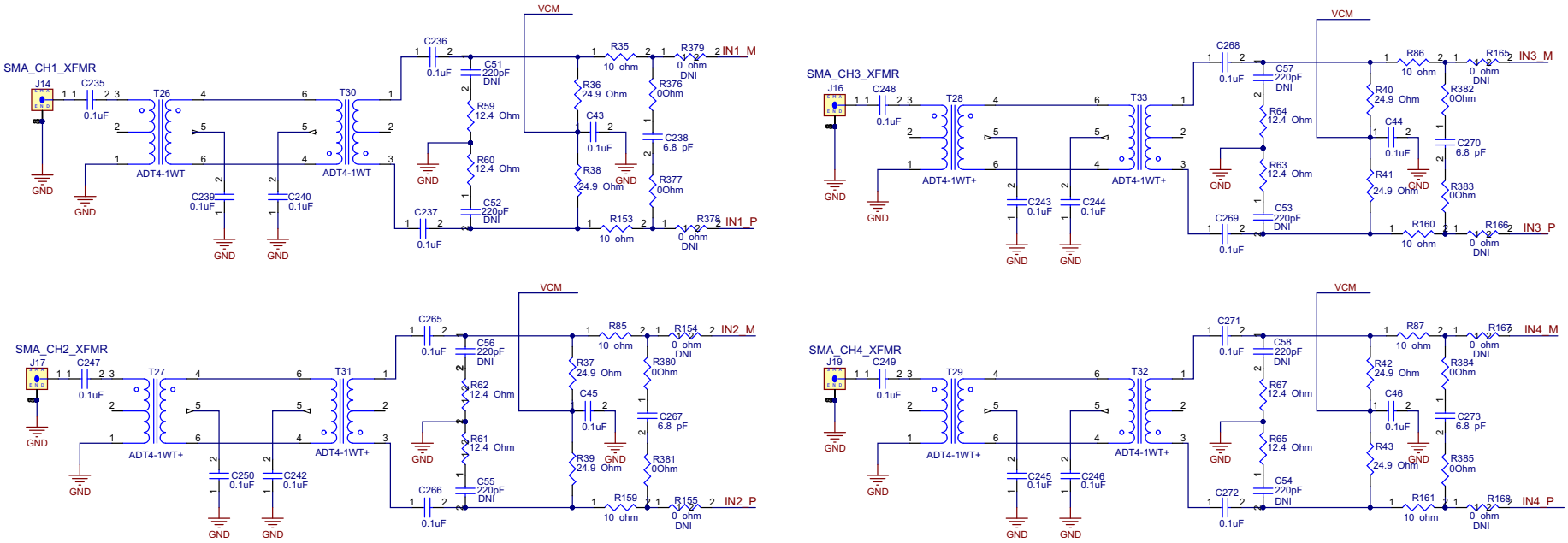

Figure 81. ADS5296A Schematic, Sheet 3 of 9

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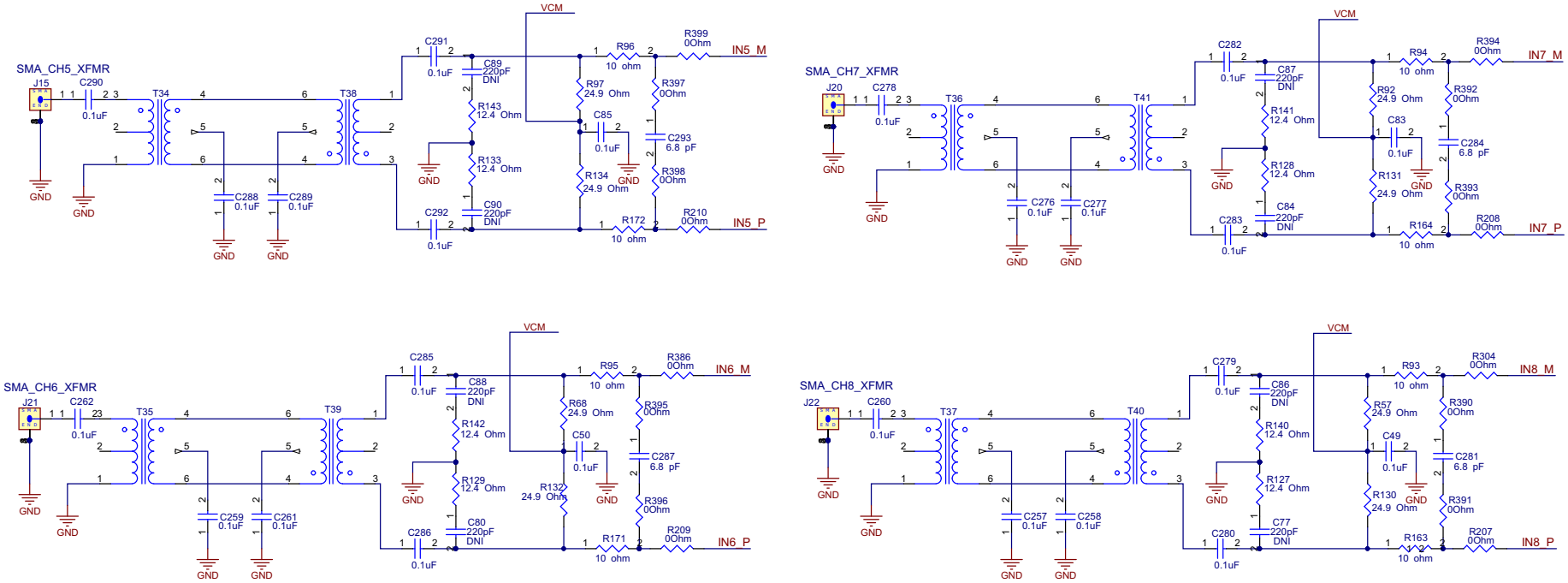

Figure 82. ADS5296A Schematic, Sheet 4 of 9

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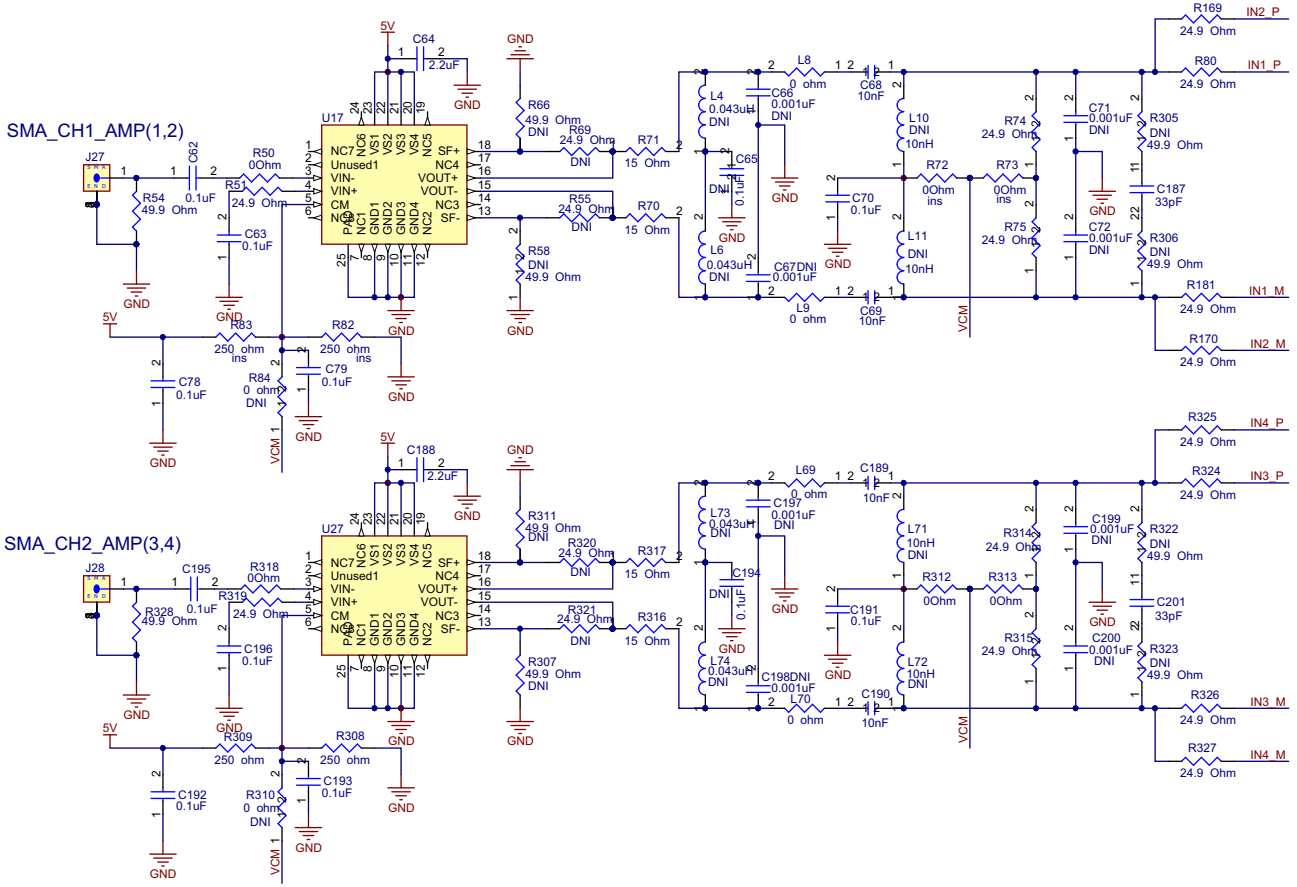

Figure 83. ADS5296A Schematic, Sheet 5 of 9

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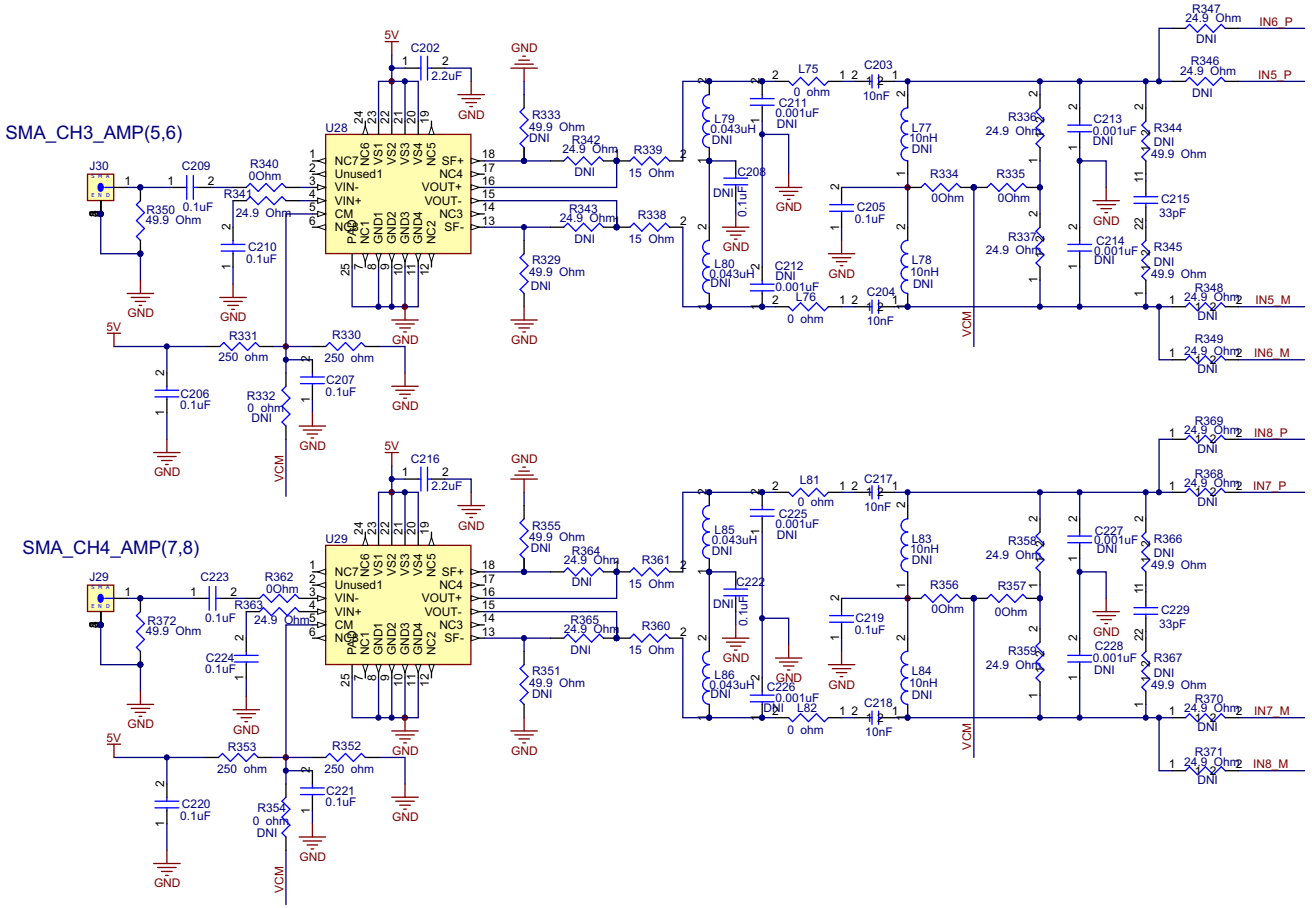

Figure 84. ADS5296A Schematic, Sheet 6 of 9

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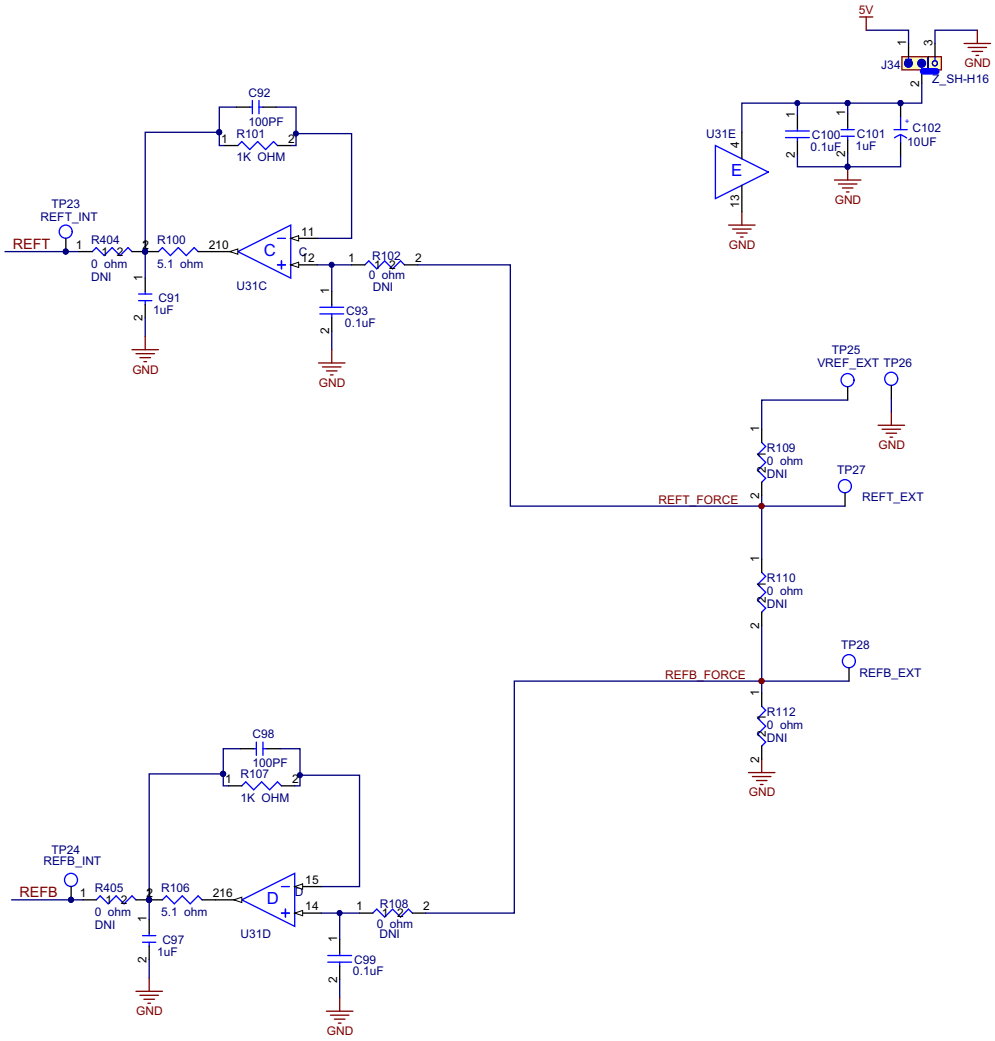

Figure 85. ADS5296A Schematic, Sheet 7 of 9

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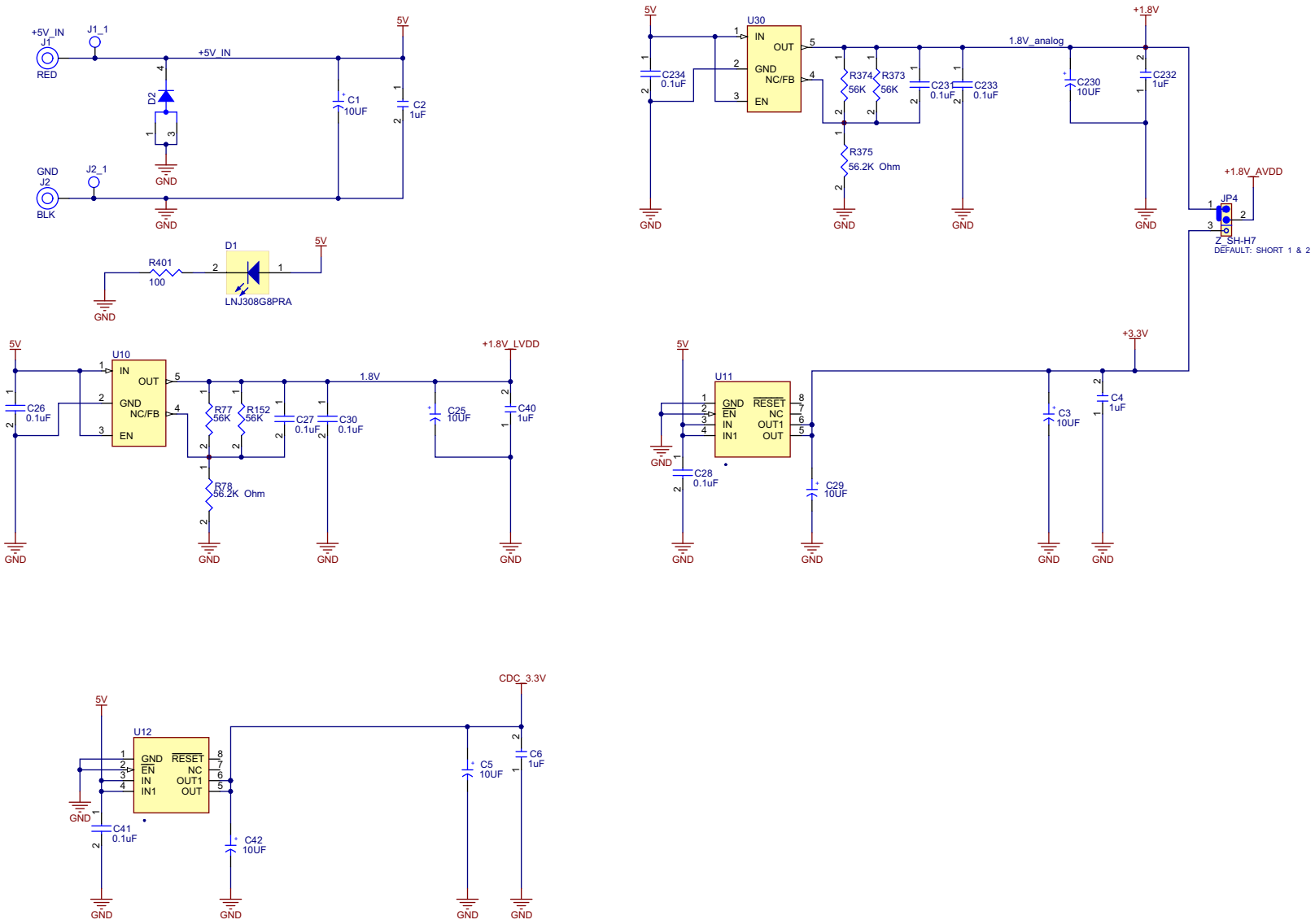

Figure 86. ADS5296A Schematic, Sheet 8 of 9

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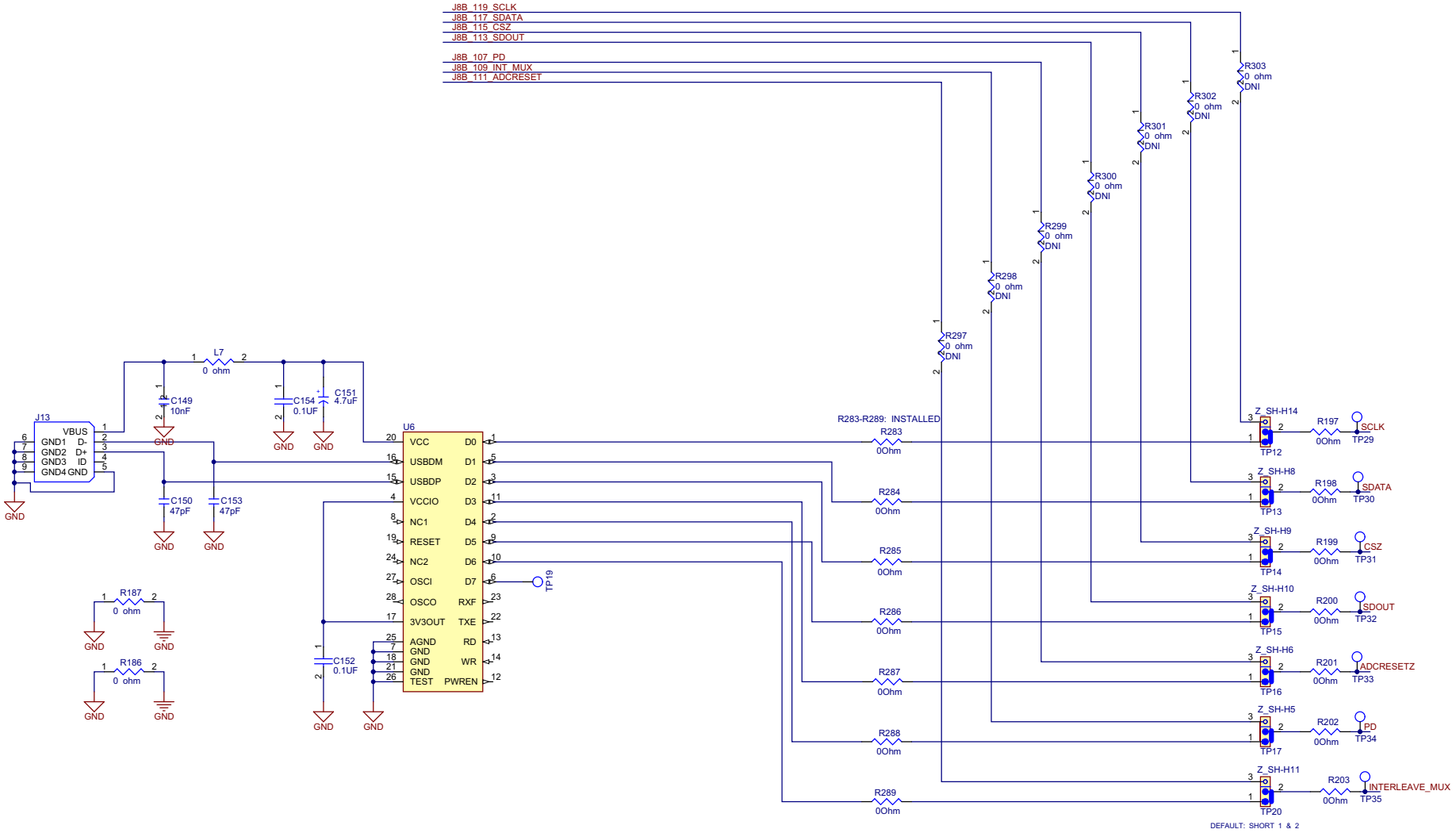

Figure 87. ADS5296A Schematic, Sheet 9 of 9

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7 ADS5296A EVM Bill of Materials

Table 2. ADS5296A EVM Bill of Materials

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
8	C1, C3, C5, C25, C29, C42, C102, C230	10UF	AVX	TAJB106K016RNJ	CAP TANT 10UF 16V 10% 1210
90	C10, C11, C12, C18, C20, C26, C27, C28, C30, C41, C43, C44, C45, C46, C49, C50, C59, C60, C61, C62, C63, C70, C78, C79, C83, C85, C93, C99, C100, C124, C125, C126, C191, C192, C193, C195, C196, C205, C206, C207, C209, C210, C219, C220, C221, C223, C224, C231, C233, C234, C235, C236, C237, C239, C240, C242, C243, C244, C245, C246, C247, C248, C249, C250, C257, C258, C259, C260, C261, C262, C265, C266, C268, C269, C271, C272, C276, C277, C278, C279, C280, C282, C283, C285, C286, C288, C289, C290, C291, C292	0.1uF	AVX	06035C104JAT2A	CAP CER .10UF 50V X7R 10% 0603
1	C149	10nF	MURATA	GRM188R71H103KA01D	CAP 10000PF 50V CERM X7R 0603
2	C150, C153	47pF	MURATA	GRM1885C1H470JA01D	CAP CERAMIC 47PF 50V 0603 SMD
1	C151	4.7uF	AVX	TAJA475K020R	CAP TANTALUM 4.7UF 20V 10% SMD
2	C152, C154	0.1UF	TAIYO YUDEN	GMK105BJ104KV-F	0.1uF 35V X5R 0402
4	C187, C201, C215, C229	33pF	MURATA	GRM1885C1H330JA01D	CAP CER 33PF 50V X7R 10% 0603
9	C2, C4, C6, C40, C91, C97, C101, C232, C294	1uF	AVX	0603YC105KAT2A	CAP CER 1.0UF 16V X7R 10% 0603
8	C238, C267, C270, C273, C281, C284, C287, C293	6.8 pF	MURATA	GRM1885C1H6R8DZ01D	CAP CER 6.8PF 50V NP0 0603
16	C51, C52, C53, C54, C55, C56, C57, C58, C77, C80, C84, C86, C87, C88, C89, C90	220pF	AVX	06035A221FAT2A	DNI; CAP CERM 220PF 1% 50V NP0 0603
4	C64, C188, C202, C216	2.2uF	TDK	C1608X5R1E225K	2.2UF 25V X5R 10% 0603
4	C65, C194, C208, C222	0.1uF	MURATA	GRM1885F51E104ZA01D	DNI
16	C66, C67, C71, C72, C197, C198, C199, C200, C211, C212, C213, C214, C225, C226, C227, C228	0.001uF			DNI
8	C68, C69, C189, C190, C203, C204, C217, C218	10nF	TDK	C1608X7R1H103K	.01uF, 50V, 10%, X7R, 0603
2	C92, C98	100PF	Panasonic	ECH-U1C101JX5	CAP FILM 100PF 16VDC 0603
1	D1	LNJ308G8PRA	PANASONIC	LNJ308G8PRA	LED, GREEN, SMT-0603
1	D2	MBRB2515L	ON Semiconductor	MBRB2515LT4GOSCT-ND	DIODE SCHOTTKY 15V 25A D2PAK
1	J1	RED	ALLIED ELECTRONICS	ST-351A	Banana Female Red
1	J1_1	T POINT R (RED)	Keystone Electronics	5000	
1	J13	USB_MINI_AB	JAE	DX3R005HN2E700	USB_MINI_AB
11	J14, J15, J16, J17, J18, J19, J20, J21, J22, J31, J33	SMA	SAMTEC	SMA-J-P-H-ST-TH1	JACK PANEL MOUNT SMA
1	J2	BLK	ALLIED ELECTRONICS	ST-351B	Banana Female Black
1	J2_1	T POINT R (BLK)	Keystone Electronics	5001	
4	J27, J28, J29, J30	SMA	Johnson	1420-0711-821	Side Mounted SMA
18	J34, J35, J36, J37, J38, J39, J40, JP2, JP3, JP4, JP14, TP12, TP13, TP14, TP15, TP16, TP17, TP20	HEADER 3POS .1 CTR	ANY	JUMPER,3P,.100CC	JUMPER,3P,.100CC
1	J8	QTH-060-02-F-D-A	SAMTEC	QTH-060-02-F-D-A	High speed connector
1	JP1	HEADER_1x2_100_430L	SAMTEC	HMTSW-102-07-G-S-.240	CONN HEADER 2POS .100" T/H GOLD
8	L10, L11, L71, L72, L77, L78, L83, L84	10nH	Stewart	EXC-ML32A680U	DNI
8	L4, L6, L73, L74, L79, L80, L85, L86	0.043uH	Stewart	EXC-ML32A680U	DNI
64	L7, L8, L9, L69, L70, L75, L76, L81, L82, R3, R50, R72, R73, R197, R198, R199, R200, R201, R202, R203, R207, R208, R209, R210, R283, R284, R285, R286, R287, R288, R289, R304, R312, R313, R318, R334, R335, R340, R356, R357, R362, R376, R377, R380, R381, R382, R383, R384, R385, R386, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R402, R403, R404, R405	0 ohm	PANASONIC	ERJ-3GEY0R00V	RESISTOR,SMT,0603,0 OHM,5%,ZERO OHM JUMPER

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Table 2. ADS5296A EVM Bill of Materials (continued)

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
2	R100, R106	5.1 ohm	VISHAY	CRCW06035R10FKEA	RES 5.10 OHM 1/10W 1% 0603 SMD
2	R101, R107	1K OHM	TYCO ELECTRONICS	CRG0603F1K0	RES 1.00K OHM 1/10W 1% 0603
2	R186, R187	0 ohm	PANASONIC	ERJ-2GE0R00X	RES 0 OHM 1/16W 1% 0402 SMD
17	R35, R46, R85, R86, R87, R93, R94, R95, R96, R153, R159, R160, R161, R163, R164, R171, R172	10 ohm	PANASONIC	ERJ-3GEYJ100V	RES 10.0 OHM 0603 SMD
36	R36, R37, R38, R39, R40, R41, R42, R43, R51, R57, R68, R74, R75, R80, R92, R97, R130, R131, R132, R134, R169, R170, R181, R314, R315, R319, R324, R325, R326, R327, R336, R337, R341, R358, R359, R363	24.9 Ohm	PANASONIC	ERJ-3EKF24R9V	RES 24.9 OHM 1/10W 1% 0603 SMD
3	R45, R48, R401	100	Panasonic	ERJ-3GEYJ101V	RES 100 OHM 1/10W 5% 0603 SMD
2	R53, R56	10K Ohm	PANASONIC	ERJ-3EKF1002V	RES 10.0K OHM 1/10W 1% 0603 SMD
16	R55, R69, R320, R321, R342, R343, R346, R347, R348, R349, R364, R365, R368, R369, R370, R371	24.9 Ohm	PANASONIC	ERJ-3EKF24R9V	DNI; RES 24.9 OHM 1/10W 1% 0603 SMD
16	R58, R66, R305, R306, R307, R311, R322, R323, R329, R333, R344, R345, R351, R355, R366, R367	49.9 Ohm	PANASONIC	ERJ-3EKF49R9V	DNI; RES 49.9 OHM 1/10W 1% 0603 SMD
16	R59, R60, R61, R62, R63, R64, R65, R67, R127, R128, R129, R133, R140, R141, R142, R143	12.4 Ohm	PANASONIC	ERJ-3EKF12R4V	RES 12.4 OHM 1/10W 1% 0603 SMD
5	R6, R54, R328, R350, R372	49.9 Ohm	PANASONIC	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
8	R70, R71, R316, R317, R338, R339, R360, R361	15 Ohm	PANASONIC	ERJ-3EKF15R0V	RES 15 OHM 1/10W 1% 0603 SMD
4	R77, R152, R373, R374	56K	PANASONIC	ERJ-3EKF5602V	RES 56.0K OHM 1/10W 1% 0603 SMD
3	R78, R375, R400	56.2K Ohm	PANASONIC	ERJ-3EKF5622V	RES 56.2K OHM 1/10W 1% 0603 SMD
8	R82, R83, R308, R309, R330, R331, R352, R353	250 ohm	VISHAY	PLT0603Z2500AST5	RES 250 OHM 0.05% 5PPM 0603 SMD
30	R84, R102, R108, R109, R110, R112, R154, R155, R165, R166, R167, R168, R180, R182, R183, R184, R185, R188, R297, R298, R299, R300, R301, R302, R303, R310, R332, R354, R378, R379	0 ohm	PANASONIC	ERJ-3GEY0R00V	DNI; RESISTOR,SMT,0603,0 OHM,5%,ZERO OHM JUMPER
1	T15	TC4-1WG2+	Mini-Circuits	TC4-1WG2+	
16	T26, T27, T28, T29, T30, T31, T32, T33, T34, T35, T36, T37, T38, T39, T40, T41	ADT4-1WT	Mini-Circuits	ADT4-1WT+	
16	TP2, TP9, TP19, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35	T POINT R	Keystone Electronics	5001	
1	U1	ADS5296A	Texas Instruments	ADS5296IRGC	TI Supplied Device
2	U10, U30	TPS73201-SOT23	Texas Instruments	TPS73201DBVR	IC LDO REG 250MA ADJ-V SOT23-5
2	U11, U12	TPS77533D	Texas Instruments	TPS77533D	IC 3.3V 500MA LDO REG 8-SOIC
4	U17, U27, U28, U29	THS770006	Texas Instruments	THS770006IRGER	IC AMP DIFF ADC DVR 16BIT 24VQFN
1	U2	80 MHZ	ECS INC	ECS-3953M-800-BN	OSCILLATOR, 80 MHZ, 4-PIN
1	U21	CDCLVP1102	Texas Instruments	CDCLVP1102RGTT	IC CLK BUFF 1:2 LVPECL SGL 16QFN
1	U31	2.7 V TO 5.5 V	TEXAS INSTRUMENTS	OPA4353EA	IC OPAMP GP R-R 44MHZ 16QSOP
1	U6	FT245RL	FTDI Chip	FT245RL	IC USB TO PARALLEL FIFO 28-SSOP
18	Z_SH-H3, Z_SH-H4, Z_SH-H5, Z_SH-H6, Z_SH-H7, Z_SH-H8, Z_SH-H9, Z_SH-H10, Z_SH-H11, Z_SH-H14, Z_SH-H16, Z_SH-H17, Z_SH-H18, Z_SH-H19, Z_SH-H20, Z_SH-H21, Z_SH-H22, Z_SH-H23	SHUNT-HEADER	Keltron	MJ-5.97-G-F1 or equivalent	SHUNT FOR HEADER

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8 ADS5296A EVM Layout

Figure 88 through Figure 93 illustrate the PCB layouts for the EVM.

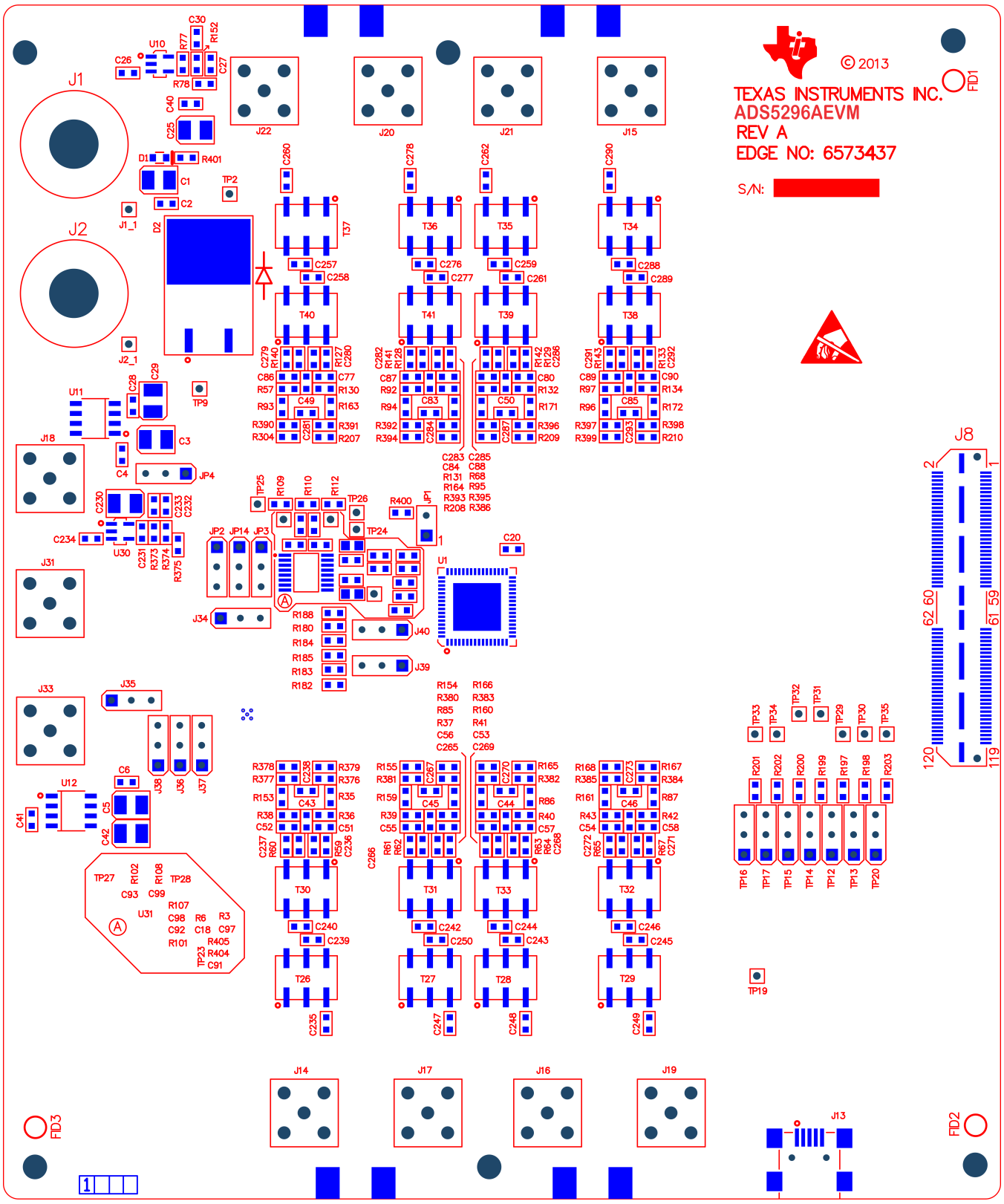

Figure 88. ADS5296A EVM Top Layer Assembly Drawing – Top View

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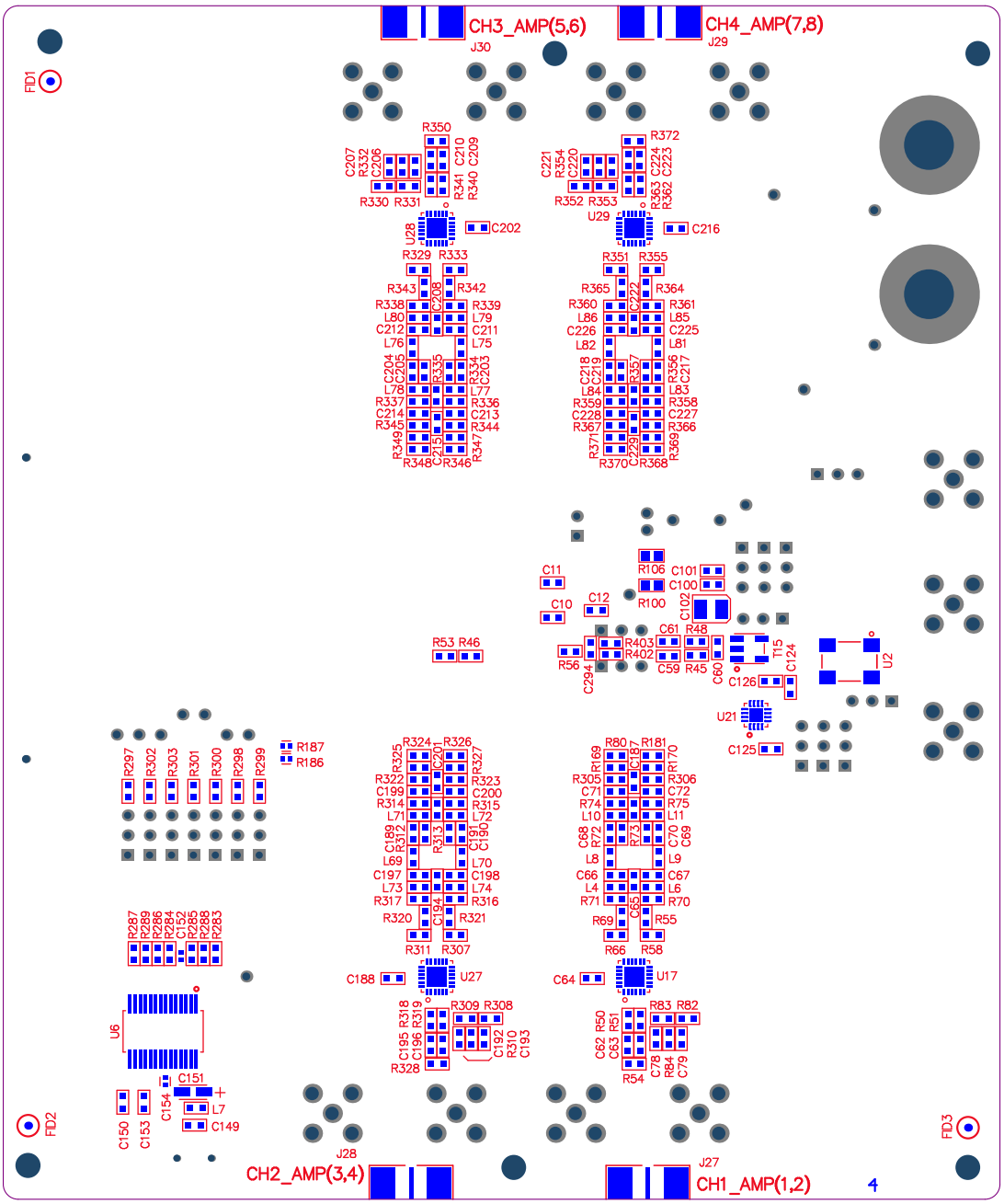

Figure 89. ADS5296A EVM Bottom Layer Assembly Drawing – Bottom View

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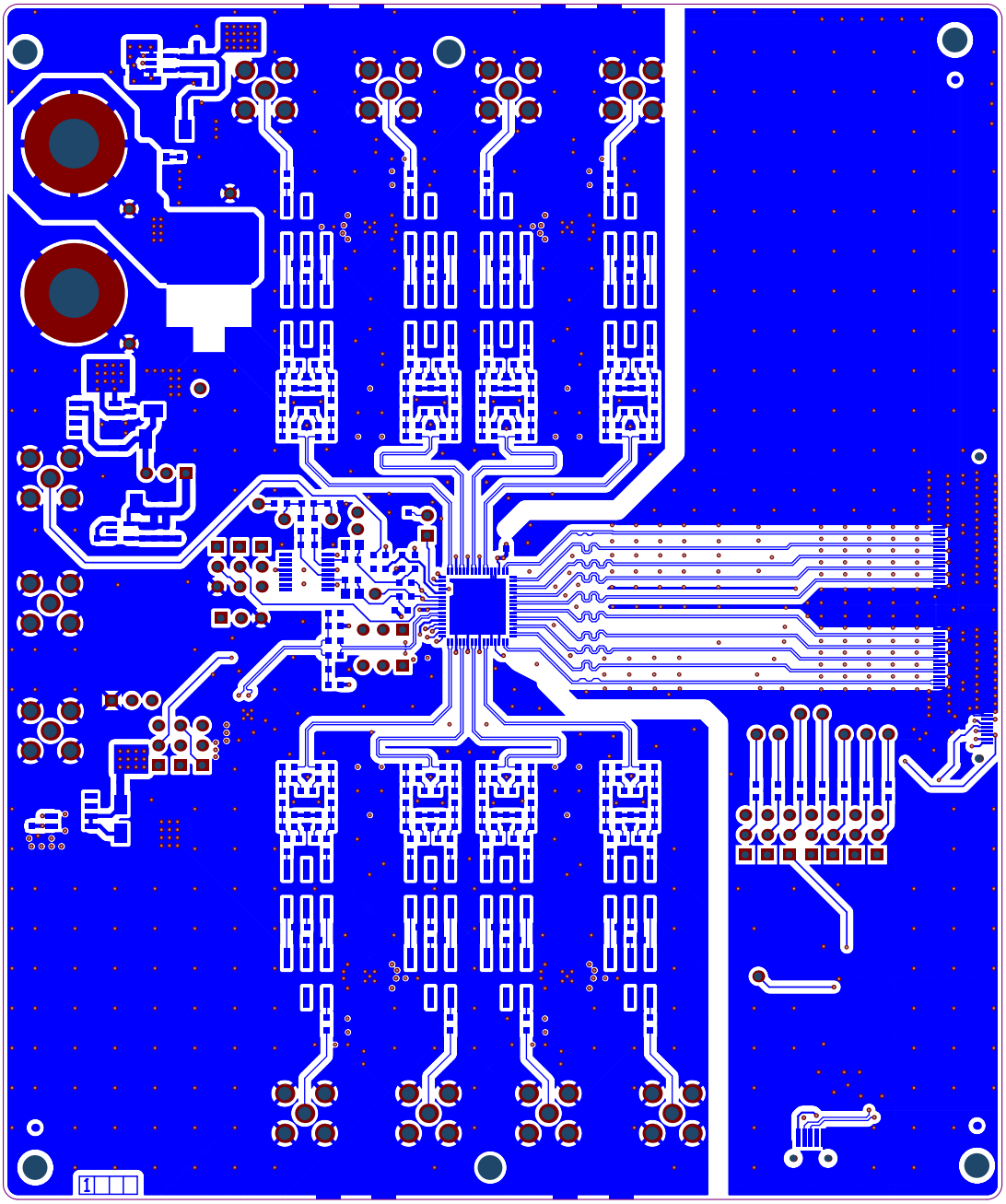

Figure 90. ADS5296A EVM Top Side

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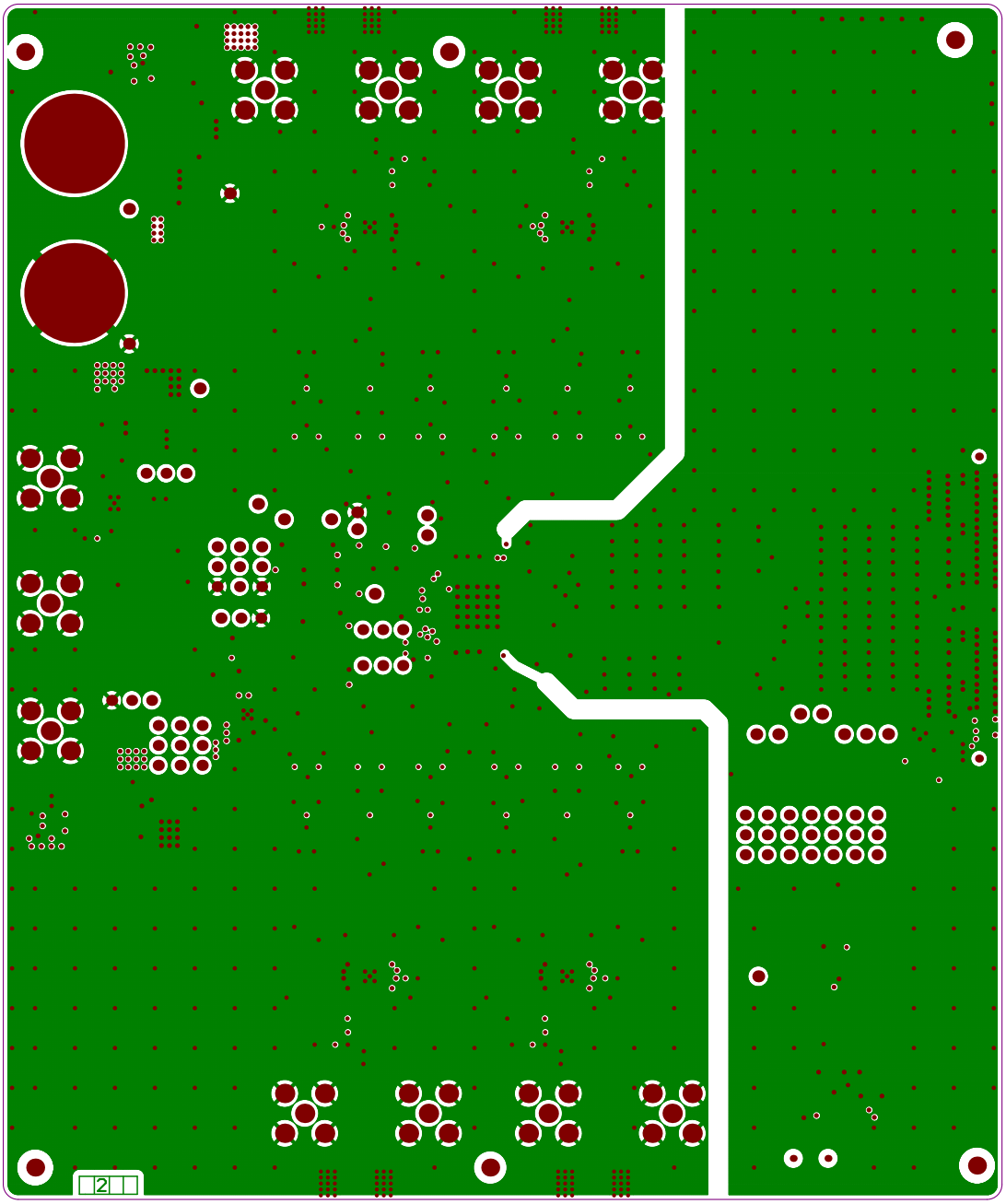

Figure 91. ADS5296A EVM Ground Plane

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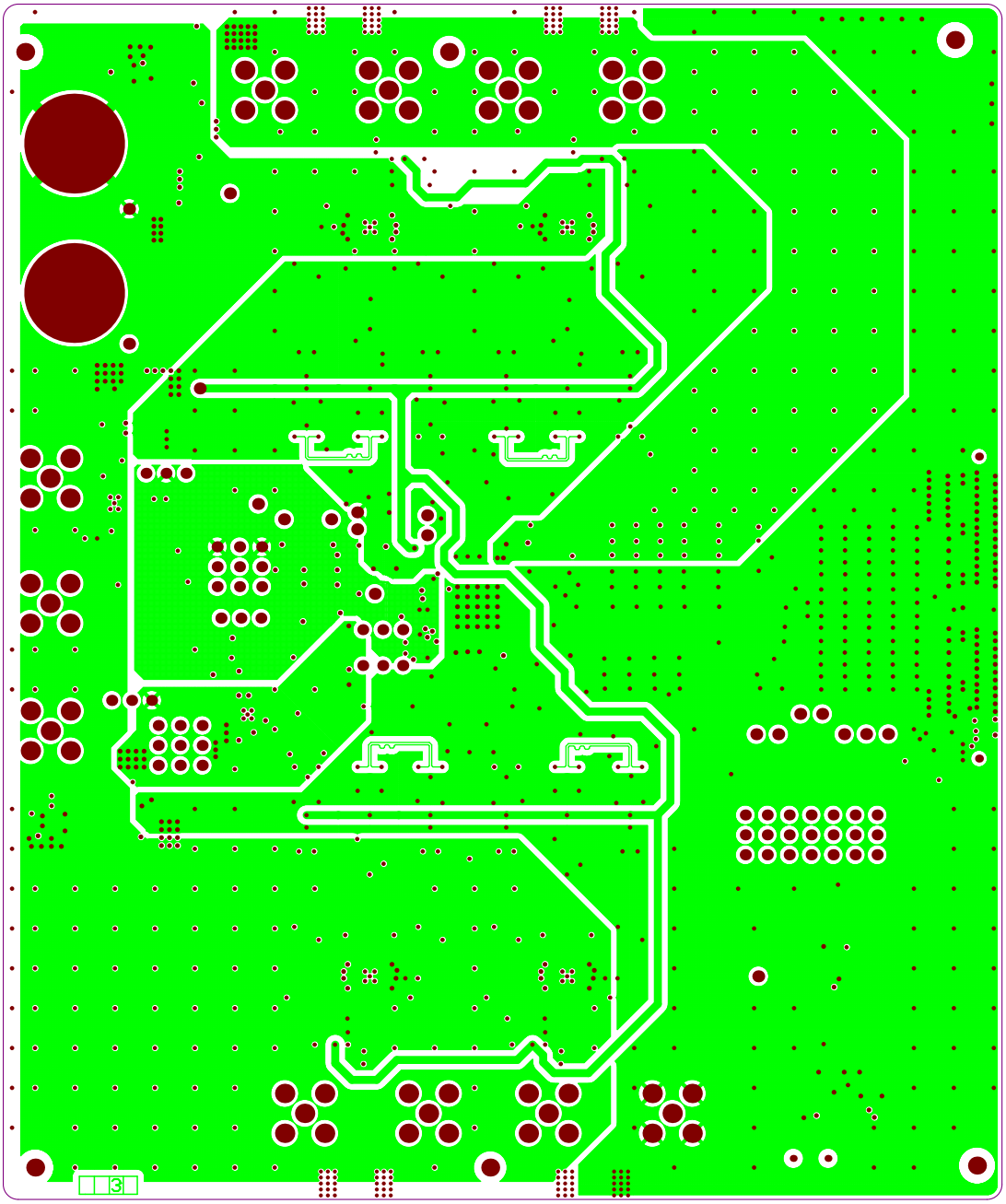

Figure 92. ADS5296A EVM Signal Plane

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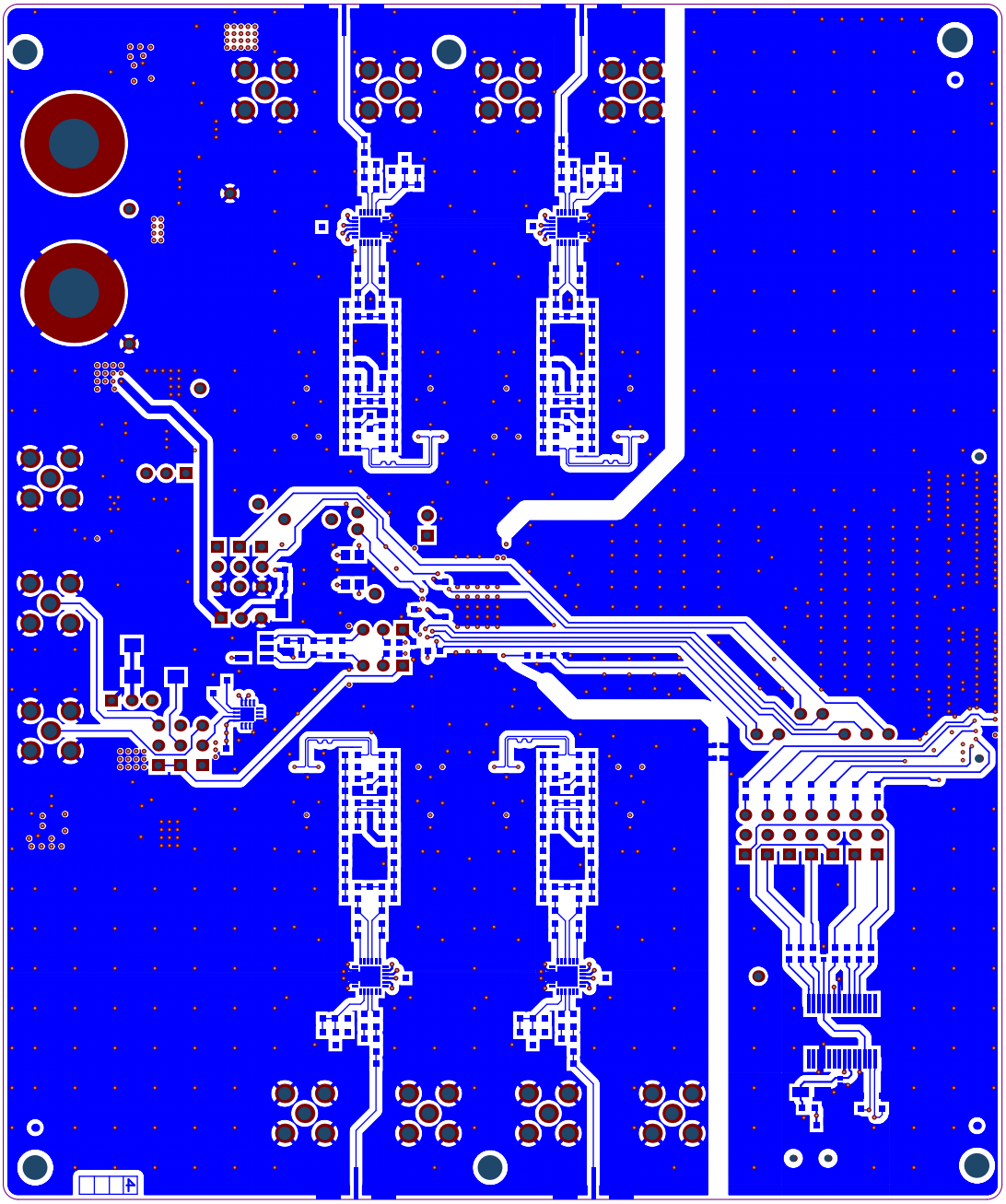

Figure 93. ADS5296A EVM Bottom Side

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

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