This user’s guide describes the characteristics, operation, and use of TI’s TSW16DX370EVM Rev B. The equipment required, setup procedures, device configuration, and an evaluation and troubleshooting section are also included.
Contents

1 Introduction ........................................................................................................................................ 3
2 Equipment ......................................................................................................................................... 4
  2.1 Evaluation Board Feature Identification Summary ................................................................. 4
  2.2 Required Equipment ..................................................................................................................... 4
3 Setup Procedure ............................................................................................................................... 5
  3.1 Install the High Speed Data Converter Pro (HSDC Pro) Software ......................................... 6
  3.2 Install the Configuration GUI Software ...................................................................................... 6
  3.3 Connect the EVM and TSW14J56EVM ..................................................................................... 6
  3.4 Connect the Power Supplies to the Boards ................................................................................. 6
  3.5 Connect the Signal Generators to the EVM (RF Signal OFF) .................................................... 6
  3.6 Connect the EVM and TSW14J56EVM to the PC ................................................................. 7
  3.7 Open the HSDP Software and Load the FPGA Image to the TSW14J56EVM ......................... 7
  3.8 Program the EVM Using the Configuration GUI in the HSDC Pro Software ......................... 7
  3.9 Verify TSW14J56EVM Switch Settings, Initialize the JESD204B Link (CPU_RESET), and Verify TSW14J56EVM Status LEDs ........................................................... 8
  3.10 Turn the Signal Generator RF Outputs ON ............................................................................. 8
  3.11 Capture Data Using the HSDP Software .................................................................................. 8
  3.12 Re-Verify TSW14J56EVM Status LEDs .................................................................................. 9
4 Device Configuration ......................................................................................................................... 10
  4.1 Supported JESD204B Features ................................................................................................. 10
  4.2 Using the Device Configuration GUI ....................................................................................... 10
  4.3 Low-Level Control .................................................................................................................... 19
5 Evaluation Troubleshooting ............................................................................................................ 20

Appendix A .......................................................................................................................................... 21

List of Figures

1 EVM Feature Locations ...................................................................................................................... 4
2 EVM Test Setup ............................................................................................................................... 5
3 High Speed Data Converter Pro (HSDP) GUI ................................................................................. 9
4 Configuration GUI INTRO Tab ......................................................................................................... 11
5 Configuration GUI ADC CORE Tab ............................................................................................... 12
6 Configuration GUI JESD240B Tab ................................................................................................. 12
7 LMH6521 Tab ................................................................................................................................. 13
8 LMK04828 MACRO CONFIG Tab ................................................................................................. 13
9 LMK04828 PLL1 Config Tab ............................................................................................................ 15
10 LMK04828 PLL2 Config Tab ......................................................................................................... 15
11 LMK04828 SYSREF and SYNC Tab ............................................................................................ 16
12 LMK04828 Clock Outputs Tab ...................................................................................................... 16
13 LMX2581 MACRO CONFIG Tab ................................................................................................. 17
14 LMX2581 PLL Config Tab ............................................................................................................ 18
15 Low-Level Register Control Tab .................................................................................................. 19

List of Tables

1 Default State of LEDs on the TSW14J56EVM During Normal Operation .................................. 8
2 Default State of LEDs on the TSW14J56EVM During Normal Operation .................................. 9
3 Troubleshooting Procedures ........................................................................................................ 20
4 EVM Jumper Settings ..................................................................................................................... 21
5 Meaning of LEDs on the TSW14J56EVM ..................................................................................... 21
6 Required State of Switches on the TSW14J56EVM ...................................................................... 22
1 Introduction

The TSW16DX370EVM is a reference design board used to evaluate the receiver IF subsystem solution with over 100-MHz usable bandwidth including the following products from Texas Instruments:

- ADC16DX370 dual channel 16-bit analog-to-digital converter (ADC) sampling at 368.64 MSPS
- LMH6521 dual digitally controlled variable gain amplifier (DVGA)
- TRF37B32 dual down-converting mixer with integrated IF amplifier
- LMX2581 wideband frequency synthesizer with integrated VCO
- LMK04828 ultra low jitter synthesizer and jitter cleaner

This evaluation board also includes the following important features:

- High speed serial JESD204B data output over a standard FMC interface connector.
- Device register programming via USB connector and FTDI USB-to-SPI bus translator for all devices.

The digital data from the TSW16DX370EVM board can be quickly and easily captured with the TSW14J56EVM data capture board. The TSW14J56EVM captures the high speed serial data, decodes the data, stores the data in memory, and then uploads it for analysis to a connected PC via a USB interface. The High Speed Data Converter Pro (HSDC Pro) software on the PC communicates with the hardware and processes the data.

With proper hardware selection in the HSDC Pro software, the TSW14J56 is automatically configured to support a data capture from the ADC16DX370EVM at the default sampling rate of 368.64 MSPS and serial data rate of 7.3728 Gbps.

For the rest of this document, the following references apply:

- The TSW16DX370EVM evaluation board is referred to only as ‘EVM’
- The ADC16DX370 device is referred to only as ‘ADC’
- The LMH6521 device is referred to only as ‘LMH’
- The TRF37B32 device is referred to only as ‘TRF’
- The LMX2581 is referred to only as ‘LMX’
- The LMK04828 is referred to only as ‘LMK’
2 Equipment

This section describes how to setup the EVM on the bench with the proper equipment to evaluate the full performance of the reference design.

2.1 Evaluation Board Feature Identification Summary

![Figure 1. EVM Feature Locations](image)

2.2 Required Equipment

The following equipment and documents are included in the EVM evaluation kit:

- Evaluation board (EVM)
- User’s guide (this document)
- Power supply cable with barrel connector and flying leads (for connection of the EVM to a +6-V bench power supply)
- Mini-USB cable

**CAUTION**

Ensure that the power cable is connected to the bench power supply and EVM with the correct polarity. Connecting the cable with an incorrect polarity may damage the EVM. Testing the voltage at the output of the power cable (at the barrel connector) is recommended before connecting the power cable to the EVM.

The following list of equipment contains items that are not included in the EVM evaluation kit but the items are required for evaluation of this product:

- TSW14J56EVM data capture board plus power cable and mini-USB cable
- High Speed Data Converter Pro software
- PC running Microsoft® Windows® 8, Windows 7, or Windows XP
Setup Procedure

- 2x (or dual-channel) Bench power supplies capable of +6V/2A and +5V/2A
- One (1) Low-Noise Signal Generator. The following generators are recommended:
  - RF generator, > +17 dBm, ≤ 40 dBc harmonics, < 500 fs jitter 20 kHz – 20 MHz, 10 MHz – 2 GHz frequency range
  - HP HP8644B
  - Rohde & Schwarz SMA100A
- Bandpass filter for analog input for desired RF input frequency from 700–2700MHz. The following filters are recommended:
  - Bandpass filter, ≥ 60-dB harmonic attenuation, ≤ 5% bandwidth, > +18-dBm power, < 5-dB insertion loss
  - Trilithic 5VH-series Tunable BPF
  - K&L BT-series Tunable BPF
  - TTE KC6 or KC7-series Fixed BPF
- 3-dB resistive attenuator, SMA, 50 Ω
- Signal path cables, SMA or BNC

3 Setup Procedure

Figure 2. EVM Test Setup
3.1 Install the High Speed Data Converter Pro (HSDC Pro) Software

Download the most recent version of the HSDP software from the High Speed Data Converter Pro Software product page. Follow the installation instructions to install the software.

**CAUTION**
The HSDC Pro software must be installed before connecting the TSW14J56EVM to the PC for the first time.

3.2 Install the Configuration GUI Software

1. Download the configuration GUI software from the TSW16DX370EVM product page at www.ti.com
2. Extract files from the zip file
3. Run setup.exe and follow the installation instructions

3.3 Connect the EVM and TSW14J56EVM

With the power off, connect the EVM to the TSW14J56EVM via the FMC connector as shown in Figure 2. Check that the standoffs provide the proper height for robust connector connections.

3.4 Connect the Power Supplies to the Boards

1. Confirm that the power switch on the TSW14J56EVM is in the OFF position.
2. Connect the power cable for the TSW14J56EVM to the bench power supply and test the voltage and polarity at the cable output. The barrel connector core must be +5V relative to the outside shield.
3. Connect the power cable with +5V to the TSW14J56EVM.
4. Turn the power switch of the TSW14J56EVM to the ON position.
5. Connect the power cable for the TSW16DX370EVM to the bench power supply and test the voltage and polarity at the cable output. The barrel connector core must be +6V relative to the outside shield.
6. Connect the power cable with +6V to the TSW14J56EVM.

**CAUTION**
Ensure that the power cable is connected to the bench power supply and EVM with the correct polarity. Connecting the cable with an incorrect polarity may damage the EVM. Testing the voltage at the output of the power cable (at the barrel connector) is recommended before connecting the power cable to the EVM.

3.5 Connect the Signal Generators to the EVM (RF Signal OFF)

1. Connect a signal generator to the RFINA input of the EVM through a bandpass filter and attenuator at the SMA connector. This must be a low noise signal generator. A trilithic tunable bandpass filter is recommended to filter the signal from the generator. Configure the signal generator for –25 dBm, 1750 MHz.
   • **Important**: Coherent sampling of the input signal is not possible with the default hardware configuration of this EVM. A windowing function must be used in HSDC Pro for FFT analysis
2. **Do not yet** turn on the RF output of the signal generator.

**CAUTION**
This TRF device at the input of this reference design has an IP1dB = +29 dBm, but the signal path gain may cause saturation for sinusoidal signals as low as –24 dBm.
3.6 Connect the EVM and TSW14J56EVM to the PC
1. Connect the EVM to the PC with the Mini-USB cable
2. Connect a Mini-USB cable from the PC to the TSW14J56EVM.
3. If this is the first time connecting the TSW14J56EVM to the PC, then follow the on-screen instructions to automatically install the device drivers. See the TSW14J56EVM user’s manual for more specific instructions.

3.7 Open the HSDP Software and Load the FPGA Image to the TSW14J56EVM
1. Open the HSDP software
2. Press OK to confirm the serial number of the TSW14J56EVM device
3. Select the ‘TSW16DX370EVM’ device from the ADC select drop-down in the top left corner and Press YES to update the firmware.
   • Important: Configuring the ADC16DX370 with options other than the default register values may require different instructions for selecting the device in HSDC Pro. See the appendix for more details.

   NOTE: Depending on the quality of the signal generator used for the input signal, a bandpass filter may not be required. The EVM achieves ~70 dB of selectivity outside the IF passband, attenuating the spurs of most signal generators to insignificant levels.

4. Enter the ADC sampling rate (Fs) as ‘368.64M’ or the desired sampling rate
   • This number should be equal to the actual sampling rate of the device and must be updated if the sampling rate changes.

3.8 Program the EVM Using the Configuration GUI in the HSDC Pro Software
1. Note that selecting the ‘TSW16DX370EVM’ in the ADC select drop-down menu made an additional ‘TSW16DX370EVM’ tab appear in HSDC Pro. Select the TSW16DX370EVM tab in the HSDC Pro software.
2. Navigate to the INTRO tab in the GUI
3. Press the ‘Program LMK04828’ button.
4. Verify that the ‘PLL LOCKED’ (D10) and ‘LMK LOCKED’ (D9) LEDs become lit on the EVM.
5. Press the ‘Calibrate ADC16DX370’ button.
6. Press the ‘Program LMX2581’ button.
7. Verify that the ‘LD’ LED, next to the LMX2581, becomes lit.
8. Press the ‘Program LMH6521’ button.
3.9 **Verify the TSW14J56EVM Switch Settings, Initialize the JESD204B Link (CPU_RESET), and Verify TSW14J56EVM Status LEDs**

1. Observe the switches and jumpers on the TSW14J56EVM and verify that they are in the correct position. The required switch settings are shown in Table 6.

2. Press the **CPU_RESET** button (SW7) on the TSW14J56EVM. This button is used to reset the JESD204B receiver core in the receiving FPGA and should be pressed after power up, after changing the test setup, or after changing particular device configuration registers.

3. Verify the status of the D1–D8 LEDs on the TSW14J56EVM. See the appendix for more information regarding the status LEDs.

<table>
<thead>
<tr>
<th>LED</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>N/A</td>
</tr>
<tr>
<td>D2</td>
<td>Blinking</td>
</tr>
<tr>
<td>D3</td>
<td>ON</td>
</tr>
<tr>
<td>D4</td>
<td>Blinking</td>
</tr>
<tr>
<td>D5</td>
<td>ON</td>
</tr>
<tr>
<td>D6</td>
<td>OFF</td>
</tr>
<tr>
<td>D7</td>
<td>OFF</td>
</tr>
<tr>
<td>D8</td>
<td>ON</td>
</tr>
<tr>
<td>FPGA_DONE</td>
<td>ON</td>
</tr>
</tbody>
</table>

3.10 **Turn the Signal Generator RF Outputs ON**

Turn on the RF signal outputs of the signal generators connector to RFINA.

3.11 **Capture Data Using the HSDP Software**

The following settings are made in the HSDC Pro window (Figure 3):

1. Verify that ‘TSW16DX370EVM’ is the selected device.

2. Verify the ‘ADC sampling rate (Fs)’ as ‘368.64M’. This value must be equal to the operating sampling rate of the device.

3. Select the Test to perform.

4. Select the data view.

5. Select the channel to view.

6. When viewing FFT results, verify that an appropriate windowing function such as ‘Blackman’ is selected.

7. Press the capture button to capture new data.

8. Additional Tips:

   • Use the ‘Notch Frequency Bins’ from the Test Options file menu to remove bins around DC (eliminate DC noise, offset) or the fundamental (eliminate phase noise from signal generators).

   • Open the ‘Capture Option’ dialog from the Data Capture Options file menu to change the capture depth or to enable FFT averaging.

   • For analyzing only a portion of the spectrum, use the ‘Single Tone’ Test with the ‘Bandwidth Integration Markers’ from the ‘Test Options’ file menu. The ‘Channel Power’ test may also be useful.

   • For analyzing only a subset of the captured data, set the ‘Analysis Window (samples)’ setting to a value less than the number total samples captured and move the green/red markers in the small transient data window at the top of the screen to select the data sub-set of interest.
3.12 **Re-Verify TSW14J56EVM Status LEDs**

Verify the status of the D1–D8 LEDs on the TSW14J56EVM. Note that D4 has changed to indicate that the JESD204B link is established. See the [appendix](#) for more information regarding the status LEDs.

<table>
<thead>
<tr>
<th>LED</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>N/A</td>
</tr>
<tr>
<td>D2</td>
<td>Blinking</td>
</tr>
<tr>
<td>D3</td>
<td>OFF</td>
</tr>
<tr>
<td>D4</td>
<td>Blinking</td>
</tr>
<tr>
<td>D5</td>
<td>ON</td>
</tr>
<tr>
<td>D6</td>
<td>OFF</td>
</tr>
<tr>
<td>D7</td>
<td>OFF</td>
</tr>
<tr>
<td>D8</td>
<td>ON</td>
</tr>
<tr>
<td>FPGA_DONE</td>
<td>ON</td>
</tr>
</tbody>
</table>
4 Device Configuration

The ADC device is programmable via the serial programming interface (SPI) bus accessible through the FTDI USB to SPI converter located on the EVM. A GUI is provided to write instructions on the bus and program the registers of the ADC device.

For more information about the registers of a particular device, see the device datasheet.

4.1 Supported JESD204B Features

The ADC device supports some configuration of the JESD204B interface. Due to limitations in the TSW14J56EVM firmware, all JESD204B link features of the ADC device are not supported. The following table describes the supported and non-supported features.

<table>
<thead>
<tr>
<th>JESD204B Feature</th>
<th>Supported by ADC16DX370 Device</th>
<th>Supported by TSW14J56</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of lanes per channel (L)</td>
<td>L = 1 or 2</td>
<td>L = 1 supported</td>
</tr>
<tr>
<td></td>
<td></td>
<td>L = 2 supported with special instructions for configuring HSDC Pro software</td>
</tr>
<tr>
<td>Number of Frames per Multiframe (K)</td>
<td>K = 9 to 32</td>
<td>K = 32 supported</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other K values not supported at this time.</td>
</tr>
<tr>
<td>Scrambling</td>
<td>Scrambling supported</td>
<td>Scrambling not supported at this time.</td>
</tr>
<tr>
<td>Test Patterns</td>
<td>PRBS7, PRBS15, PRBS23 supported D21.5, K28.5, ILA, Ramp patterns supported</td>
<td>ILA and RAMP supported</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PRBS7, PRBS15, PRBS23, D21.5, K28.5 not supported at this time.</td>
</tr>
<tr>
<td>Speed</td>
<td>Lane rates from 7.4 Gbps down to 1 Gbps</td>
<td>Lane rates from 7.4 Gbps (Fs = 370 MSPS) down to 1 Gbps (Fs = 170 MSPS).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The Fs parameter must be properly set in HSDC Pro.</td>
</tr>
</tbody>
</table>

4.2 Using the Device Configuration GUI

The Device Configuration GUI must be installed separately from the HSDC Pro installation, but the Configuration GUI automatically integrates into the HSDC Pro Software. If HSDC Pro is opened and the device is selected corresponding to a Configuration GUI that is already installed, then the Configuration GUI will automatically load as a selectable tab. If the Configuration GUI is opened before HSDC Pro, it will open as a standalone GUI.

Figure 4 and Figure 5 show the GUI open to the INTRO tab and ADC CORE tab, respectively. Tabs at the top of the panel organize the configuration into device and EVM features with user-friendly controls and a low-level tab for directly configuring the registers. The EVM has four (4) configurable devices, namely the ADC, LMH, LMX, and LMK. The Register Map for each device is provided in the respective device datasheet.
### Control

<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program LMK04828</td>
<td>Executes the ‘LMK04828_config2.cfg’ script</td>
</tr>
<tr>
<td>Calibrate ADC16DX370</td>
<td>Executes the ‘ADC16DX370_CalDIVCLK1.cfg’ script, running the calibration procedure required by the device</td>
</tr>
<tr>
<td>Program LMX2581</td>
<td>Executes the configuration script pointed to by the selection menu on the LMX2581 → MACRO_CONFIG tab</td>
</tr>
<tr>
<td>Program LMH6521</td>
<td>Enables both LMH6521 channels and sets the attenuation to 24 dB</td>
</tr>
<tr>
<td>Demo One-Push Setup</td>
<td>Executes the following series of configuration scripts:</td>
</tr>
<tr>
<td></td>
<td>LMK04828_configDemo.cfg</td>
</tr>
<tr>
<td></td>
<td>ADC16DX370_configDemo.cfg</td>
</tr>
<tr>
<td></td>
<td>LMX2581_configDemo.cfg</td>
</tr>
<tr>
<td></td>
<td>LMH6521_configDemo.cfg</td>
</tr>
</tbody>
</table>

---

**Figure 4. Configuration GUI INTRO Tab**

**EVM Configuration Procedure**

1. Press the ‘Program LMK04828’ button to the right to configure the LMK docking chip on the EVM or select a different configuration on the LMK04828 Tab. Pressing the ‘Program LMK04828’ button executes Configuration 2.
2. Pressing the ‘Calibrate ADC16DX370’ button to the right to calibrate the ADC. Use the ADC16DX370 tab to further configure this device.
3. Press the button to the right to configure the LO to output a default frequency value (3468 MHz) or configure the integrated LO frequency of the LMK0481 to the desired value on the LMX2581 Tab.
4. Press the ‘Program LMH6521’ button. This enables the DAC and sets the attenuation to 16 dB. Use the LMH6521 tab to further configure the DUS.

Note: Manually calibrating the ADC after power-up is not strictly required unless the sampling rate is changed or GAIN0 is changed after power-up.
Figure 5. Configuration GUI ADC CORE Tab

Figure 6. Configuration GUI JESD240B Tab
Figure 7. LMH6521 Tab

Figure 8. LMK04828 MACRO CONFIG Tab
<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
</table>
|  | **Used to set the ADC sampling rate to a value different than the default value**  
  ● Executes ‘LMK04828_config1.cfg’ script  
  ● LMK set in clock distribution mode  
  ● Reference signal must be applied to REFIN SMA between 100 MHz and 370 MHz ($F_{REFIN}$), +6 dBm  
  ● ADC clocked by LMK, Sampling rate = $F_{REFIN}$  
  ● No ADC SYSREF  
  ● Reference frequency sent to FPGA = $F_{REFIN}$ / 2  
  ● SYSREF frequency sent to FPGA = $F_{REFIN}$ / 32  
  ● LMX2581 OSCin reference frequency = $F_{REFIN}$  
  **NOTE:** This impacts the frequency plan and noise optimization of the LMX2581  
  ● EVM hardware must be changed to remove power to Y1 (Remove FB18) |
|  | **Used to set the default ADC sampling rate**  
  ● Appropriate configuration for default hardware  
  ● Executes ‘LMK04828_config2.cfg’ script  
  ● LMK PLL1 disabled, PLL2 with internal PLL enabled  
  ● LMK reference provided by Y1, 61.44 MHz  
  ● ADC clocked by LMK, Sampling rate = 368.64 MSPS  
  ● No ADC SYSREF  
  ● Reference frequency send to FPGA = 184.32 MHz  
  ● SYSREF frequency sent to FPGA = 11.52 MHz  
  ● LMX2581 OSCin reference frequency = 368.64 MHz |
|  | **Used for LMK04828 development**  
  ● Executes ‘LMK04828_config3.cfg’ script.  
  ● By default, this script is the same script as LMK04828_config2.cfg  
  ● Intended for editing |
Figure 9. LMK04828 PLL1 Config Tab

Figure 10. LMK04828 PLL2 Config Tab
Figure 11. LMK04828 SYSREF and SYNC Tab

Figure 12. LMK04828 Clock Outputs Tab
<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO Frequency Selection</td>
<td>• Executes the configuration script 'LMX2581_XXX.cfg' where XXX is the RF output frequency</td>
</tr>
<tr>
<td></td>
<td>• Requires OSCin reference frequency = 368.64 MHz which occurs for the default LMK04828 configuration</td>
</tr>
<tr>
<td></td>
<td>• CUSTOM script intended for editing and development</td>
</tr>
</tbody>
</table>

Figure 13. LMX2581 MACRO CONFIG Tab
Figure 14. LMX2581 PLL Config Tab
### 4.3 Low-Level Control

The Low-Level View tab, shown in Figure 15, allows configuration of the devices at the bit-field level. At any time, the following controls may be used to configure or read from the device:

<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
</table>
| Register Map Summary                         | Displays the devices on the EVM, registers for those devices, and the states of the registers  
  - Clicking on a register field allows individual bit manipulation in the Register Data Cluster  
  - The Value column shows the value of the register at the time the GUI was last updated  
  - The LR column shows the value of the register at the time the register was last read  |
| Write Register Button                        | Write to the register highlighted in the Register Map Summary with the value in the Write Data field                                                                                                                                                           |
| Write All Button                             | Update all registers shown in the Register Map Summary with the values shown in the Register Map Summary  
  - Can be used to re-synchronize the GUI with the state of the hardware  |
| Read Register Button                         | Read from the register highlighted in the Register Map Summary and display the results in the Read Data field                                                                                                                                               |
| Read All Button                              | Read from all registers in the Register Map Summary and display the current state of the hardware                                                                                                                                                     |
| Load Config Button                           | Load a Configuration File from disk and execute the commands in the file                                                                                                                                                                                      |
| Save Config Button                           | Save a Configuration File to disk that contains the current state of configuration                                                                                                                                                                         |
| Register Data Cluster                        | Manipulate individual accessible bits of the register highlighted in the Register Map Summary                                                                                                                                                               |
| Individual Register Cluster with Read/Write Register Buttons | Perform a generic read or write command to the device shown in the ‘Block’ drop-down box using the Address and Write Data information                                                                                       |

![Figure 15. Low-Level Register Control Tab](image-url)
5 Evaluation Troubleshooting

Table 3 provides troubleshooting procedures for several issues.

Table 3. Troubleshooting Procedures

<table>
<thead>
<tr>
<th>Issue</th>
<th>Troubleshoot</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Problem</td>
<td>Verify the test setup shown in Figure 2 and repeat the setup procedure as described in this document.</td>
</tr>
<tr>
<td></td>
<td>Check power supply to EVM and TSW14J56EVM. Verify that the power switches are in the ON position.</td>
</tr>
<tr>
<td></td>
<td>Check signal and clock connections to EVM.</td>
</tr>
<tr>
<td></td>
<td>Visually check the top and bottom layers of the board to verify that nothing looks discolored or damaged.</td>
</tr>
<tr>
<td></td>
<td>Check the connection of all boards together.</td>
</tr>
<tr>
<td></td>
<td>Try pressing the CPU_RESET button on the TSW14J56EVM.</td>
</tr>
<tr>
<td></td>
<td>Try power-cycling the external power supply to the EVM and re-program the LMK and ADC devices.</td>
</tr>
<tr>
<td>TSW14J56 LEDs are not correct</td>
<td>Verify the settings of the configuration switches on the TSW14J56EVM.</td>
</tr>
<tr>
<td></td>
<td>Verify that the EVM configuration GUI is communicating with the USB and that the configuration procedure has been followed.</td>
</tr>
<tr>
<td></td>
<td>(LEDs Not Blinking) Reprogram the LMK devices.</td>
</tr>
<tr>
<td></td>
<td>Try pressing the CPU_RESET button on the TSW14J56EVM.</td>
</tr>
<tr>
<td></td>
<td>Try capturing data in HSDC Pro to force an LED status update.</td>
</tr>
<tr>
<td>Configuration GUI is not working properly</td>
<td>Verify that the USB cable is plugged into the EVM and the PC.</td>
</tr>
<tr>
<td></td>
<td>Check the computer’s Device Manager and verify that a ‘USB Serial Device’ is recognized when the EVM is connected to the PC.</td>
</tr>
<tr>
<td></td>
<td>Verify that the green ‘USB Status’ LED light in the top right corner of the GUI is lit. If it is not lit, press ‘Reconnect FTDI’ button.</td>
</tr>
<tr>
<td></td>
<td>Try restarting the configuration GUI.</td>
</tr>
<tr>
<td>Configuration GUI is not able to connected to the EVM</td>
<td>Use the free FT_PROG software from FTDI Chip and verify that the on-board FTDI chip is programmed with a Product Description that reflects the name of the EVM.</td>
</tr>
<tr>
<td>HSDP Software is not capturing good data or analysis results are incorrect.</td>
<td>Verify that the TSW14J56EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDP software.</td>
</tr>
<tr>
<td></td>
<td>Check that the proper ADC device is selected.</td>
</tr>
<tr>
<td></td>
<td>Check that the analysis parameters are properly configured.</td>
</tr>
<tr>
<td>HSDP Software gives a Time-Out error when capturing data</td>
<td>Try to reprogram the LMK device and reset the JESD204 Link.</td>
</tr>
<tr>
<td></td>
<td>Verify that the ADC sampling rate is correctly set in the HSDP software.</td>
</tr>
<tr>
<td>Sub-Optimal Measured Performance</td>
<td>Try pressing the ‘Calibrate ADC’ button on the INTRO tab or repeating the configuration GUI procedure for programming the EVM.</td>
</tr>
<tr>
<td></td>
<td>Check that the spectral analysis parameters are properly configured.</td>
</tr>
<tr>
<td></td>
<td>Verify that bandpass filters are used in the clock and input signal paths and that low-noise signal sources are used.</td>
</tr>
</tbody>
</table>
A.1  **EVM Jumper Settings**
The TSW16DX370EVM has three different jumpers with the following functions.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Function</th>
<th>Default Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>TRF37B32 Low Power Mode Select</td>
<td>Short 1-2: Low Power Mode enabled</td>
</tr>
<tr>
<td>JP2</td>
<td>ADC16DX370 SPI Bus Level Translator Interface Voltage. Set to be consistent with the SDO output interface voltage of the ADC16DX370.</td>
<td>Short 1-2: 3.3V</td>
</tr>
<tr>
<td>JP3</td>
<td>LMX2581 Readback Routing</td>
<td>Short 1-2: Register readback routed to testpoint TP2</td>
</tr>
</tbody>
</table>

A.2  **TSW14J56EVM LED Bank and Switch Configuration**
The LEDs on the TSW14J56EVM indicate the status of the capture board as well as status of the JESD204B link. The LEDs have the following meaning:

<table>
<thead>
<tr>
<th>LED</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| FPGA_DONE | FPGA Programming  
ON: FPGA has been programmed  
OFF: FPGA has NOT been programmed or is being programmed |
| D1    | TX SYNC~  
ON: Synchronization being requested (code group synchronization phase of link initialization)  
OFF: Synchronization not requested (code group synchronization complete)  
Note: The status of this LED is only valid after attempting a data capture in HSDC Pro |
| D2    | TX Device Clock  
BLINKING: Device clock is being received from the LMK device on the EVM  
NOT BLINKING: Device clock not received |
| D3    | SYNC~  
ON: Synchronization being requested (code group synchronization phase of link initialization)  
OFF: Synchronization not requested (code group synchronization complete)  
Note: The status of this LED is only valid after attempting a data capture in HSDC Pro |
| D4    | RX Device Clock  
BLINKING: Device clock is being received from the LMK device on the EVM  
NOT BLINKING: Device clock not received |
| D5    | No Function |
| D6    | DDR3 Memory Calibration Done  
ON: Calibration not done  
OFF: Calibration done, normal operation |
| D7    | DDR3 Memory Calibration Success  
ON: Calibration not successful  
OFF: Calibration successful, normal operation |
| D8    | DDR3 Memory Calibration Fail  
ON: Calibration not failed, normal operation  
OFF: Calibration failed |
Table 6. Required State of Switches on the TSW14J56EVM

<table>
<thead>
<tr>
<th>Switch</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1[1]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW1[2]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW1[3]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW1[4]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW4[1]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW4[2]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW4[3]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW4[4]</td>
<td>OFF</td>
</tr>
<tr>
<td>SW8, MSEL0–MSEL4</td>
<td>All ON</td>
</tr>
<tr>
<td>TDI, TDO, TCK, TMS jumpers</td>
<td>All should be shorting pins 1-2</td>
</tr>
<tr>
<td>JP1 (Y1 PWR)</td>
<td>Short pins 1-2 (HI Setting)</td>
</tr>
<tr>
<td>J8 (USB PWR)</td>
<td>Short pins 1-2</td>
</tr>
<tr>
<td>JP9 (U8 ENB)</td>
<td>Short pins 2-3</td>
</tr>
</tbody>
</table>

A.3  **HSDC Pro Settings for Optional ADC16DX370 Configuration**

A.3.1  **Changing the Number of Serial Output Lanes (L)**

The ADC16DX370 outputs data on two lanes (one lane/channel) by default but the device may also be configured to output on four total lanes. This option is selected using the ‘L’ parameter on the JESD204B tab in the Configuration GUI. Changing the lane configuration from the default requires special HSDC Pro configuration. Contact TI for more information.

A.3.2  **Changing the Number of Frames per Multi-Frame (K)**

Changing the number of frames per multi-frame output by the JESD204 transmitted (ADC16DX370) is configured using the ‘K’ parameter on the JESD204B tab in the Configuration GUI. This parameter must be matched by the receiving device. Changing K from the default requires special HSDC Pro configuration. Contact TI for more information.

A.4  **Exercising the SYSREF Input of the ADC**

The SYSREF input is used to align the phase of the ADC’s internal local multi-frame clock (LMFC) according to the JESD204B interface specification but it is not required to establish a link and evaluate the analog performance of the ADC with this EVM. Upon power-up, the ADC assumes a default alignment for its LMFC and proceeds to synchronize with the receiving device without requiring a SYSREF input event.

A SYSREF signal may be applied to the ADC from the LMK04828 to validate the response of the ADC to a SYSREF event. The SYSREF signal path is AC coupled, therefore only periodic signals with frequencies larger than 5 MHz are supported. Note that continuously running an SYSREF signal to the ADC during normal operating will degrade the spurious performance of the ADC.
A.5 Customizing the EVM Frequency Plan

A.5.1 Signal Path Considerations

The signal path of the TSW16DX370EVM includes two separate LC bandpass filters (BPF). These filters, in conjunction with the LO frequency and the ADC sampling rate set the frequency plan of this design which is intended for a ~100-MHz channel bandwidth and 276.48-MHz intermediate frequency (IF).

The default bandpass filters restrict the signal path frequency plan, but they may be changed. The footprints provide optimal support for a 10-pole BPF with a standard architecture. An optimal re-design of the filters should include modeling of the PCB.

A.5.2 Configuring the LMK04828

By default, the LMK04828 is configured to use PLL2 with an internal VCO and a 61.44-MHz reference from Y1. This reference is multiplied to derive the ADC sampling clock, ADC SYSREF, FPGA reference, FPGA SYSREF, and LMX2581 reference.

The LMK04828 may optionally be configured as a clock distributor and divider. A reference signal may be applied to the REFIN input (~+6 dBm) which is then divided down or passed through to generate the necessary clocks. Basic support for this configuration is available using GUI controls. Script-based customization of this mode is possible using the configuration scripts also supported by the GUI. Hardware changes are required to turn off the Y1 reference by removing FB18.

A.5.3 Configuring the LMX2581

By default, the LMX2581 can be configured to support a wide range of LO frequencies using the configuration GUI. Configuration may be performed with the MACRO configurations, CUSTOM script, or the controls present on the more detailed tabs. Care must be taken to consider the OSCin reference frequency coming from the LMK04828.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (March 2015) to B Revision

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Removed +5-V power supply from kit and replaced with flying lead power cable.</td>
<td>4</td>
</tr>
<tr>
<td>In the Setup Procedure section, changed the EVM Test Setup image and the Connect the Power Supplies to the Boards section.</td>
<td>5</td>
</tr>
</tbody>
</table>
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3.1.1 **Notice applicable to EVMs not FCC-Approved:**

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3.1.2 **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:**

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.
FCC Interference Statement for Class B EVM devices

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:
(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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http://www.tij.co.jp/sds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan.
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.
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西新宿三井ビル

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4.3.1 User shall operate the EVM within TI’s recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
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