EVM User's Guide: DAC81401EVM

DAC81401 Evaluation Module

Description

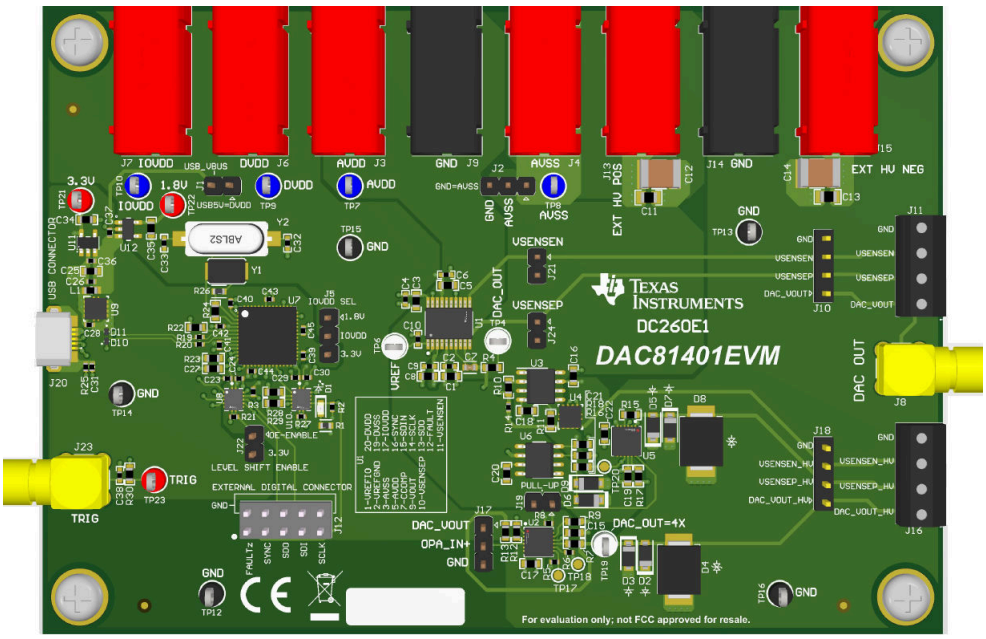
The 16-bit DAC81401 and 12-bit DAC61401 (DACx1401) are a pin-compatible family of single-channel, buffered, high-voltage-output digital to-analog converters (DACs) with an integrated 2.5-V internal reference. These devices are specified monotonic and provide exceptional linearity of less than 1 LSB.

Get Started

1. Order the EVM.
2. Configure EVM jumpers.
3. Install DAC814xxEVM GUI from ti.com.
4. Connect USB and external power supplies.
5. Launch DAC814xxEVM GUI.

Features

- Configurable circuit to evaluate DAC
- Onboard VDD and IOVDD (1.8-V or 3.3-V) support
- High-voltage 4× gain stage is available to support up to an 80-V output
- Output protection circuit on gain output stage
- Trigger output is available for synchronous measurement
- FT4232 used to easily write to DAC using DAC814xxEVM GUI
- External SPI connections available



1 Evaluation Module Overview

1.1 Introduction

The DACx1401 devices offer bipolar output voltages of ±20 V, ±10 V, ±5 V, and full-scale unipolar output voltages of 40 V, 10 V and 5 V. The DAC output range is programmable.

This user's guide describes the characteristics, operation, and recommended use cases of the DAC81401EVM. This document provides examples and instructions on how to use the DAC81401EVM board and included software. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the DAC81401EVM. This document also includes a schematic, reference printed circuit board (PCB) layouts, and a complete bill of materials (BOM).

1.2 Kit Contents

Table 1-1 details the contents of the EVM kit. Contact the TI Product Information Center at (972) 644-5580 if any component is missing. Download the latest versions of the related software on the TI website, www.ti.com.

Table 1-1. DAC81401EVM Kit Contents

Item	Quantity
DAC81401EVM	1
USB-A to Micro-USB Cable	1

1.3 Specification

Figure 1-1 shows the block diagram of the DAC81401EVM board. By default, the DAC81401EVM connects to a local machine USB port through a USB-A to Micro-USB cable.

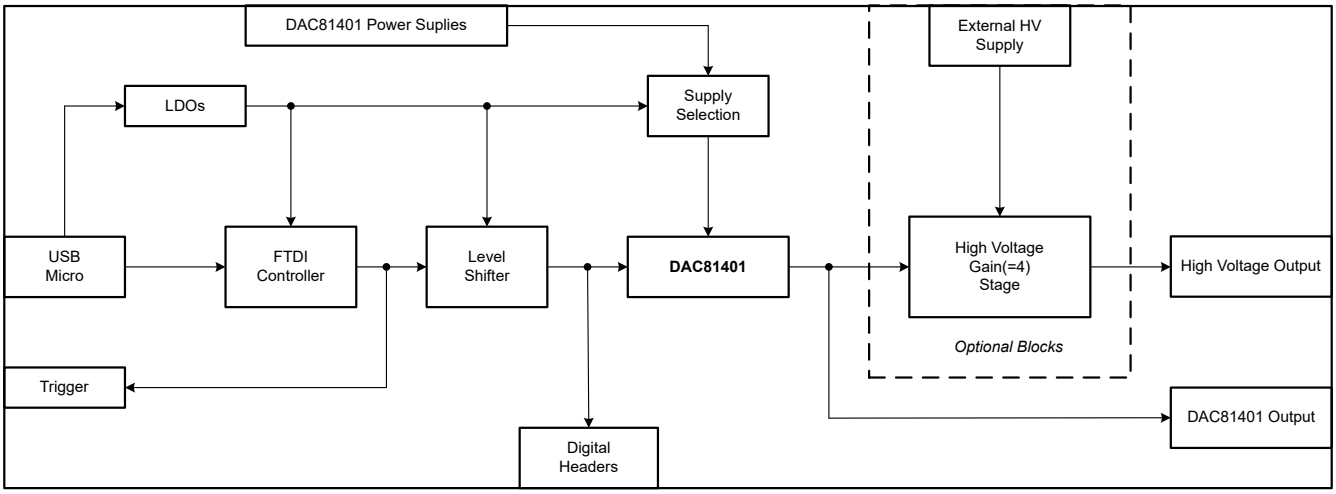


Figure 1-1. DAC81401EVM Functional Block Diagram

The USB provides the 5 V default DVDD supply to the DAC81401. Voltage regulators generates 3.3 V and 1.8 V from USB 5 V supply. These 3.3 V and 1.8 V supplies are used to power the FTDI controller, level shifter and IOVDD of DAC81401. IOVDD can be 3.3-V or 1.8-V depending on the jumper J5 setting. DVDD and IOVDD device supply inputs for the DAC81401 can be externally supplied through J7 and J6 banana jacks respectively, with proper settings of jumpers J1 and J5. DAC81401 AVDD and AVSS (can be GND through jumper J2) needs external power supply connection through J3 and J4 banana jacks respectively.

Optional *High voltage gain stage* needs separate power supply through J13 and J15 banana jacks. This high voltage stage provides 4 times gained DAC81401 output voltage, up to 0-80 V or ± 40-V. Attenuated output voltage by 4, is used on the VSENSEP to close the loop properly on DAC81401 side.

1.4 Device Information

The documents in Table 1-2 provide information regarding Texas Instruments integrated circuits used in the assembly of the DAC81401EVM. This user's guide is available from the TI web site under literature number SLAU905. Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions are available from the TI web site at www.ti.com, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

Table 1-2. Related Device Documentation

Document	Literature Number
DAC81401 product data sheet	SLAU905
OPA593 product data sheet	SBOS659
OPA189 product data sheet	OPA189

2 Software

2.1 GUI Installation

This section provides the procedure for EVM software installation.

The EVM software is compatible with the Windows® 10 operating system. Before installing the software, make sure that the DAC80401EVM is not connected to the local machine.

Download the latest version of the EVM graphical user interface (GUI) installer from the *Order and start development* subsection of the DAC81401EVM tool folder on TI.com. Run the GUI installer to install the DAC81401EVM GUI software on your local machine.

When the DAC804xxEVM GUI is launched, an installation dialog window opens and prompts the user to select an installation directory. If left unchanged, Figure 2-1 shows that the software location defaults to *C:\Program Files (x86)\Texas Instruments\DAC814xxEVM.*

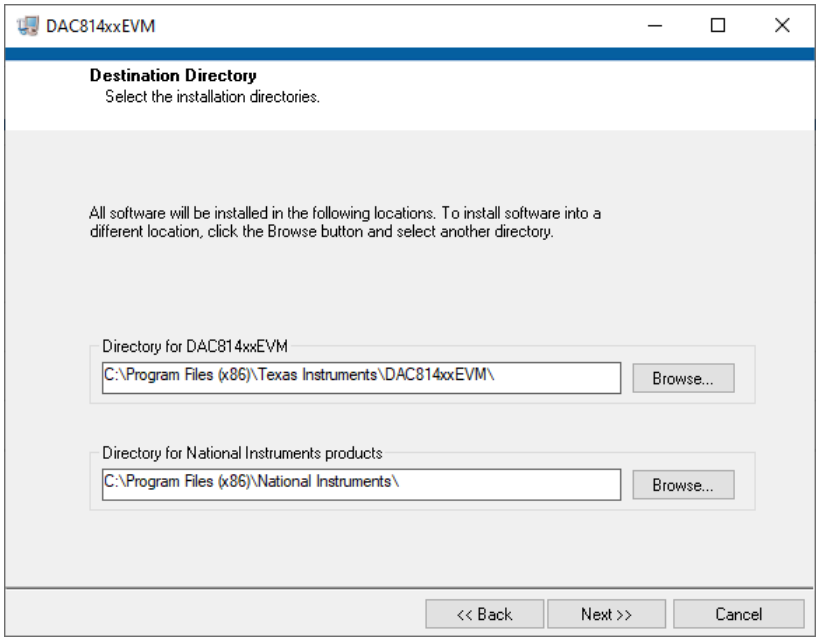


Figure 2-1. Software Installation Path

The EVM software also installs the Future Technology Devices International Limited (FTDI) USB drivers using a separate executable file. Figure 2-2 shows the FTDI USB drivers installation window that is automatically launched after the DAC814xxEVM software installation is complete.

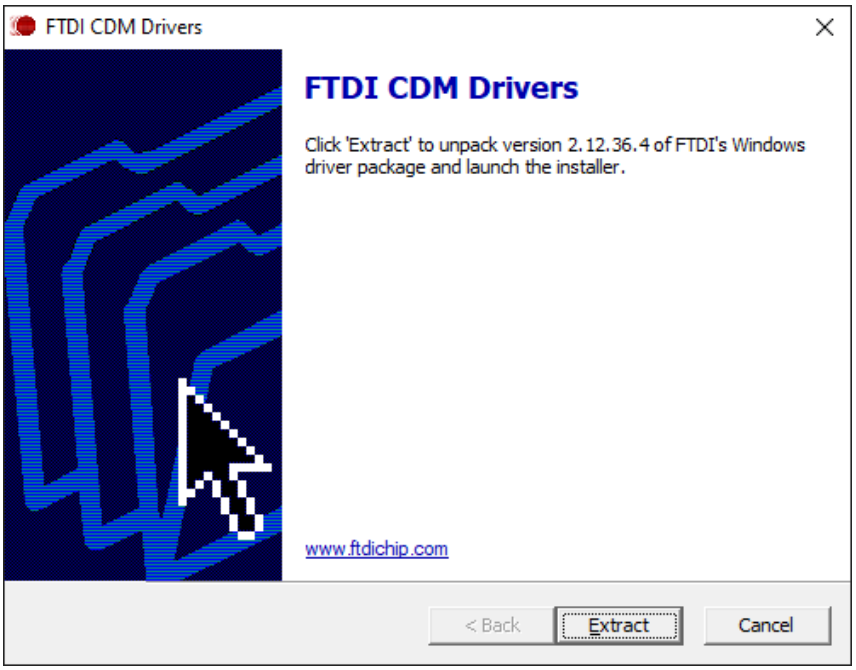


Figure 2-2. FTDI USB Drivers

2.2 Software Description

To launch the software, locate the *DAC814xxEVM* folder in the *Start Menu*, and select the *DAC814xxEVM* icon as shown in Figure 2-3.

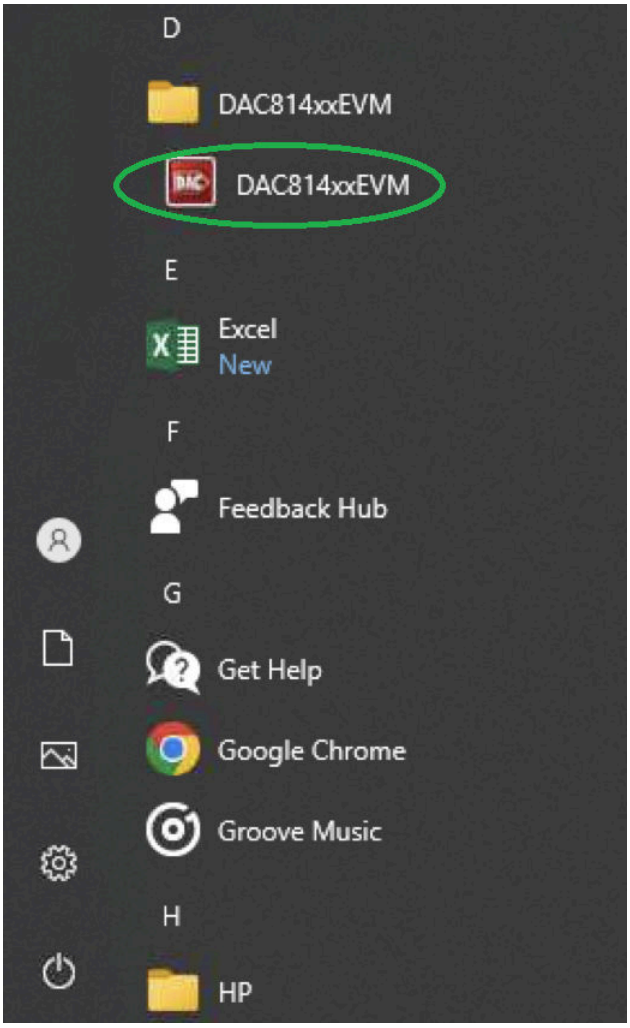


Figure 2-3. DAC814xxEVM Software Installation in Start Menu

Figure 2-4 shows that if the onboard FTDI controller is connected correctly, then the status bar at the bottom of the screen displays *CONNECTED*. If the controller is not properly connected or not connected at all, then the status displays *DEMO*. If the graphical user interface (GUI) does not display the *CONNECTED* status while the EVM is connected, then unplug and reconnect the EVM and relaunch the GUI software.

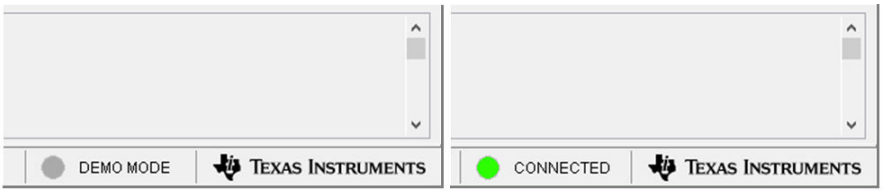


Figure 2-4. DAC814xxEVM GUI Connection Detection

DAC81401 High Level page provides quick access to basic DAC81401 functionality as shown in Figure 2-5.

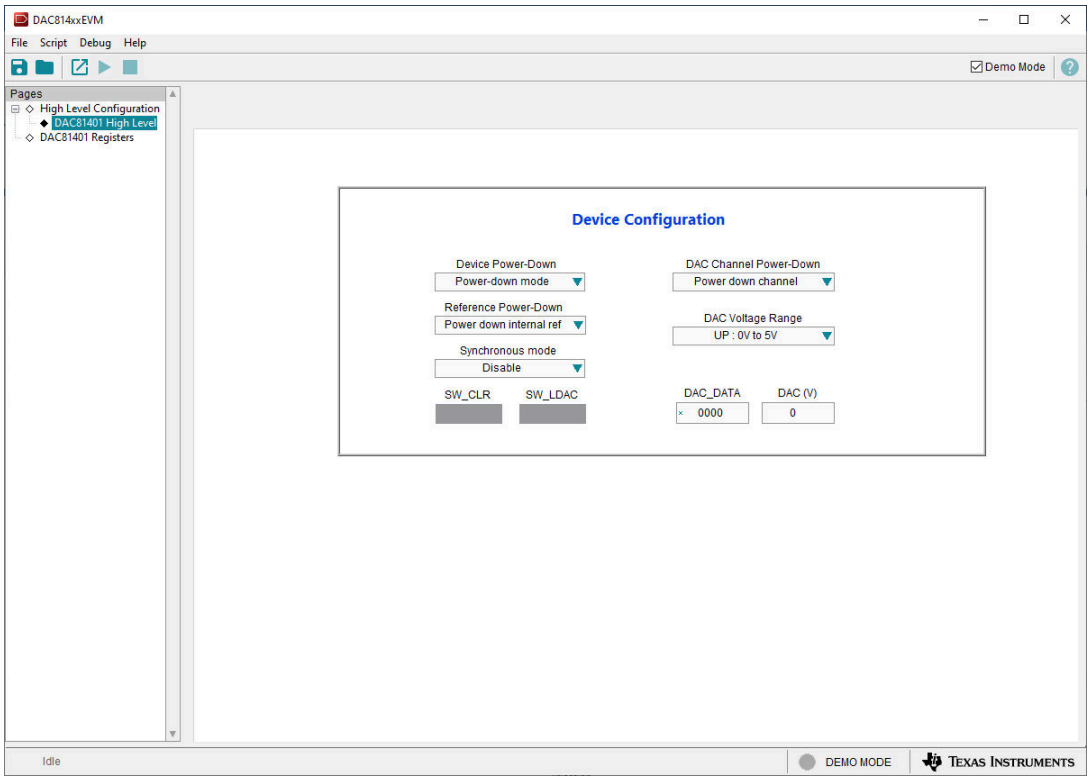


Figure 2-5. DAC81401EVM High Level Page

The *DAC81401 Registers* page, shown in Figure 2-6, allows the user to access low-level communication directly with the DAC81401 registers. Selecting a register on the Register Map list shows a description of the values in that register, as well as information on the register address, default value, size, and current value. Values are read from and written to the registers by writing to the Value or bit field of the GUI.

The *Register Map* page also provides the FTDI GPIO controls for DAC81401EVM. For example, OPE_EN, TRIG and $\overline{\text{FAULT}}$ pins, under the FTDI section.

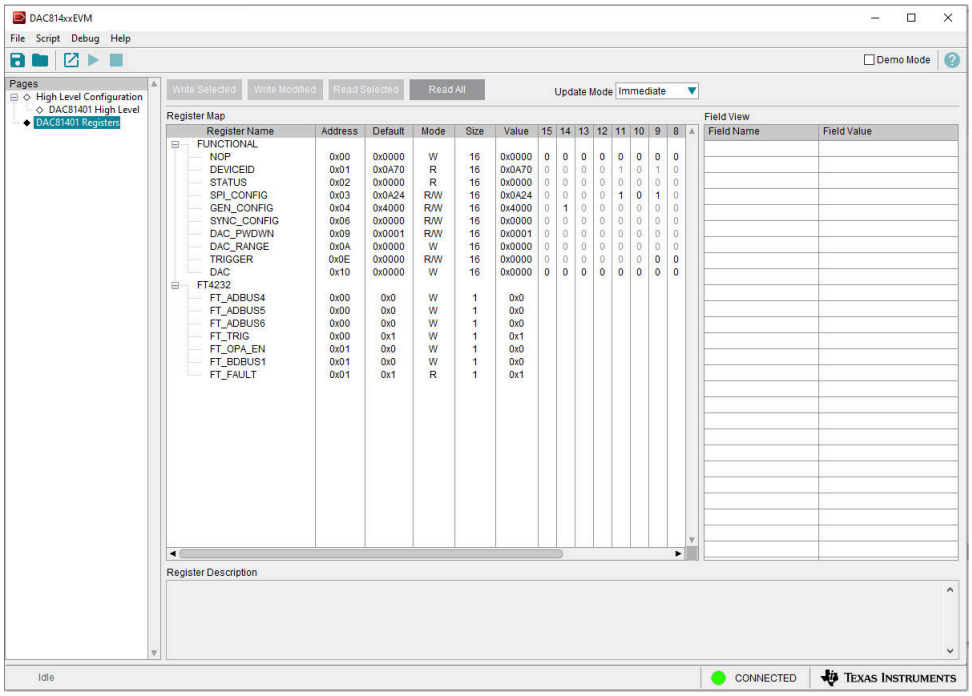


Figure 2-6. DAC81401EVM Registers Page

To store the values of the register map locally, select *Save Configuration* under the *File* menu option. The stored configuration files can be recalled and loaded by selecting *Open Configuration* as shown in Figure 2-7.

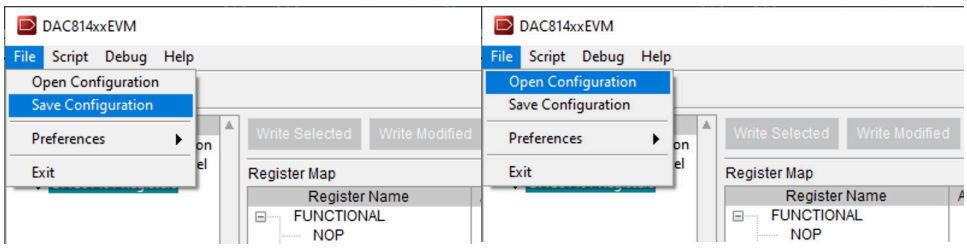


Figure 2-7. DAC81401EVM Save/Open Configuration

3 Hardware

3.1 Power Requirements

The USB connection at J12 provides 5 V to the EVM. This connection is necessary if using the DAC814xxEVM GUI, as the communication is done through the USB port and the FT4232 is powered by one of the LDOs on the board. On board supplies for DVDD (5-V USB supply through J1) and IOVDD (LDO generated 1.8-V or 3.3-V through J5) are also available. DVDD and IOVDD power supply of DAC81401 can be provided externally through J5 and J7 respectively. AVDD and AVSS power supply of DAC81401 need to connected externally through J3 and J4 respectively. AVSS can be connected to GND through J2. Optional *EXT HV POS* (V+) and *EXT HV NEG* (V-) supplies are needed for OPA593 (U2, U5) while using the *high-voltage gain stage*.

- AVDD : 0 to 41.5 V (default + 15 V)
- AVSS : 0 to -21.5 V (default - 15 V)
- DVDD : 4.5 V to 5.5 V (default + 5 V)
- IOVDD : 1.7 V to 5.5 V (default + 3.3 V)
- (AVDD - AVSS) must not be greater than 43 V
- EXT HV POS (V+) - EXT HV NEG : ± 4 V to ±42.5 V or 8 V to 85 V (default ± 25 V)

Table 3-1 summarizes the external power connections.

Table 3-1. DAC81401EVM Power Supply Inputs

Terminal	Name	Function
J3	AVDD	Positive supply voltage for the DAC81401 output buffers
J4	AVSS	Negative supply voltage for DAC81401 output buffers
J5	DVDD	Digital and analog supply voltage for the DAC81401
J7	IOVDD	IO supply voltage for setting the digital I/O operating voltage for the DAC81401
J9	GND	Ground connection
J13	EXT HV POS	Optional positive supply for high voltage gain stage operational amplifier
J14	GND	Ground connection
J15	EXT HV NEG	Optional negative supply for high voltage gain stage operational amplifier

3.2 Jumper Information

The jumpers must be connected properly to operate the DAC81401EVM for it's intended operation. Table 3-2 provides the details of the configurable jumper settings on the EVM. Figure 3-1 and Figure 3-2 shows the default jumper connections on the board with *High-voltage gain stage* enabled and *High-voltage gain stage* disabled respectively.

Table 3-2. DAC81401EVM Jumper Summary

Header	Name	Function
J1	DVDD=USB5V	**Short 1-2** – DVDD = 5 V supplied through USB power (default) **Open** – DVDD supplied through J6
J2	AVSS SEL	**Short 1-2** – AVSS supplied through J3 **Short 2-3** – AVSS connected to board GND (default) **Open** – AVSS supply pin is floating (not recommended)
J5	IOVDD SEL	**Short 1-2** – IOVDD = 1.8V supplied through LDO (U12) output **Short 2-3** – IOVDD = 3.3V supplied through LDO (U11) output (default) **Open** – IOVDD = 1.8V supplied through J7
J10	DAC CHANNEL TP	**Short 1-2** – DAC81401 VOUT is connected to VSENSEP pin (default) **Short 3-4** – DAC81401 VSENSEN pin connected to GND (default) **Open(1-2 and 3-4)** – VOUT, VSENSEP and VSENSEN pins of the DAC81401 are floating (not recommended)
J17	VOUT-GND SEL	**Short 1-2** – OPA593 +IN (U2)connected to DAC81401 output **Short 2-3** – OPA593 +IN (U2) connected to GND (default) **Open** – OPA593 +IN (U2) pin is floating (not recommended)
J18	DAC CHANNEL TP	**Short 1-2** – OPA593 OUT (U2) connected to OPA593 +IN (U5) pin **Short 3-4** – DAC81401 VSENSEN pin connected to GND **Open(1-2 and 3-4)** – High voltage gain stage is not connected to DAC81401 (default)
J19	PULL-UP	**Short 1-2** – pulled down to GND and OPA593 (U2,U5) is in power down mode **Open** – OPA_EN = 1 bit : OPA593 (U2,U5) is in active mode and OPA_EN bit = 0: OPA593 (U2,U5) is in active mode (default)
J21	VSENSEN	**Short 1-2** – VSENSEN of high voltage gain stage is connected to DAC81401 VSENSEN pin **Open** – VSENSEN of high voltage gain stage is open (default)
J24	VSENSEP	**Short 1-2** – VSENSEP of high voltage gain stage is connected to DAC81401 VSENSEP pin **Open** – VSENSEP of high voltage gain stage is open (default)
J22	LEVEL SHIFT ENABLE	**Short 1-2** – Digital buffers (U8,U10) enabled **Open** – Digital buffers (U8,U10) disabled

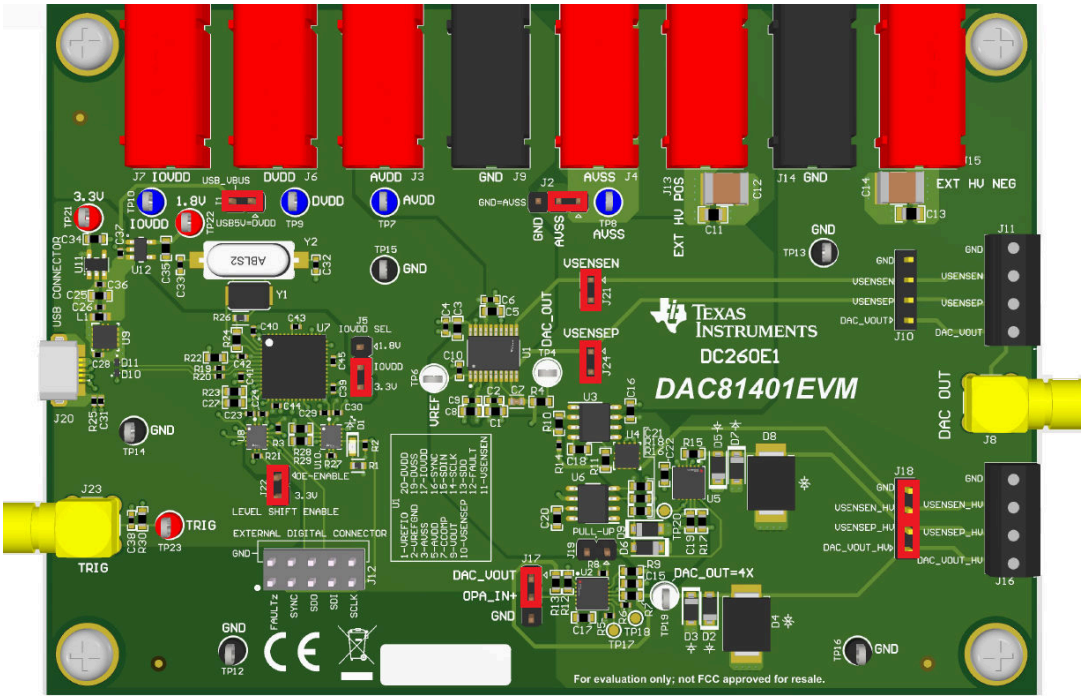


Figure 3-1. Default Header Settings with High Voltage Gain Stage Enabled

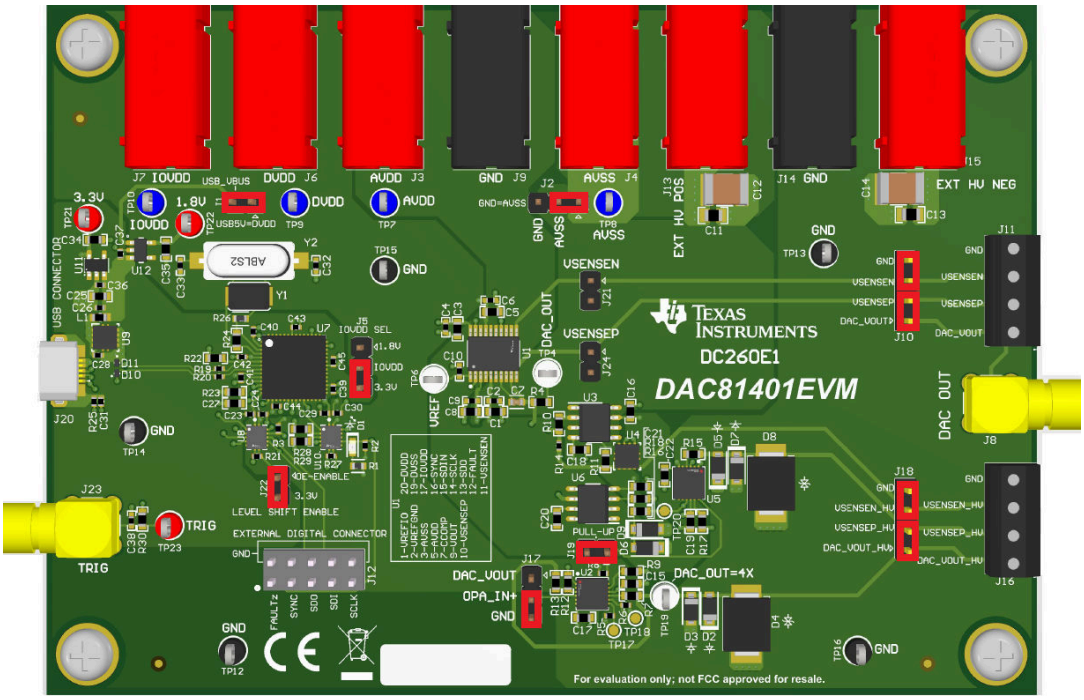


Figure 3-2. Default Header Settings with High Voltage Gain Stage Disabled

3.3 Setup

After the power and jumper configurations are set up per Figure 3-1 or Figure 3-2 , and the DAC814xxEVM GUI is fully installed, connect the USB cable from the DAC81401EVM USB port to the local machine. Figure 3-3 displays the system hardware setup.

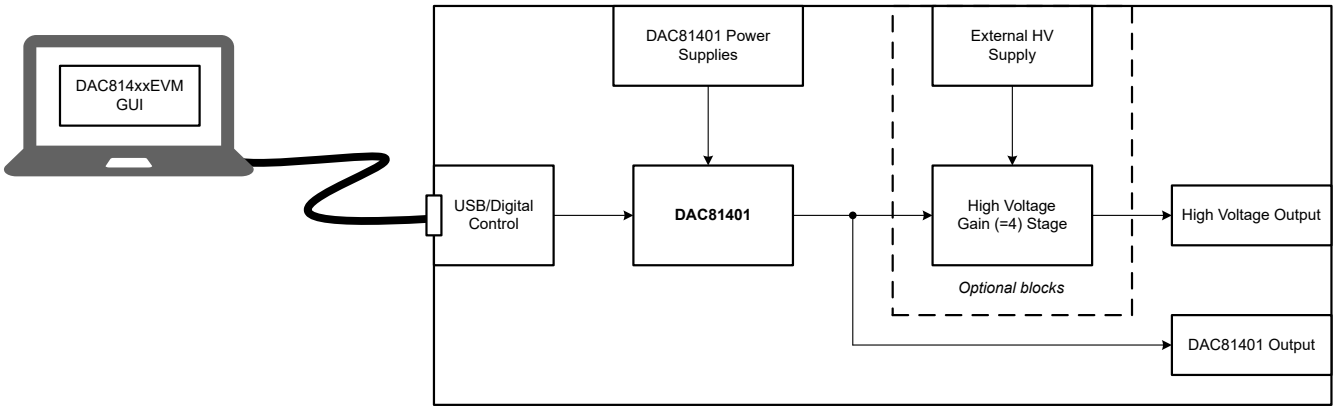


Figure 3-3. DAC81401EVM Hardware Setup

Once all the connection is done, power up the DAC81401EVM hardware as described in the power requirement section 3-1.

For basic DAC81401 device check, use one of the following sequences in the DAC814xxEVM GUI:

- **From *DAC81401 Register* page**
  - Write 0x0A24 to the SPI_CONFIG (0x03) register to power up the device
  - Write 0x0000 to the GEN_CONFIG (0x04) register to power up the internal reference
  - Write 0x0000 to the DAC_PWDWN (0x09) register to power up the DAC output
  - Write 0x7FFF to the DAC (0x10) register to configure the DAC_OUT to 2.5-V on DAC_OUT (TP4) or 10 V on TP18 (pin-1) while high voltage gain stage is active
- **From *DAC81401 High Level* page**
  - Device Power Down: select *Active mode* to power up the device
  - Reference Power-Down: select *Activate internal ref* to power up the internal reference
  - DAC Channel Power-Down: select *Activate channel* to power up the DAC output
  - DAC_DATA: write 0x7FFF to get 2.5-V on DAC_OUT (TP4) or 10 V on TP18 (pin-1) while high voltage gain stage is active

The default voltage range for the DAC81401 is 0 V to 5 V. Configure the voltage range by modifying the "DAC Voltage Range" control on DAC814xxEVM GUI High Level page, or by writing to the "DAC_RANGE" register in the Low Level page as shown in section 2-2.

3.4 Header Information

The EVM provides access to the DAC81401 digital pins through header J12. Table 3-3 lists the J12 pin definitions.

Table 3-3. DAC81401EVM Header J12 Pin Definitions

Pin Number	Signal	Description
1	$\overline{\text{FAULT}}$	DAC81401 $\overline{\text{FAULT}}$ output
3	SYNC	DAC81401 chip-select input
5	SDO	DAC81401 serial data output
7	SDI	DAC81401 serial data input
9	SCLK	Serial-clock input
2,4,6,8,10	GND	Ground

The pins on J12 can be used to externally control the DAC81401 with SPI commands if the FTDI controller is disconnected from the DAC, by opening the J22 jumper.

3.5 Test Points

The DAC81401EVM has a variety of test points available for measuring and debugging purposes. Table 3-4 explains the purpose of each test point.

Table 3-4. DAC81401EVM Test Points

Test Point	Net	Description
TP4	DAC_VOUT	DAC81401 output
TP6	VREF	DAC81401 reference voltage
TP7	AVDD	DAC8140 1 AVDD
TP8	AVSS	DAC81401 AVSS
TP9	DVDD	DAC81401 DVDD
TP10	IOVDD	DAC81401 IOVDD
TP12,TP13,TP14,TP16,TP16	GND	Ground connection
TP17	Current flag (U2)	Current flag output of OPA593 (U2)
TP18	Thermal flag (U2)	Thermal flag output of OPA593 (U2)
TP19	DAC_OUT = 4×	High voltage gain BY 4× output for DAC81401 DAC_OUT
TP20	DAC VSENSEP HV	Attenuated by 4X output for DAC81401 VSENSEP
TP21	3P3V	3.3-V LDO output
TP22	1P8V	1.8-V LDO output
TP23	TRIG	FTDI trigger pin

4 Hardware Design Files

4.1 Schematics

Figure 4-1 through Figure 4-4 shows the DAC81401EVM schematic. Components not populated on the DAC81401EVM board are marked with red cross and "DNI*" text.

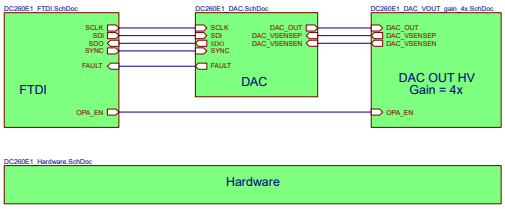


Figure 4-1. DAC81401EVM Schematic : Top Level Blocks

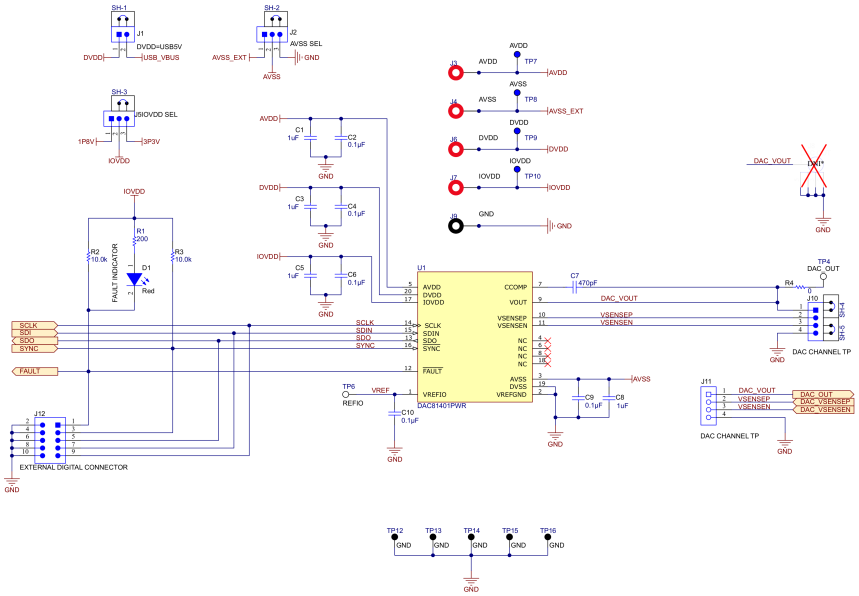


Figure 4-2. DAC81401EVM Schematic : DAC81401 Interface

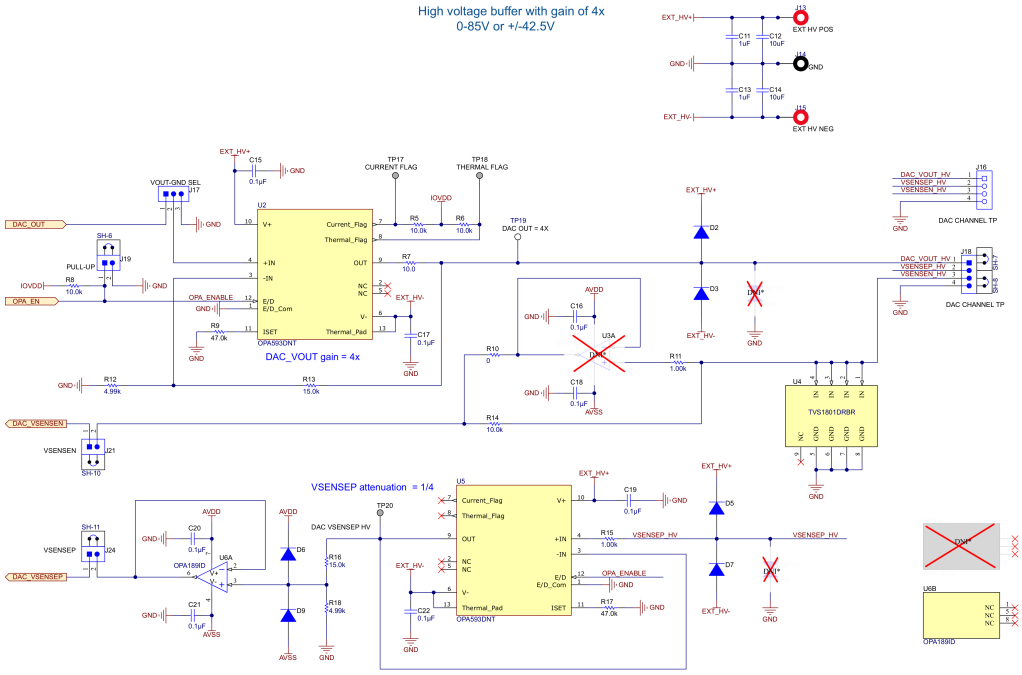


Figure 4-3. DAC81401EVM Schematic : High Voltage Gain Stage

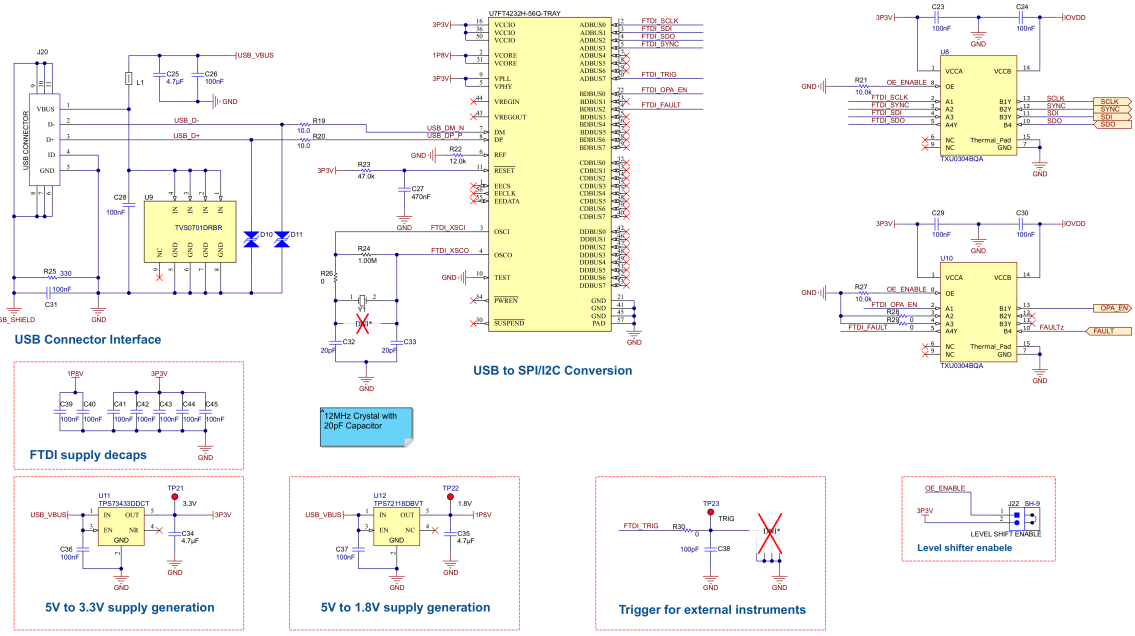


Figure 4-4. DAC81401EVM Schematic : FTDI Controller Interface

4.2 PCB Layouts

Figure 4-5 through Figure 4-8 show the board layout for the DAC81401EVM.

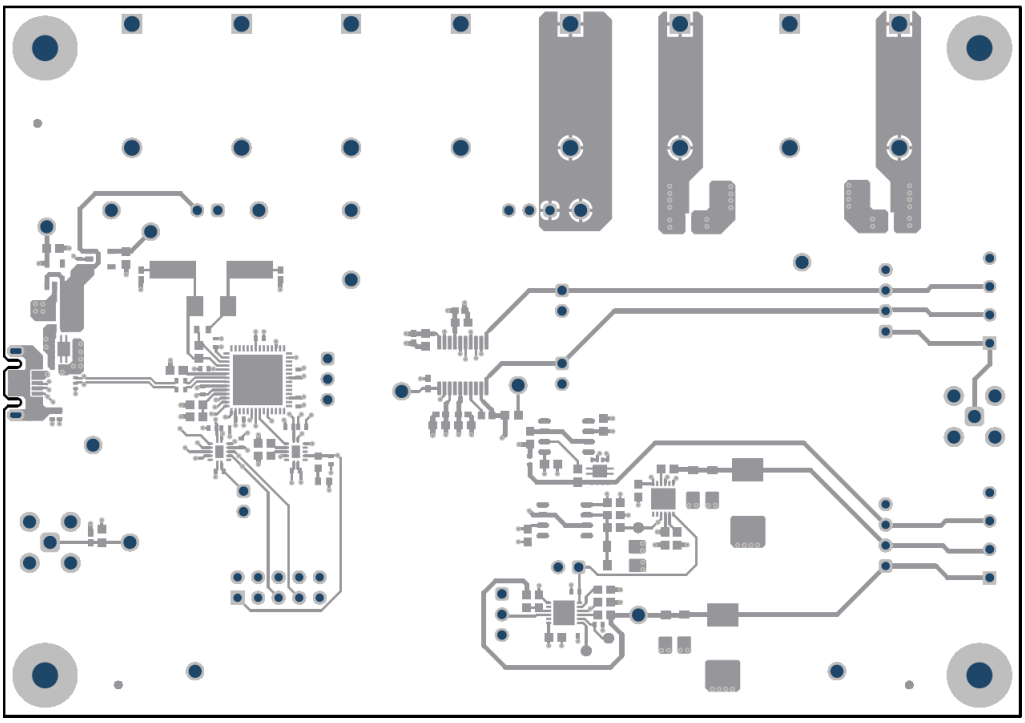


Figure 4-5. DAC81401EVM PCB Top Layer Layout

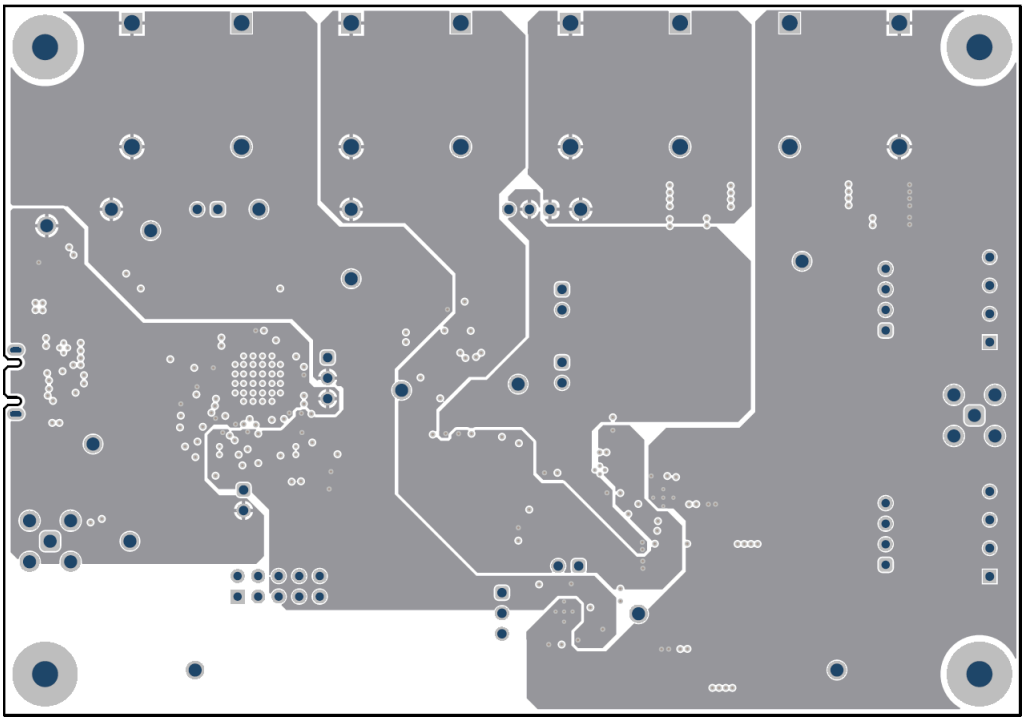


Figure 4-6. DAC81401EVM PCB Mid Layer 1 Layout

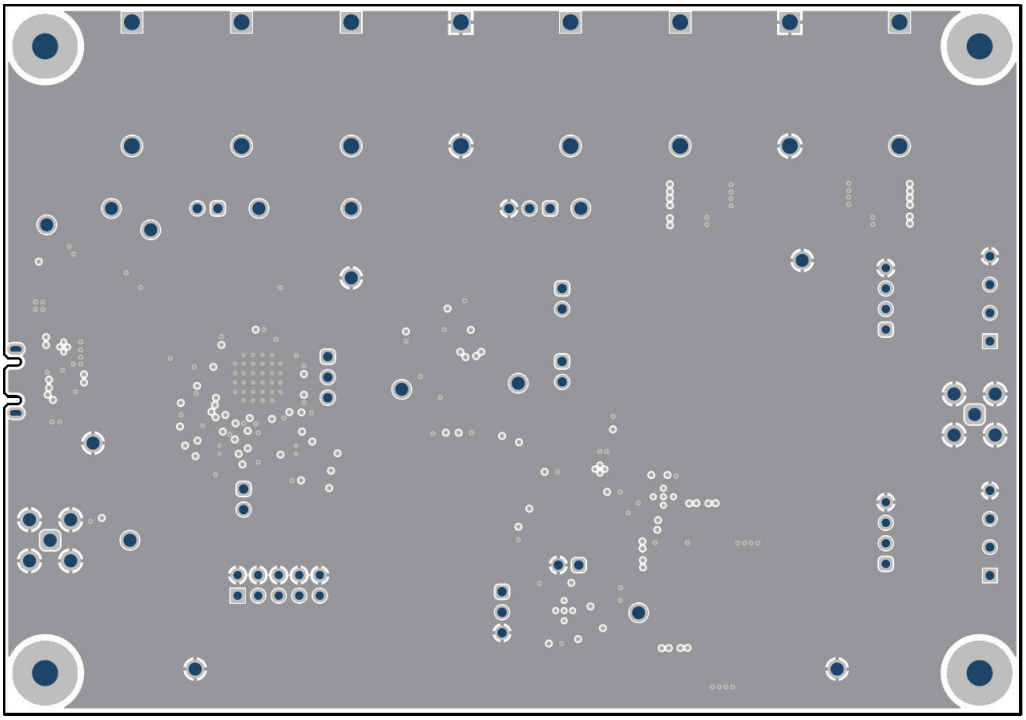


Figure 4-7. DAC81401EVM PCB Mid Layer 2 Layout

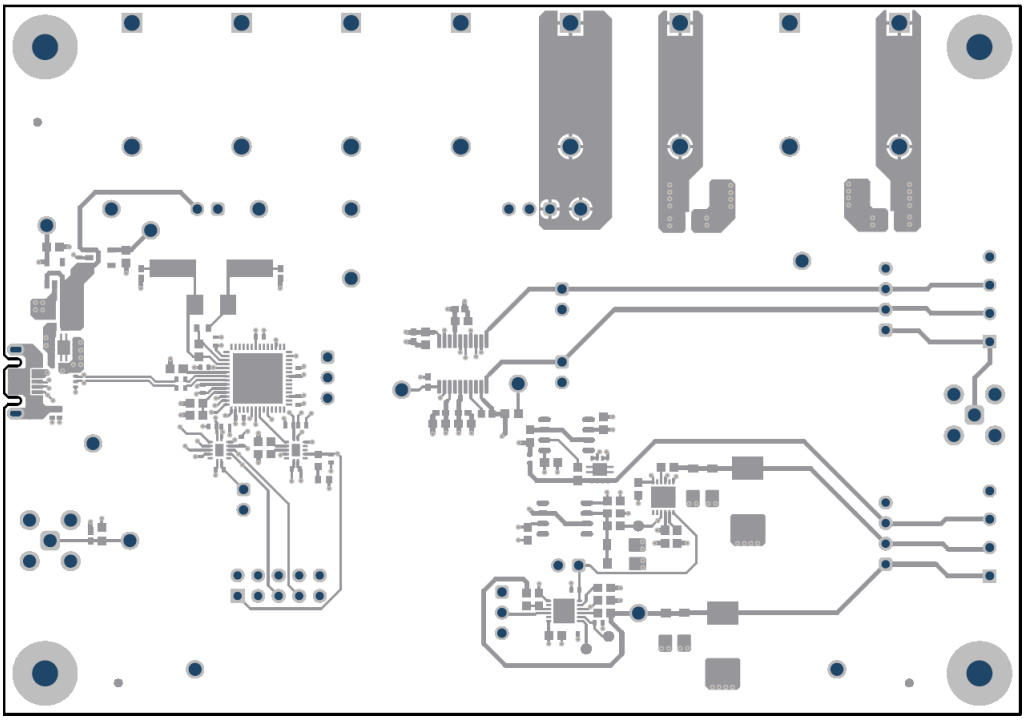


Figure 4-8. DAC81401EVM PCB Bottom Layer Layout

4.3 Bill of Materials (BOM)

Table 4-1 lists the DAC81401EVM bill of materials (BOM).

Table 4-1. Bill of Materials for the DAC81401EVM

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Assembly Details
C1,C3,C5,C8	4	1 µF	CAP, CERM, 1 uF, 50 V, +/- 10%, X5R, 0603	0603	885012206126	Wurth Elektronik	Installed
C2, C4, C6, C9, C10	5	0.1 µF	CAP, CERM, 0.1 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	885012205086	Wurth Elektronik	Installed
C7	1	470 pF	Cap Ceramic 470 pF 50 V C0G 1% SMD 0603 125°C Paper T/R	0603	885012006061	Wurth Elektronik	Installed
C11,C13	2	1 µF	CAP, CERM, 1 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	0805_HV	CGA4J3X7S2A105K125AB	TDK	Installed
C12,C14	2	10 µF	CAP, CERM, 10 uF, 100 V,+/- 20%, X7S, AEC-Q200 Grade 1, 1812	CKG45N_500	CKG45NX7S2A106M500JJ	TDK	Installed
C15, C16, C17, C18, C19, C20, C21, C22	8	0.1 µF	CAP, CERM, 0.1 µF, 100 V,+/- 10%, X8L, AEC-Q200 Grade 0, 0603	0603	885012206120	Wurth Elektronik	Installed
C23, C24, C26, C28, C29, C30, C31, C36, C37, C39, C40, C41, C42, C43, C44, C45	16	0.1 µF	CAP, CERM, 0.1 µF, 25 V,+/- 10%, X7R, 0402	0402S	885012205085	Wurth Elektronik	Installed
C25	1	4.7 µF	CAP, CERM, 4.7 uF, 10 V, +/- 20%, X7R, 0603	0603	GRM188Z71A475ME15D	MuRata	Installed
C27	1	0.47 µF	CAP, CERM, 0.47 uF, 25 V, +/- 10%, X7R, 0603	0603	885012206075	Wurth Elektronik	Installed
C32,C33	2	20 pF	CAP, CERM, 20 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H200JA01D	MuRata	Installed
C34,C35	2	4.7 µF	CAP, CERM, 4.7 uF, 16 V,+/- 10%, X7R, 0603	0603	GRM188Z71C475KE21D	MuRata	Installed
C38	1	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	885012005061	Wurth Elektronik	Installed
D1	1	Red	LED, Red, SMD	LTST-C191_Red	LTST-C191KRKT	Lite-On	Installed
D2,D3,D5,D6,D7,D9	6		Diode, Switching, 100 V, 0.15 A, SOD-123	DOS-123	1N4148W-TP	Micro Commercial Components	Installed
D10,D11	2		1-Channel ESD Protection Diode for USB Type-C and Thunderbolt 3, DPY0002A (X1SON-2)	DPY0002A	TPD1E01B04DPYR	Texas Instruments	Installed
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	Fiducial10-20	N/A	N/A	Installed

Table 4-1. Bill of Materials for the DAC81401EVM (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Assembly Details
H1,H2,H3,H4	4		MACHINE SCREW PAN PHILLIPS 4-40	NY PMS 440 0025 PH	NY PMS 440 0025 PH	B&F Fastener Supply	Installed
H5,H6,H7,H8	4		HEX STANDOFF #4-40 NYLON 1/2"	Keystone_1902C	1902C	Keystone	Installed
J1,J19,J21,J22,J24	5		Header, 2.54 mm, 2×1, Gold, TH	WURTH_61300211121	61300211121	Wurth Elektronik	Installed
J2,J5,J17	3		Header, 2.54 mm, 3×1, Gold, TH	WURTH_61300311121	61300311121	Wurth Elektronik	Installed
J3,J4,J6,J7,J13,J15	6		Standard Banana Jack, insulated, 10 A, red	571-0500	571-0500	DEM Manufacturing	Installed
J9,J14	2		Standard Banana Jack, insulated, 10 A, black	571-0100	571-0100	DEM Manufacturing	Installed
J10,J18	2		Header, 100mil, 4×1, Gold, TH	TSW-104-07-G-S	61300411121	Wurth Elektronik	Installed
J11,J16	2		Terminal Block, 3.5mm Pitch, 4×1, TH	TERM_BLK_ED555-4DS	ED555/4DS	On Shore Technology Inc.	Installed
J12	1		Header, 100mil, 5×2, Tin, TH	CONN_PEC05DAAN	61301021121	Wurth Elektronik	Installed
J20	1		Receptacle, USB 2.0, Micro B, 5 Position, R/A, SMT	Molex_1051640001	1051640001	Molex	Installed
L1	1	600 ohm	Ferrite Bead, 600 ohm @ 100 MHz, 1 A, 0603	0603S	782633601	Wurth Elektronik	Installed
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Label_650x200	THT-14-423-10	Brady	Installed
R1	1	200.0	200 Ohms ±1% 0.125W, 1/8W Chip Resistor 0603 (1608 Metric) Anti-Sulfur, Moisture Resistant Thin Film	FP-RNCP0603FTD200R_0603-MFG	RNCP0603FTD200R	Stackpole Electronics Inc	Installed
R2,R3,R5,R6,R8,R21,R27	7	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402S	RMCF0402FT10K0	Stackpole Electronics Inc	Installed
R4,R10,R14,R28,R29,R30	6	0	RES, 0, 5%, 0.1 W, 0603	0603	RC0603JR-070RL	Yageo America	Installed
R7	1	10.0	RES, 10.0, 0.05%, 0.1 W, 0603	0603	RNCF0603AKT10R0	Stackpole Electronics Inc	Installed
R9,R17,R23	3	47.0k	RES, 47.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0747KL	Yageo	Installed
R11,R15	2	1.00k	RES, 1.00 k, 0.1%, 0.1 W, 0603	0603	RT0603BRB071KL	Yageo America	Installed
R12,R18	2	4.99k	RES, 4.99 k, 0.01%, 0.1 W, 0603	0603	RNCF0603TKY4K99	Stackpole Electronics Inc	Installed
R13,R16	2	15.0k	RES, 15.0 k, 0.05%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERA-3ARW153V	Panasonic	Installed
R19,R20	2	10.0	RES, 10.0, 1%, 0.063 W, 0402	0402S	RK73H1ETTP10R0F	KOA Speer	Installed

Table 4-1. Bill of Materials for the DAC81401EVM (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Assembly Details
R22	1	12.0k	RES, 12.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0712KL	Yageo	Installed
R24	1	1.00Meg	RES, 1.00 M, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M00FKEA	Vishay-Dale	Installed
R25	1	330	RES, 330, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402S	ERJ-2RKF3300X	Panasonic	Installed
R26	1	0	0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	FP-ERJ-3GEY0R00V_0603-MFG	ERJ-3GEY0R00V	Panasonic	Installed
SH-1, SH-2, SH-3, SH-4, SH-5, SH-6, SH-7, SH-8, SH-9, SH-10, SH-11	11		Shunt, 2.54mm, Gold, Black	Wurth_60900213421	60900213421	Wurth Elektronik	Installed
TP4, TP6, TP19	3		Test Point, Multipurpose, White, TH	Keystone5012	5012	Keystone Electronics	Installed
TP7, TP8, TP9, TP10	4		Test Point, Multipurpose, Blue, TH	Keystone5127	5127	Keystone Electronics	Installed
TP12, TP13, TP14, TP15, TP16	5		Test Point, Multipurpose, Black, TH	Keystone5011	5011	Keystone Electronics	Installed
TP21, TP22, TP23	3		Test Point, Multipurpose, Red, TH	Keystone5010	5010	Keystone Electronics	Installed
U1	1		Single-Channel, 16-Bit, High-Voltage Output DACs With Precision Internal Reference	PW0020A-MFG	DAC81401PWR	Texas Instruments	Installed
U2,U5	2		85 V, 250 mA Output Current, Precision Operational Amplifier	DNT0012B-MFG	OPA593DNT	Texas Instruments	Installed
U4	1		18 V Bidirectional Flat-Clamp Surge Protection Device, DRB0008A (VSON-8)	DRB0008A	TVS1801DRBR	Texas Instruments	Installed
U6	1		Precision, Lowest-Noise 36-V, Zero-Drift, 14-MHz MUX-Friendly, Rail-to-Rail Output, Operational Amplifier, D0008A (SOIC-8)	D0008A_N	OPA189ID	Texas Instruments	Installed
U7	1		Future Technology Devices International Ltd FT4232H Quad High Speed USB to Multipurpose UART/MPSSE IC, VQFN-56	VQFN-56	FT4232H-56Q-TRAY	FTDI	Installed
U8,U10	2		4-Bit Fixed Direction Voltage-Level Translator with Schmitt- Trigger Inputs, and Tri-State Outputs, WQFN14	BQA0014A-MFG	TXU0304BQA	Texas Instruments	Installed

Table 4-1. Bill of Materials for the DAC81401EVM (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Assembly Details
U9	1		7 V Bidirectional Flat-Clamp Surge Protection Device, DRB0008A (VSON-8)	DRB0008A	TVS0701DRBR	Texas Instruments	Installed
U11	1		Single Output High PSRR LDO, 250 mA, Fixed 3.3 V Output, 2.7 to 6.5 V Input, with Low IQ, 5-pin SOT (DDC), -40 to 125 degC, Green (RoHS & no Sb/Br)	DDC0005A_N	TPS73433DDCT	Texas Instruments	Installed
U12	1		Single Output Low Input Voltage Requirement LDO, 150 mA, Fixed 1.8 V Output, 1.8 to 5.5 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	DBV0005A_N	TPS72118DBVT	Texas Instruments	Installed
Y1	1		Crystal, 12 MHz, 18 pF, SMD	XTAL_ABM3	830036401	Wurth Elektronik	Installed
D4,D8	2		Diode, TVS, Bi, 85 V, 137 Vc, 1500 W, 11.5 A, SMC (No Polarity Mark)	SMC_Bi	SMCJ85CA-TR	STMicroelectronics	Not installed
J8,J23	2		SMA Jack, 50 ohm, Gold, R/A, TH	Samtec_SMA-J-P-H-RA-TH1	60311002114501	Wurth Elektronik	Not installed
U3	1		Precision, Lowest-Noise 36-V, Zero-Drift, 14-MHz MUX-Friendly, Rail-to-Rail Output, Operational Amplifier, D0008A (SOIC-8)	D0008A_N	OPA189ID	Texas Instruments	Not installed
Y2	1		Crystal, 12 MHz, 30 ppm, 18 pF, SMD	ABRACON_ABLS2	ABLS2-12.000MHZ-D4Y-T	Abracon Corporation	Not installed

5 Compliance Information

5.1 Compliance and Certifications

- DAC81401EVM EU Declaration of Conformity (DoC) for Restricting the use of Hazardous Substances (RoHS)

6 Additional Information

6.1 Trademarks

Windows® is a registered trademark of Microsoft.
All trademarks are the property of their respective owners.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2023) to Revision A (November 2023)	Page
• Added information for jumper J10	10

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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