TEXAS INSTRUMENTS

TAS3103EVM

Evaluation Module for Digital Audio Processor With 3D Effects

User's Guide

October 2002 *Digital Audio Solutions*

SLEU030

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It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Introduction

The TAS3103 EVM is an evaluation board for the TAS3103 digital audio processor. The EVM contains two TAS3103 devices to provide processing for up to six audio channels. The board is configurable to allow the full functionality of the TAS3103 digital audio processor to be evaluated. The TAS3103 EVM block diagram is shown in Figure 1–1.

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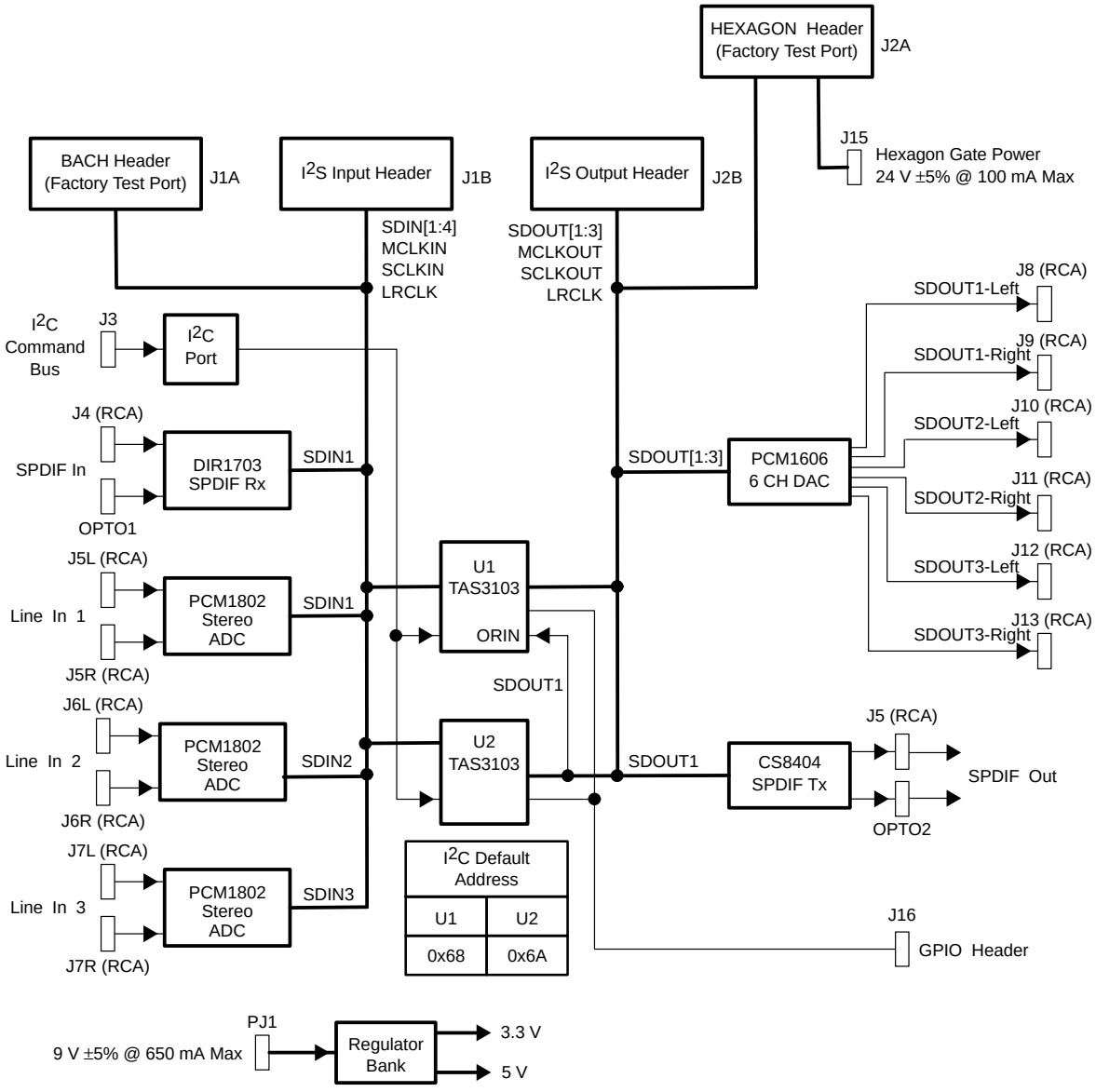
Figure 1–1. EVM Block Diagram



1.1 Input Ports

- SPDIF—Texas Instruments DIR1703 digital audio interface receiver supports sampling rates as high as 96 kHz. Two input connectors are provided, a coax input (RCA jack) and a TOSLINK optical connector.
- Six analog line-in channels—Three Texas Instruments/Burr Brown PCM1802 ADCs (24-bit, 96-kHz stereo) provide the six channels. Each ADC is provided with separate left channel and right channel RCA input jacks.
- I^2S input header—Provides the means of inputting four serial data sources (SDIN1, SDIN2, SDIN3, and SDIN4) and three clocks (MCLK, SCLK, and LRCLK). These three clocks can also be sourced from the EVM to an input device connected to the I^2S input header. One clock option is to output MCLK as a clock source to an input device, with the input device using MCLK to generate SCLK and LRCLK. Another clock option would be to source all three clocks (MCLK, SCLK, and LRCLK) to an input device. A third option would be to receive all three clocks from an input device. The input header is a 16-pin box header.
- BACH header—Factory test connector
- 24-V HEXAGON power connector—Factory test connector

1.2 Output Ports

- SPDIF—A Crystal CS8404A 96-kHz digital audio transmitter chip provides the SPDIF output. Two output connectors are provided, an RCA jack and a TOSLINK optical connector.
- A Texas Instruments Burr Brown PCM1606 six analog line-out channel, delta-sigma DAC provides six output channels. Six RCA output jacks are provided, one for each channel.
- I^2S output header—Provides the means of outputting three serial data sources (SDOUT1, SDOUT2, and SDOUT3) and three clocks (MCLK, SCLK, and LRCLK). The output header is a 16-pin box header.
- GPIO header—Provides access to the eight GPIO ports provided by the two TAS3103s. The output header is a 2x8 pin open header.
- HEXAGON header—Factory test connector

The board only requires one 9-V ±5%, 650-mA power source. A wall-mount power regulator to power the board is provided with the EVM. The power plug is a 2,1 mm PWR-MINI jack. From this 9-V input power source, the EVM provides power to a paddle board via the provided I^2C cable. The paddle board is used as an interface between a PC parallel port and the I^2C port on the EVM. The paddle board is provided with the EVM.

All clocks can be supplied by the board, the user can choose to input clocks via the I^2S input header, or the SPDIF Rx can supply all clocks.

Internally, all devices are configured to the I^2S data format. When using the SPDIF Rx or the ADCs to input data, the I^2S output header outputs I^2S formatted data. When using the I^2S input header to source data to the EVM and using either the SPDIF Tx or the DAC to output data, the data on the I^2S output header is I^2S formatted data. However, when using the I^2S input header to source data to the EVM and the I^2S output header to output the data, any of the data formats supported by the TAS34103 can be used.

The board contains a suite of switches that allow a user to place the two TAS3103s in almost all configurations the devices were designed to support. One red LED (LED1) is included to indicate power is applied and two yellow LEDs are provided to indicate the state of two of the general-purpose I/O pins. LED2, when lit, indicates U1–GPIO0 is logic 1. LED3, when lit, indicates U1–GPIO1 is logic 1. In the power-on default state these LEDs are lit.

Chapter 2

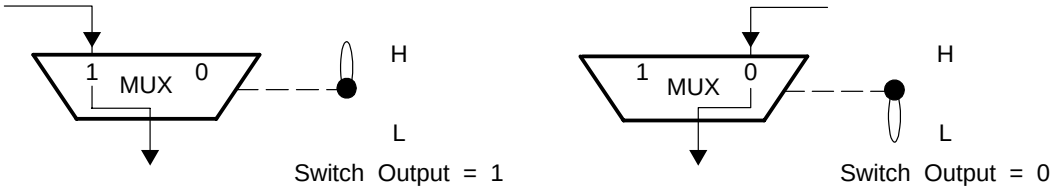
Board Configuration Options

Switches allow a user to customize the EVM to a particular application. The switches are sectioned into four groups:

- Data Flow Switches
- MCLK Routing Switches
- SCLK Routing Switches
- LRCLK Routing Switches

Figure 2–1 illustrates the schematic nomenclature adopted for all switches; the H and L markings are provided on the PCB.

Figure 2–1. Switch Settings



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2.1 Data Flow Switches

Figure 2–2 illustrates the data flow selections available. The data format settings for the ADCs, the DACs, the SPDIF Rx, and the SPDIF Tx are all hard-wired to the I^2S format. For this reason, data into and out of the I^2S ports must be I^2S formatted data if any of these devices are to be used.

Switch S2 selects between I^2S input header data and ADC data. The I^2S input header routes four serial data streams to the TAS3103s—SDIN1, SDIN2, SDIN3, and SDIN4. The ADCs only supply SDIN1, SDIN2, and SDIN3.

The SDIN2, SDIN3, and SDIN4 selections made by S2 directly route to both TAS3103s. (Note that a source for SDIN4 is only available on the I^2S input header). The SDIN1 selection made by S2 also directly routes to TAS3103–U2. But for TAS3103–U1, the SDIN1 selection made by S2 undergoes one more selection process that allows SPDIF Rx data to replace the S2 selection for SDIN1. This selection process is controlled by S4.

Table 2–1 summarizes the input data options.

Table 2–1. Data Input Options

Switch Settings		TAS3103 Input Data			
S2	**S4**	**SDIN1**	**SDIN2**	**SDIN3**	**SDIN4**
0	0	SPDIF Rx	I^2S header	I^2S header	I^2S header
0	1	I^2S header	I^2S header	I^2S header	I^2S header
1	0	SPDIF Rx	ADC	ADC	N/A
1	1	ADC	ADC	ADC	N/A

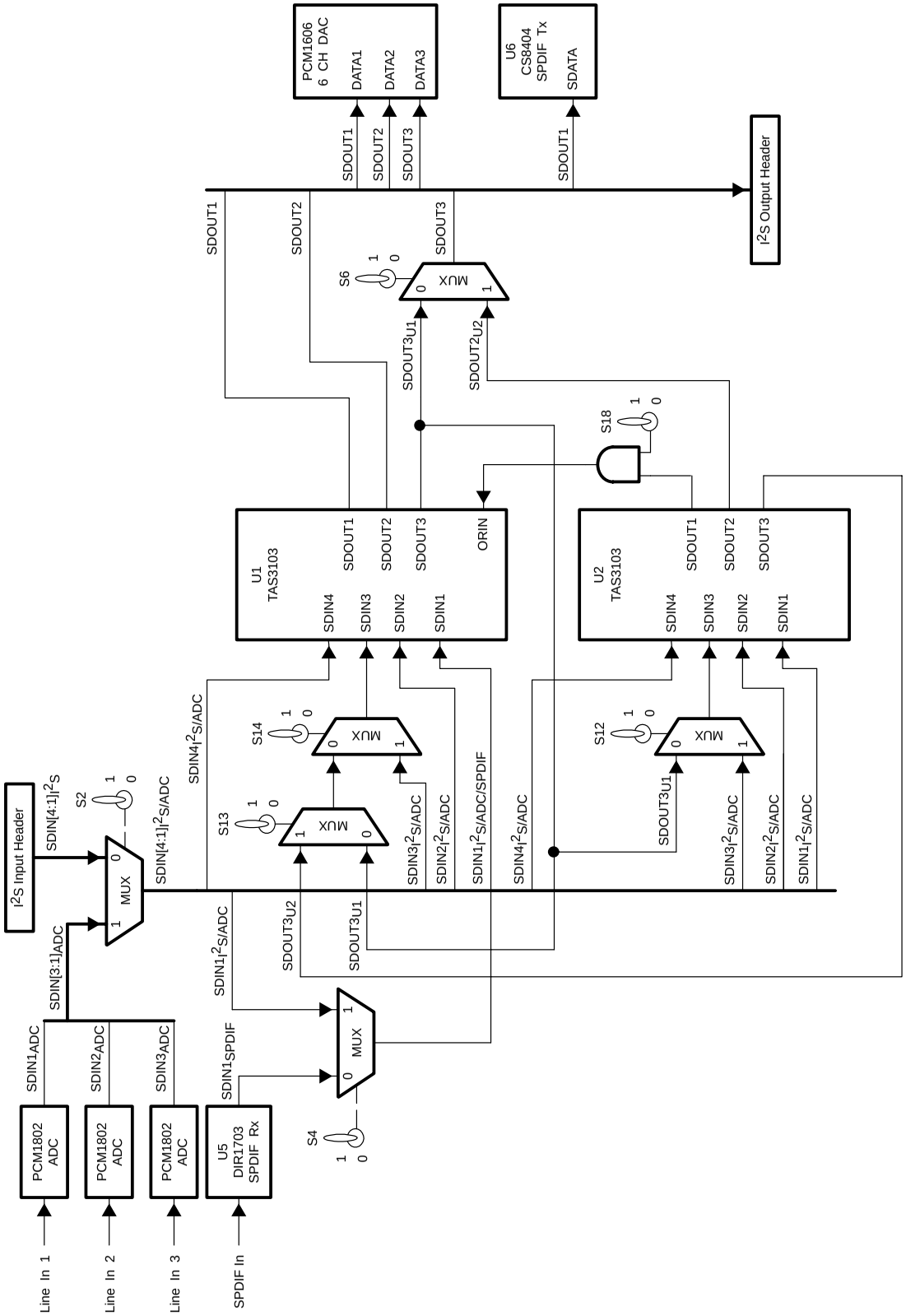
TAS3103 output data can also be fed back into input port SDIN3 on both TAS3103s. Switches S12, S13, and S14 provide the selections between S2-selected input data and the feedback data. For the input into SDIN3 on TAS3103–U2, S12 selects between the S2-selected SDIN3 input data and the SDOUT3 output from TAS3103–U1. For the input into SDIN3 on TAS3103–U1, switches S13 and S14 allow the user to select between the S2-selected SDIN3 input data, its own SDOUT3 output, or the SDOUT3 output from TS3103–U2.

Table 2–2 summarizes the data options for the TAS3103 SDIN3 inputs.

Table 2–2. TAS3103 SDIN3 Port Selections

Switch Settings			SDIN3 – TAS3103 – U1	SDIN3 – TAS3103 – U2
S12	**S13**	**S14**		
0	0	0	$SDOUT3_{U1}$	$SDOUT3_{U1}$
0	0	1	$SDIN3_{I2S/ADC}$	$SDOUT3_{U1}$
0	1	0	$SDOUT3_{U2}$	$SDOUT3_{U1}$
0	1	1	$SDIN3_{I2S/ADC}$	$SDOUT3_{U1}$
1	0	0	$SDOUT3_{U1}$	$SDIN3_{I2S/ADC}$
1	0	1	$SDIN3_{I2S/ADC}$	$SDIN3_{I2S/ADC}$
1	1	0	$SDOUT3_{U2}$	$SDIN3_{I2S/ADC}$
1	1	1	$SDIN3_{I2S/ADC}$	$SDIN3_{I2S/ADC}$

Figure 2–2. Data Path Switches



The TAS3103 can format all output channels on one TMD data stream. The output port used by the TAS3103 for this formatting option is SDOUT1. When both TAS3103s are being used and both are formatted to output a single TDM data stream, an option exists where both TDM data streams can be combined into a single TDM output data stream. In the EVM architecture, SDOUT1 of the TAS3103–U1 is chosen to be this data stream. The TDM output from the TAS3103–U2 is merged into this composite TDM data stream by connecting SDOUT1 of TAS3103–U2 to the ORIN input of the TAS3103–U1. Setting S18 to H enables this option. If ORIN of TAS3103–U1 is not used, S18 must be set to L.

For the I^2S output header and the PCM1606 DAC, outputs SDOUT1 and SDOUT2 are always sourced by TAS3103–U1, but SDOUT3 can be sourced by either SDOUT2 of the TAS3103–U2 (S6 set to H) or SDOUT3 of TAS3103–U1 (S6 set to L). The SPDIF Tx always outputs SDOUT1 of the TAS3103–U1.

2.2 MCLK Routing Switches

Figure 2–3 illustrates the MCLK options provided by the EVM. There are three choices for sourcing MCLK – SPDIF Rx, I^2S input header, and TAS3103–U1.

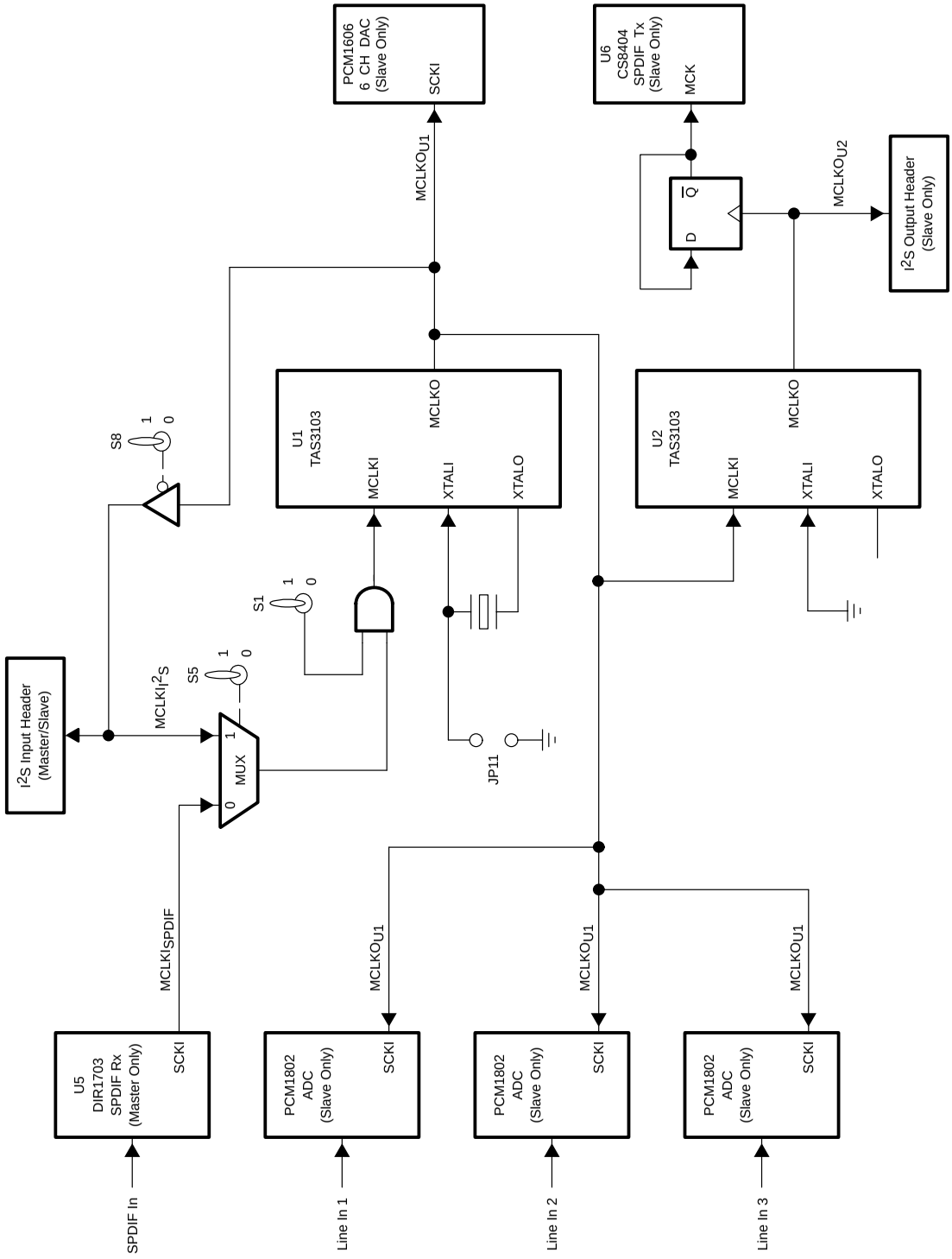
S5 selects between the SPDIF Rx MCLK (S5 = L) and an I^2S input port supplied MCLK (S5 = H). For the EVM architecture, if the SPDIF Rx is being used as a source of input data, MCLK, SCLK, and LRCLK from the SPDIF Rx must serve as the system clocks. The SPDIF Rx must always serve as clock master when used. If an MCLK from an input device connected to the I^2S input port is being used as the system MCLK, S8 must be set to H to place the driver used in a 3-state condition to output MCLK to an input device connected to the I^2S input port.

The S5 switch selection is routed to an AND gate, where it is gated with the S1 switch setting. If TAS3103–U1 is to be supplied an MCLK (TAS3103–U1 is a slave device), S1 must be set to H to allow the selected MCLK to pass through the AND gate to pin MCLKI of TAS3103–U1. Also, in this case, a shunt must be attached to JP11 to disable the XTALI pin.

If TAS3103–U1 is to serve as the source of MCLK, the crystal resource connected to pins XTALI and XTALO must be used to derive MCLK. In the TAS3103, MCLKI and XTALI are OR'ed together and thus it is necessary that MCLKI be driven with a logic 0 signal when not being supplied an external MCLK. In this case, then, S1 must be set to L, and the shunt must be removed from JP11.

MCLKO of TAS3103–U1 is used to source MCLK for all devices on the EVM other than the SPDIF Rx, regardless of whether or not TAS3103–U1 is the source of MCLK. In the TAS3103 power-up default state, MCLKO = (MCLKI OR XTALI). Subsequent I^2C commands can be issued to the TAS3103 to set MCLKO to (MCLKI OR XTALI)/2 or (MCLKI OR XTALI)/4. But for the EVM architecture, MCLKO must always be set to (MCLKI OR XTALI) if either the output DAC, the input ADCs, or the SPDIF Tx is being used.

Figure 2–3. MCLK Switches



If TAS3103–U1 is the source of MCLK and this clock is being supplied to the I^2S input port, S8 must be set to L. The architecture of the TAS3103 allows it to be the source of MCLK and yet be slaved to external SCLK and LRCLK clocks. This means that TAS3103–U1 can supply MCLK to an external device connected to the I^2S input port and operate as a slave using SCLK and LRCLK.

MCLKO of TAS3103–U1 is also used to source MCLKI for TAS3103–U2. MCLKO of TAS3103–U2 supplies MCLK to the I^2S output header and to a divide-by-2 flip-flop whose output provides MCLK to the SPDIF Tx (all devices except the SPDIF Tx use a 256 Fs MCLK; the SPDIF Tx uses a 128 Fs MCLK). For TAS3103–U2, MCLKO must remain in its power-on default state of MCLKO = MCLKI.

On the EVM, the TAS3103's MCLKO output serves as a buffer for the distribution of MCLK. These additional sources of MCLK allow optimal MCLK distribution topologies to be achieved and clock trace noise management goals to be realized.

The I^2S input port can serve as either a master port, a slave port, or a mixed port whereby MCLK is provided to an external device, but SCLK and LRCLK are provided by the external device. The I^2S output port, on the other hand, is strictly a slave port that outputs MCLK, SCLK, and LRCLK, along with data, to external devices.

Caution

TAS3103 – U1 can serve as either a master or slave device. TAS3103 – U2 must always be a slave device.

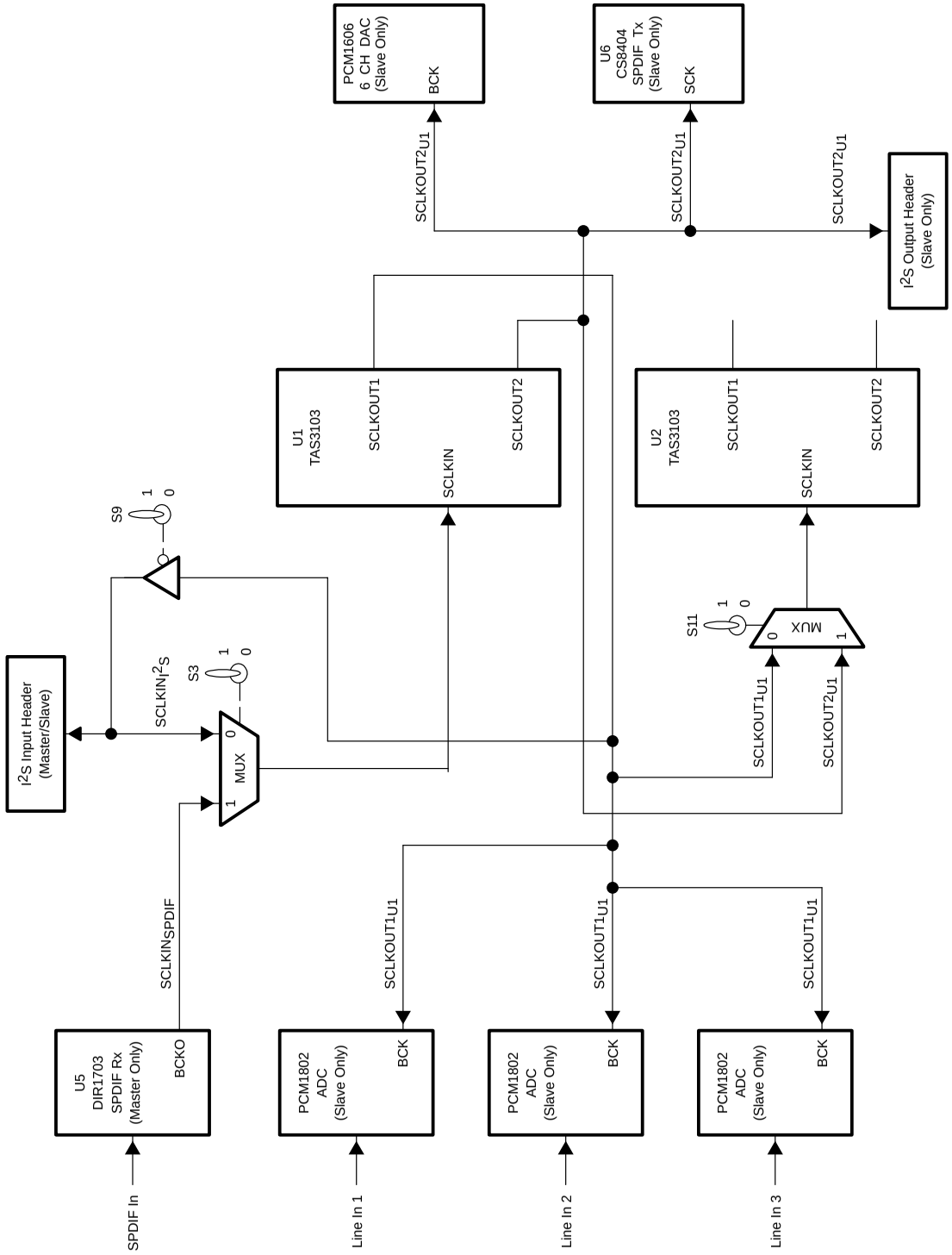
2.3 SCLK Routing Switches

Figure 2–4 illustrates the SCLK options provided by the EVM. As is the case for MCLK, there are three choices for sourcing SCLK—SPDIF Rx, I^2S input header, and TAS3103–U1. Again, if the SPDIF Rx is used to source SCLK, it must also source MCLK and LRCLK.

S3 selects between the SPDIF Rx SCLK (S3 = H) and an I^2S input port SCLK (S3 = L). The output of the S3 selection is directly routed to pin SCLKIN of TAS3103–U1. If the I^2S input port is used to source SCLK, S9 must be set to H to place in a 3-state condition the driver used to supply SCLK to an input device connected to the I^2S input port.

There are two SCLK output pins on each TAS3103. SLCKOUT1 is used to clock serial data into the TAS3103 and SCLKOUT2 is used to clock data out of the TAS3103. Two separate clocks are necessary since the input and output data bit rates can be different. An application using a discrete in/TDM out topology results in a higher frequency output clock than the input clock (SCLKOUT2 > SCLKOUT1). An application using a TDM in/discrete out topology results in a higher frequency input clock than the output clock (SCLKOUT2 < SCLKOUT1). If the TAS3103 is in the slave mode (the power-on default state), SCLKOUT1 and SCLKOUT2 are derived from SCLKIN. If SCLKOUT 1 ≠ SCLKOUT2, SCLKIN must be equal to the higher of the two clocks. If the TAS3103 is in the master mode, both SCLKOUT1 and SCLKOUT2 are derived from (MCLKI OR XTALI).

Figure 2–4. SCLK Switches



SCLKOUT1 of TAS3103–U1 serves as the SCLK for the ADCs and SCLKOUT2 of TAS3103–U1 serves as the SCLK for the 6-channel DAC and the SPDIF Tx. Both SCLKOUT clocks are routed to a multiplexer. Switch S11 selects whether SCLKOUT1 of TAS3103–U1 (S11 set to L) or SCLKOUT2 of TAS3103–U1 (S11 set to H) is routed to pin SCLKIN of TAS3103–U2. This multiplexer is necessary as either clock can be the higher frequency clock in certain applications and SCLKIN must be provided the higher of the two clocks.

If TAS3103–U1 is the master and provides SCLK to an external device on the I^2S input port, switch S9 must be set to L to enable the gate driving SCLK to the external device. When the TAS3103 is a master, the signal on pin SCLKIN is not used, and thus the state of the signal into the pin is not an issue.

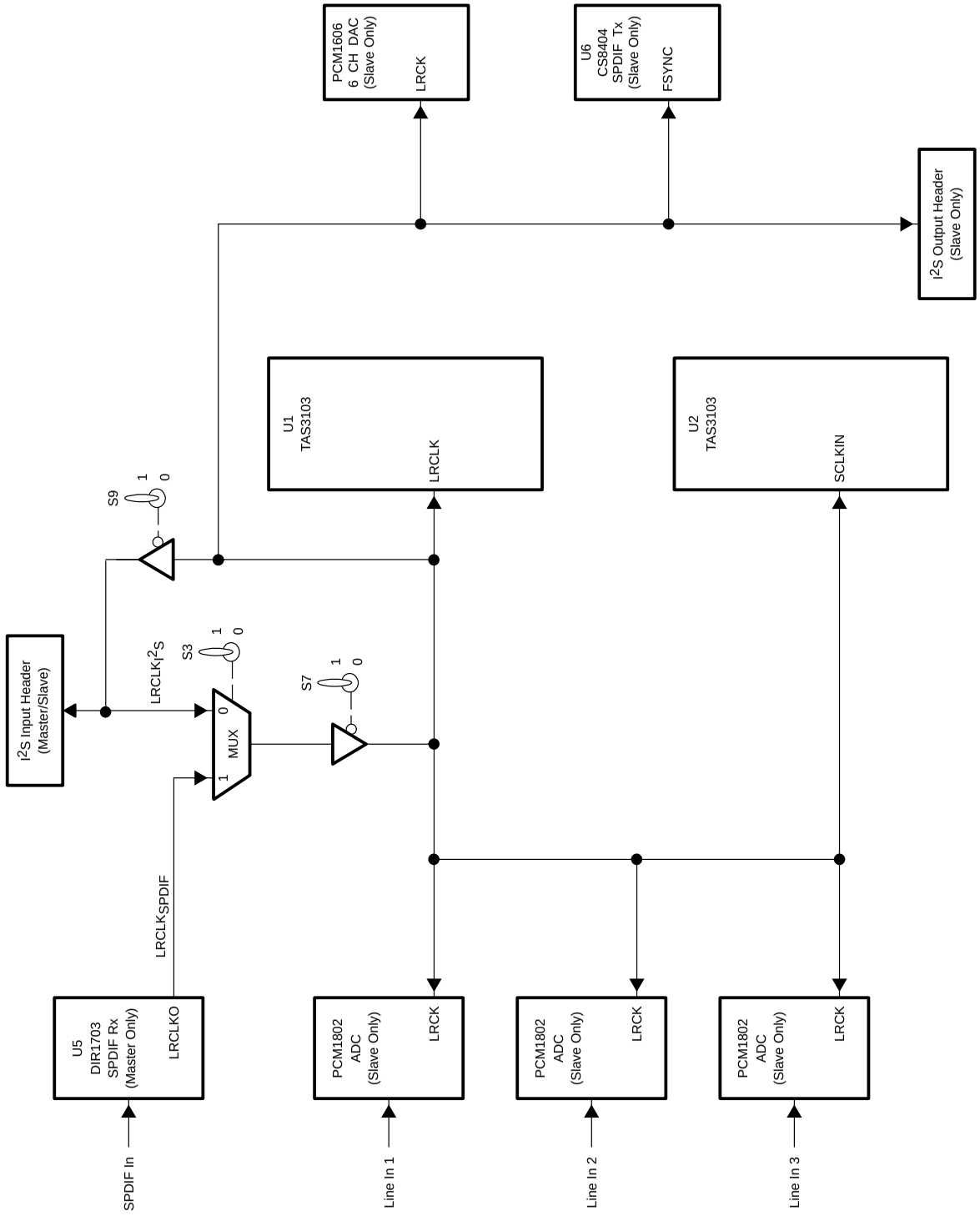
2.4 LRCLK Routing Switches

Figure 2–5 illustrates the LRCLK options provided by the EVM. There are three choices for sourcing LRCLK—SPDIF Rx, I^2S input header, and TAS3103–U1. Again, if the SPDIF Rx is used to source LRCLK, it must also source MCLK and SCLK.

S3 selects between the SPDIF Rx LRCLK (S3 = H) and an I^2S input port LRCLK (S3 = L). If the I^2S input port is used to source LRCLK, S9 must be set to H to place in a 3-state condition the driver used to supply LRCLK to an input device connected to the I^2S input port. (Note that S3 and S9 served the same functions for SCLK).

The output of the S3 selection is routed to a buffer whose output is controlled by switch S7. In the TAS3103, LRCLK is a bidirectional pin. When the TAS3103 is serving as clock master, any devices driving this pin must be placed in a 3-state condition. When S7 is set to H, the driver is placed in the 3-state condition.

Figure 2–5. LRCLK Switches



Chapter 3

EVM Contents and PCB Connector Layout

This chapter discusses the EVM contents and PCB connector layout.

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- ❑ TAS3103 Evaluation Board
- ❑ Wall-Mount Power Supply
- ❑ CD Containing
  - ■ DCT (TAS3103 GUI) Software
  - ■ ALE (Automatic Loud Speaker Equalizer) Software
  - ■ TAS3103 Data Manual
  - ■ EVM Data Manual
  - ■ DCT Operating Instructions
  - ■ TAS3103 EVM Schematic
  - ■ TAS3103 EVM Bill Of Materials
- ❑ Paddle Board for Allowing PC Control of Evaluation Board
- ❑ Paddle Board Connection Cable

3.2 PCB Connector Layout