

DEM-DAI3052A

User's Guide

DEM-DAI3052A

User's Guide

Literature Number: SLEU079
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Description

The DEM-DAI3052A is an evaluation board for the PCM3052A, a 96-kHz, 24-bit stereo audio coder/decoder (codec), with digital audio interface receiver/transmitter, optical and coaxial interface, onboard clock generator, –6-dB amplifier with LPF for ADC and 4-dB amplifier with LPF for DAC, switches or jumpers for mode or clock control, and interface connector with PC for serial mode control.

The DEM-DAI3052A operates under 5-V and ± 15 -V analog power supplies, with 1-V_{rms} or 2-V_{rms} unbalanced analog signal input and 2-V_{rms} unbalanced analog signal output.

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1.1 Block Diagram

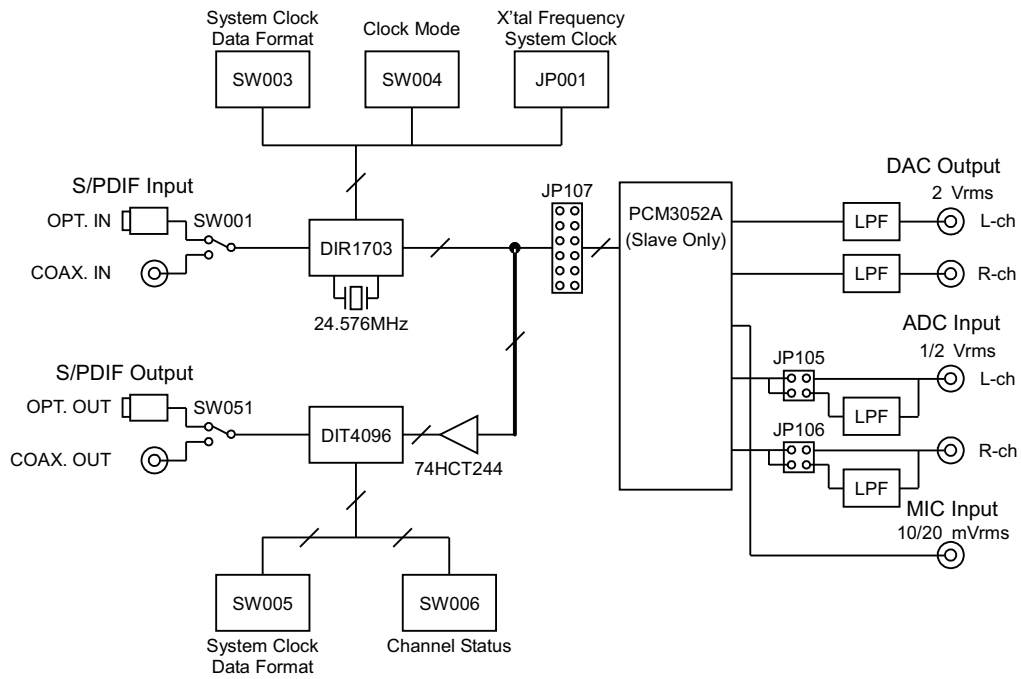


Figure 1-1. DEM-DAI3052A Block Diagram

1.2 Basic Connection and Operation

1.2.1 Basic Connections and Configurations

- Install REGTEST_I2C and other programs attached to the EVM into the appropriate folder of the PC that is used to control this EVM.
- Confirm EVM settings. SW053 must be all OFF (High). JP051 SCL, SDA, MDO, and DOUTS must be OFF, OFF, OFF, and ON, respectively.
- Connect the 5-V and ± 15 -V power supplies to V_{CC} , $\pm AV_{CC}$, and GND on CN051–CN055. If external 3.3 V is used on CN056, jumper CN057 must be removed. The ± 15 -V power supplies are required for 2-Vrms input and 2-Vrms output.
- Connect the SPDIF input to CN059 (coaxial) or U053 (optical) and output to CN058 (coaxial) or U052 (optical), and select coaxial or optical for SPDIF input and output using SW001 and SW051. Also, select the SPDIF output source from the analog-to-digital converter (ADC) output or the digital-to-analog converter (DAC) input using SW052.
- Select the system clock source from x'tal or SPDIF input recover clock using SW004, select the system clock using SW003 SCF1/0 for DIR1703 and using SW005 CLK1/0 for DIT4096, and select the system clock frequency for x'tal mode using JP001 setting.
- Set the interface format (24-bit I²S) using SW003 FMT1/0 for DIR1703 and using SW005 FMT1/0 for DIT4096.
- Set the channel status for DIT4096 using SW006 if required. (It is not required for PCM3052A evaluation.)
- Select the analog input/output configuration according to application interface, specifically, select the DUT PCM3052A V_{CC} from 5 V or 4.5 V using JP109, the Mic input configuration of single ended or differential using JP110, the ADC input full scale from 2 Vrms or 1 Vrms using JP105/6, and the DAC output LPF band width from 20 kHz or 40 kHz using JP101-104.

1.2.2 Configuration Controls

Table 1-1. CN057: 3.3-V Power Source Selection

CN057	DESCRIPTION
OFF	3.3 V must be supplied on CN056.
ON	3.3 V must be supplied by on board regulator, U051 (default).

Table 1-2. SW001: SPDIF Input Selection

SW001	DESCRIPTION
COAX	Select coaxial connector as SPDIF input (default)
OPT	Select optical connector as SPDIF input

Table 1-3. SW051: SPDIF Output Selection

SW051	DESCRIPTION
COAX	Select coaxial connector as SPDIF output
OPT	Select optical connector as SPDIF output (default)

Table 1-4. SW052: SPDIF Output Source Signal Selection

SW052	DESCRIPTION
REC	Select DOUTS of PCM3052A, DAC input
DIT	Select DIT4096 output, ADC output (default)

Table 1-5. SW004: DIR1703 Clock Source Selection

SW004	DESCRIPTION
X'tal	SCKO (system clock out) is generated from crystal clock.
PLL	SCKO is generated from SPDIF recovery clock.
AUTO	Source clock of SCKO is automatically selected according to PLL lock state (default).

Table 1-6. SW003: DIR1703 System Clock Selection

SW003		DESCRIPTION
SCF1	SCF0	
OFF (L)	OFF (L)	128 f _S
OFF (L)	ON (H)	256 f _S (Default)
ON (H)	OFF (L)	384 f _S
ON (H)	ON (H)	512 f _S

Table 1-7. SW005: DIT4096 Master Clock Selection

SW005		DESCRIPTION
CLK1	CLK0	
OFF (H)	OFF (H)	512 f _S
OFF (H)	ON (L)	384 f _S
ON (L)	OFF (H)	256 f _S (default)
ON (L)	ON (L)	Unused

Table 1-8. JP001: DIR1703 Crystal Selection for Crystal Mode System Clock and Default Sampling Frequency

JP001	DESCRIPTION
OPEN	6.144/12.288/18.432/24.576 MHz for 128 f _S /256 f _S /384 f _S /512 f _S , 48 kHz
CSBIT	12.288/24.576/36.864/49.152 MHz for 128 f _S /256 f _S /384 f _S /512 f _S , 96 kHz (default)
URBIT	11.2896/22.5792/33.8688/45.158 MHz for 128 f _S /256 f _S /384 f _S /512 f _S , 88.2 kHz
EMFLG	5.6448/11.2896/16.9344/22.5792 MHz for 128 f _S /256 f _S /384 f _S /512 f _S , 44.1 kHz
BFRAME	4.096/8.192/12.288/16.384 MHz for 128 f _S /256 f _S /384 f _S /512 f _S , 32 kHz

Table 1-9. SW003: DIR1703 Format Selection

SW003		DESCRIPTION
FMT1	FMT0	
OFF (L)	OFF (L)	16 bits MSB first, right justified
OFF (L)	ON (H)	24 bits MSB first, right justified
ON (H)	OFF (L)	24 bits MSB first, left justified
ON (H)	ON (H)	24 bits MSB first, I ² S format (default)

Table 1-10. SW005: DIT4096 Format Selection

SW005		DESCRIPTION
FMT1	FMT0	
OFF (H)	OFF (H)	16-bit right justified
OFF (H)	ON (L)	24-bit right justified
ON (L)	OFF (H)	24-bit I ² S (default)
ON (L)	ON (L)	24-bit left justified

Table 1-11. SW006: DIT4096 Channel Status Information Control⁽¹⁾

SW006	DESCRIPTION
CSS	Channel status data mode input (default: on)
COPY-C	Copy protect or channel status data input (default: on)
U	User data input (default: on)
V	Validity data input (default: on)
L	Generation status input (default: on)
/AUDIO	Audio data valid control input (default: on)
/EMPH	Pre-emphasis status input (default: off)
BLSM	Block start mode control input (default: off)
BLS	Block start I/O (default: off)

⁽¹⁾ Control of these switches is not required for PCM3052A function and performance evaluation.

Table 1-12. SW053: Mode Control

SW053	DESCRIPTION
RESET	Function control that is defined on RESET (default: off)
MDI	Function control that is defined on MDI (default: off)
MC	Function control that is defined on MC (default: off)
ML	Function control that is defined on ML (default: off)

Table 1-13. JP051: DOOTS or MDO Setting for Mode Control

JP051	DESCRIPTION
1/4	Change SCL configuration to MC configuration (default: off)
2/4	Change SCA configuration to MD configuration (default: off)
3/4	Enable MDO (default: off)
4/4	Enable DOOTS (default: on)

Table 1-14. JP109: DUT (PCM3052A) V_{CC} Supply Voltage Selection

JP109	DESCRIPTION
LEFT	DUT V _{CC} is supplied from external 5 V (default).
RIFHT	DUT V _{CC} is supplied from onboard 4.5-V regulator

Table 1-15. JP110: MIC Input Configuration

JP110	DESCRIPTION
LEFT	Single-ended microphone input
RIFHT	Differential microphone input (default)

Table 1-16. JP101-104: Lineout LPF Selection

JP101,102,103,104	DESCRIPTION
OFF	40-kHz BW
ON	20-kHz BW (default)

Table 1-17. JP105, JP106: ADC Input Level Selection

JP105,106	DESCRIPTION
1 Vrms	1.06-Vrms full-scale voltage on ADC inputs (default)
2 Vrms	2.12-Vrms full-scale voltage on ADC inputs

Table 1-18. JP107: Bridge for PCM Audio Interface

JP107	DESCRIPTION
ON	All straps must be mounted for interfacing onboard SPDIF receiver/transmitter.
OFF	All straps must be removed and connecting external audio interface signals on JP107 (signal) – JP111 (GND) for interfacing with external equipment.

Table 1-19. JP108: Bridge for Mode Control Interface

JP108	DESCRIPTION
ON	All straps must be mounted for interfacing with PC via CN060.
OFF	All straps must be removed and connecting external control interface signals on right-side of JP108 for interfacing with external equipment.

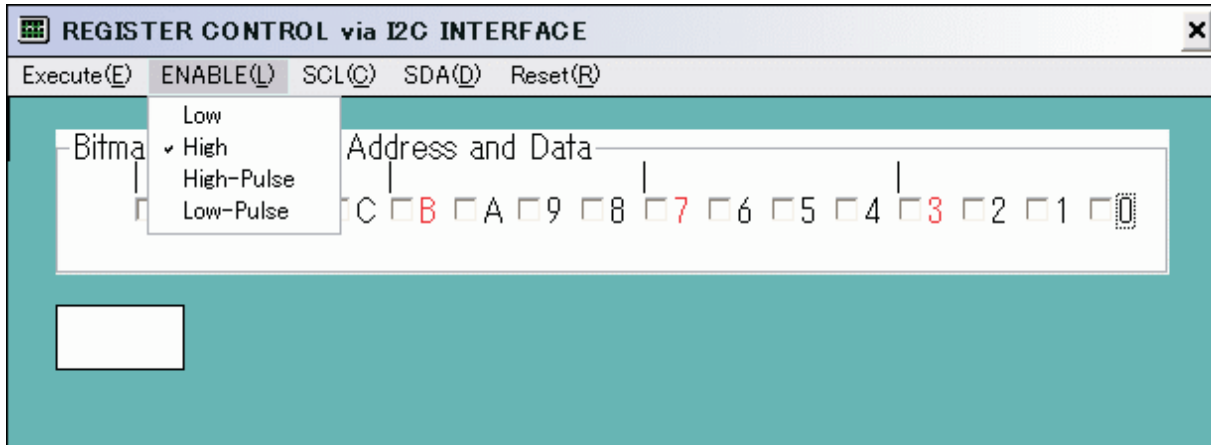
1.2.3 DEM-DAI3052A EVM Operation

Start

Run EVM control software by double clicking REGTEST_I²C.

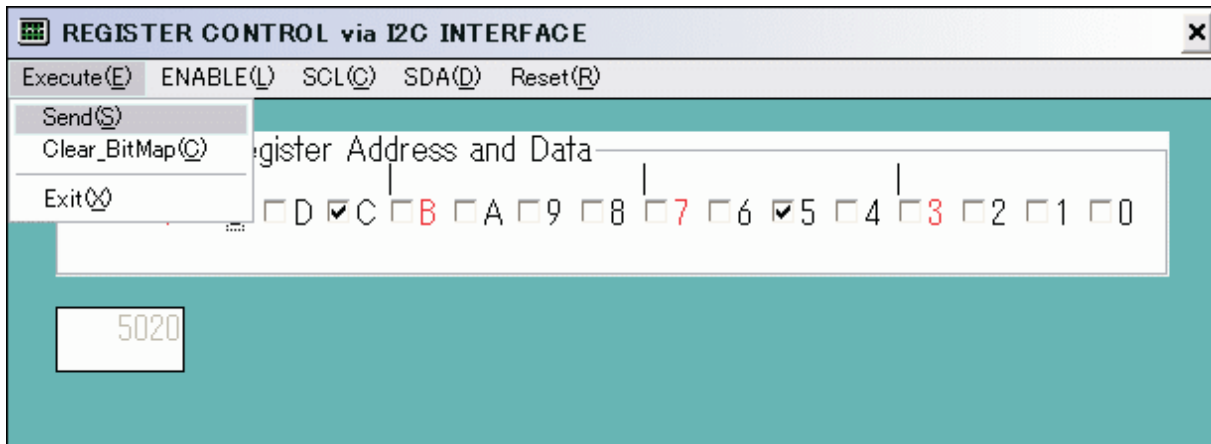
Initialization

Click pulldown menu, and select “High” for “ENABLE(L)”, “High-Pulse” for “SCL(C)”, “SDA(D)”, and “Low-Pulse” for “Reset(R)” for standard control.



Send Command

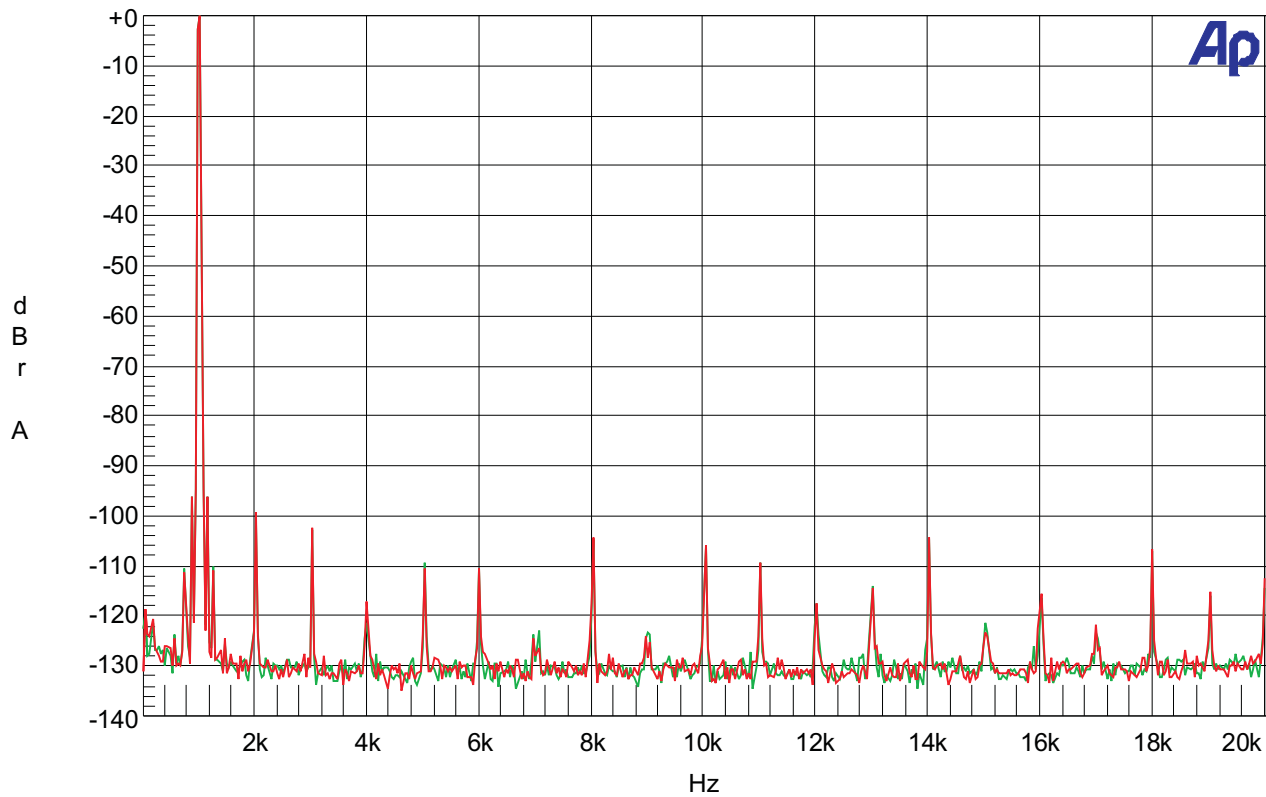
Click box, which should be set to “1”, so that address and data is set to desired value. Click pulldown menu, “Execute (E)”, and select “Send (S)”, so that command that is already set up is sent through the printer port.



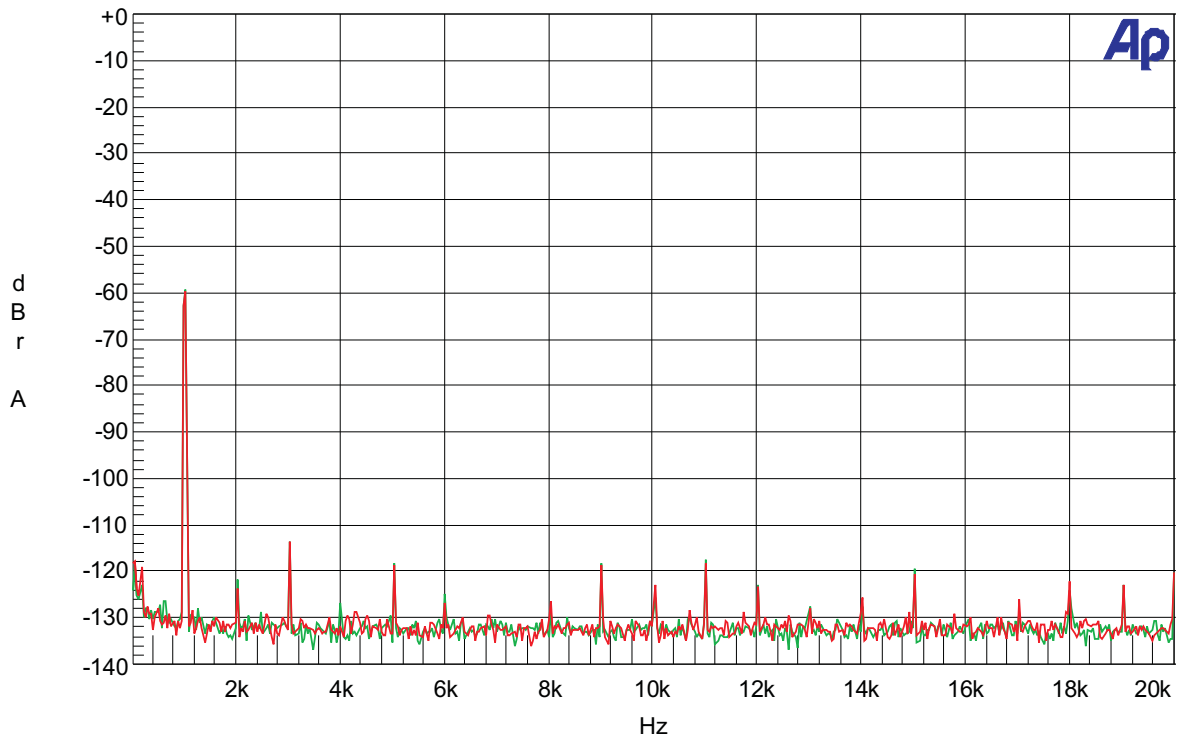
1.3 Typical Performance and Measurement Example

The following graphs show typical performance and FFT results for the ADC and DAC.

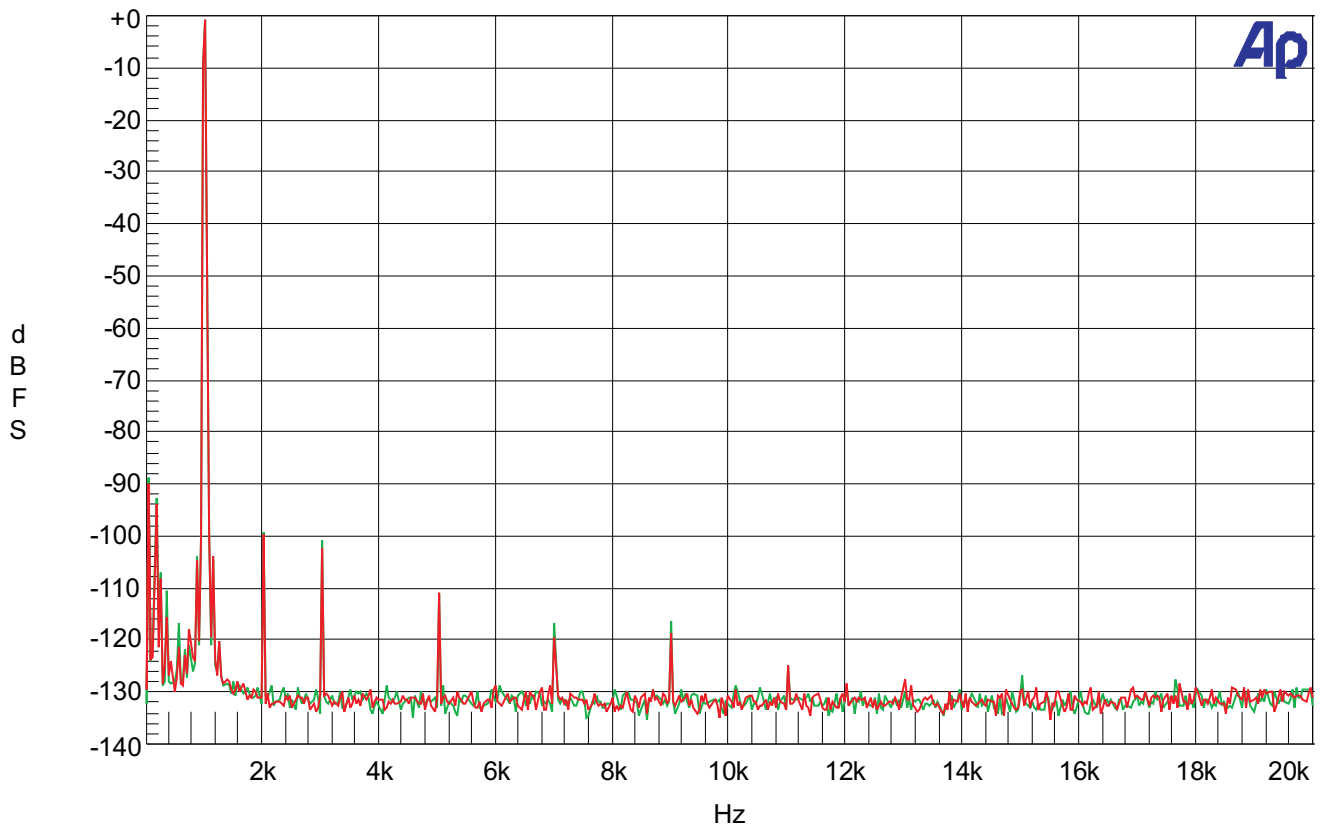
PCM3052A, DAC, 48 kHz, 0 dB



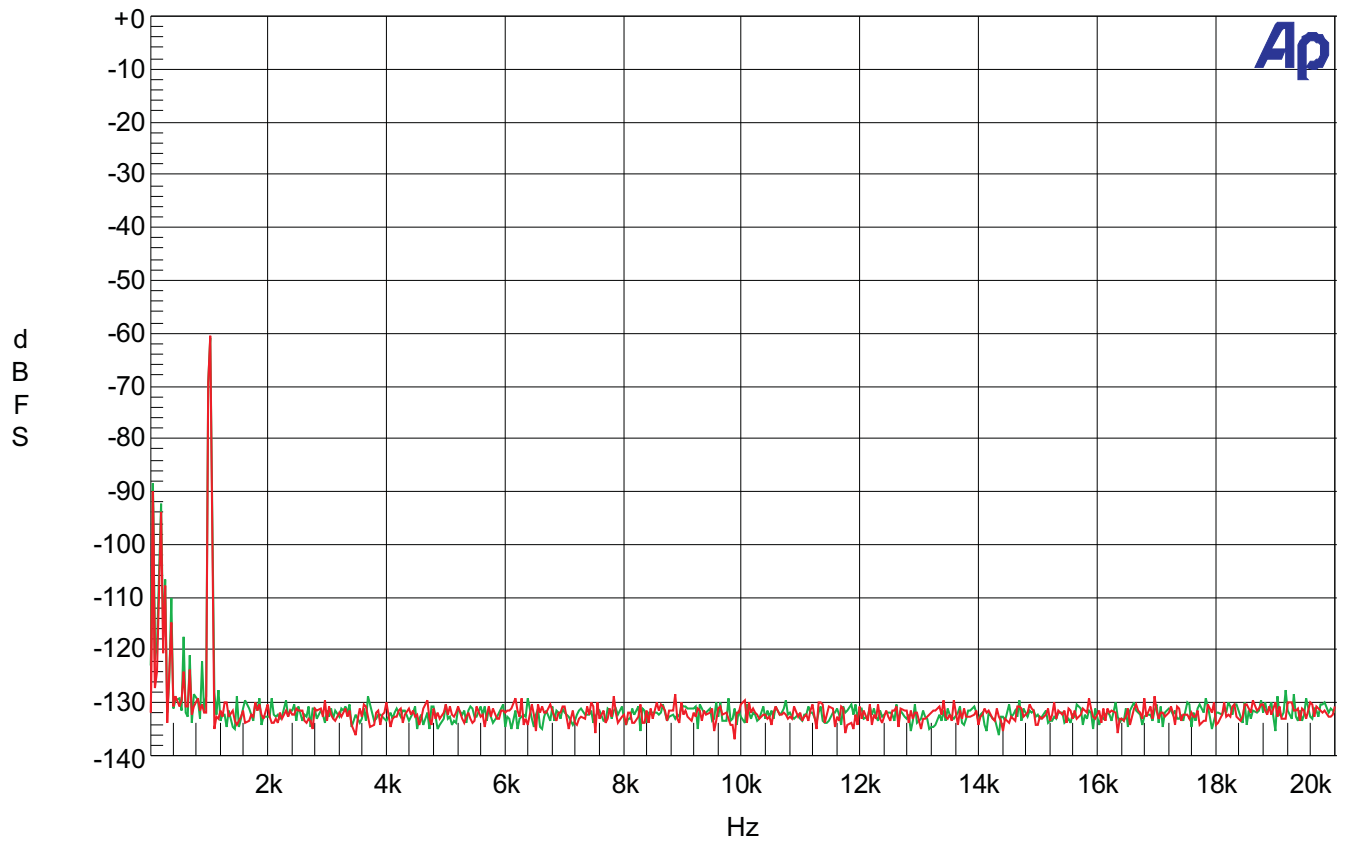
PCM3052A, DAC, 48 kHz, -60 dB



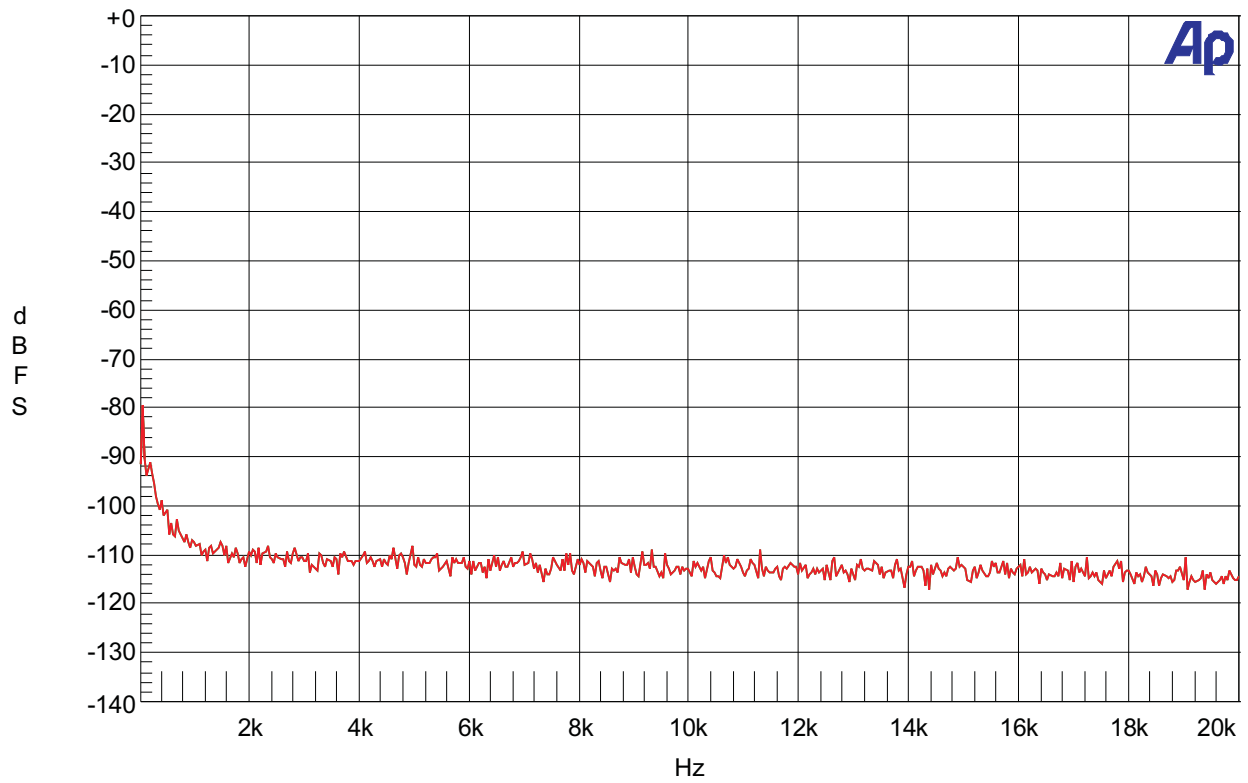
PCM3052A, ADC, 48 kHz, Line, -0.5 dB



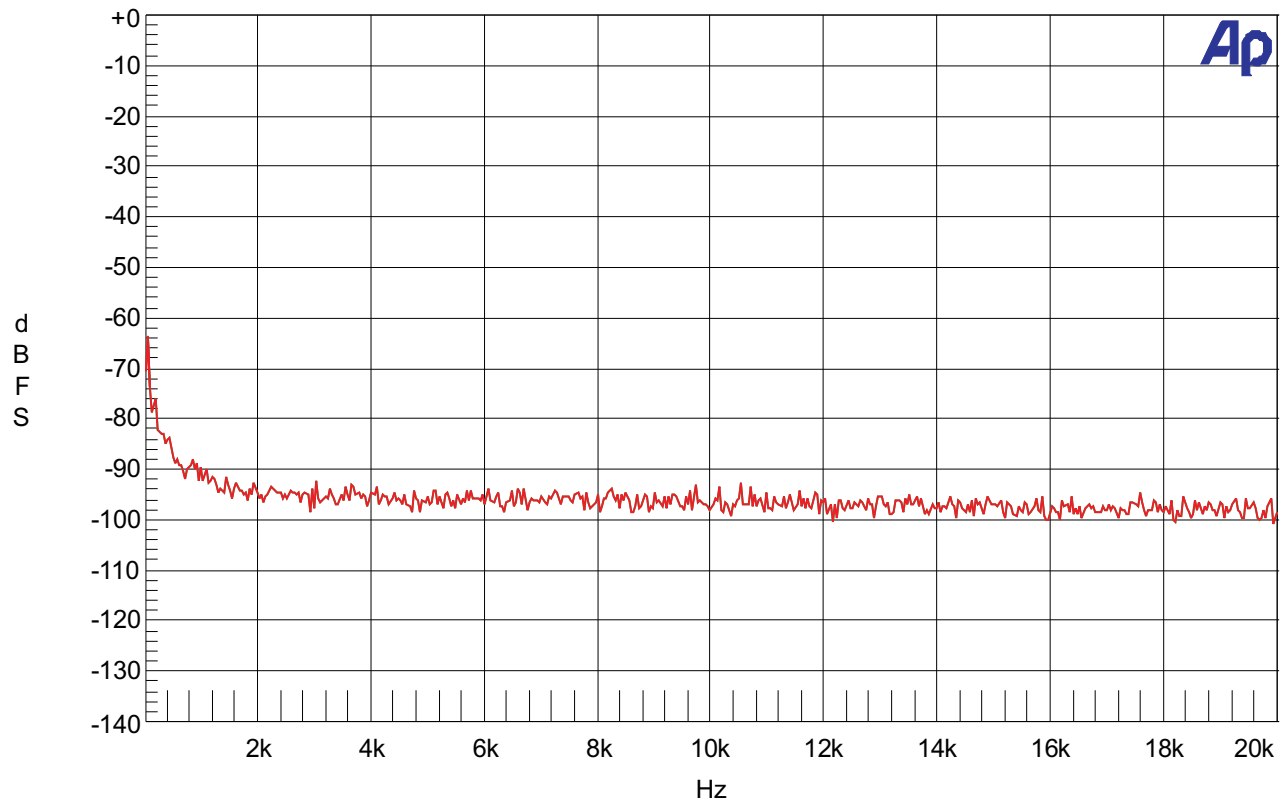
PCM3052A, ADC, 48 kHz, Line, -60 dB



PCM3052A, ADC, 48 kHz, Mic, No input signal



PCM3052A, ADC, 48 kHz, Mic with 20 dB gain, No input signal



Typical Performance and Measurement Example

Schematics and Printed Circuit Boards

This chapter presents the DEM-DAI3052A schematics, Bill of Materials (BOM), and printed circuit boards.

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2.1 DEM-DAI3052A Schematics

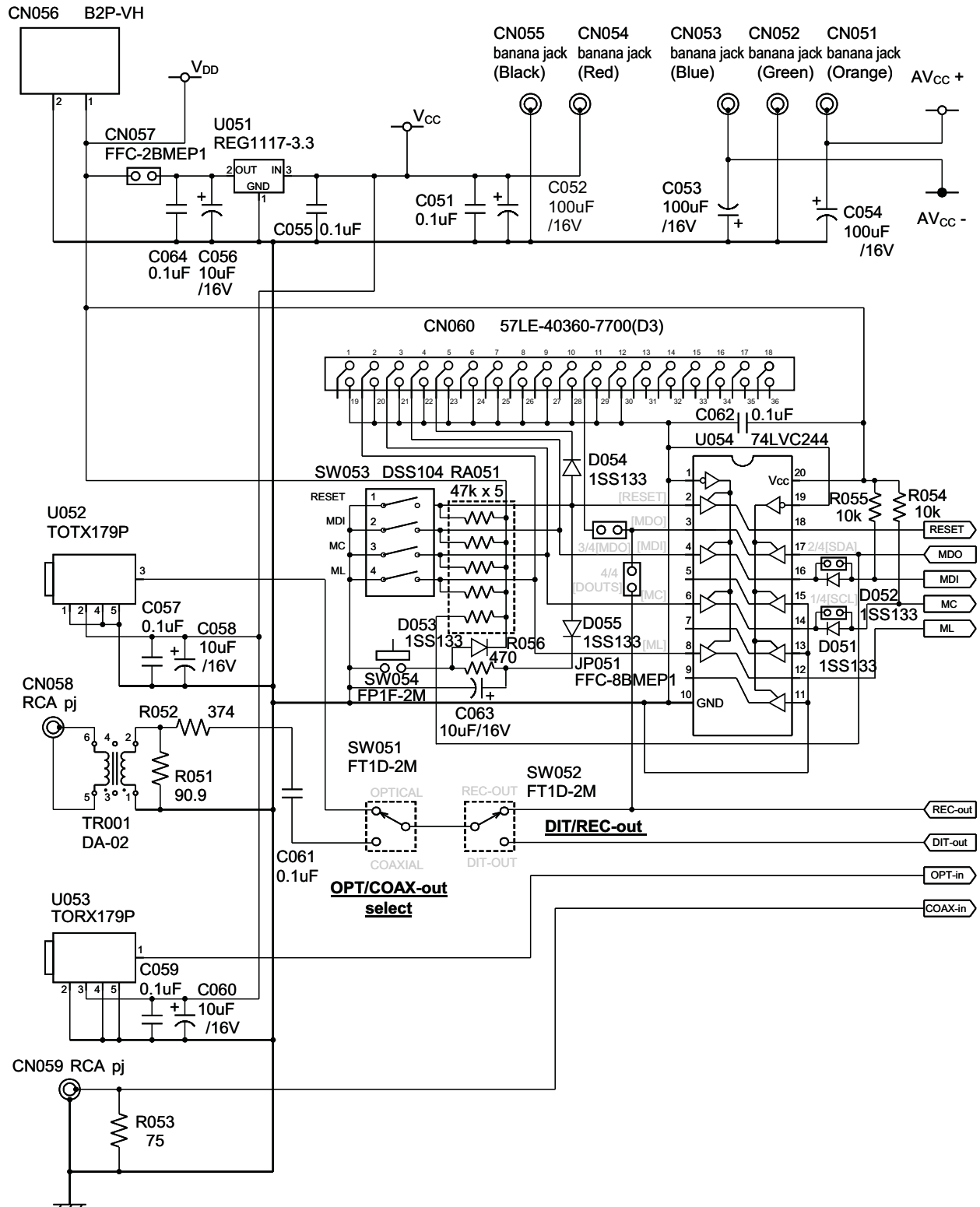


Figure 2-1. DEM-DAI3052A Power and Interface Section

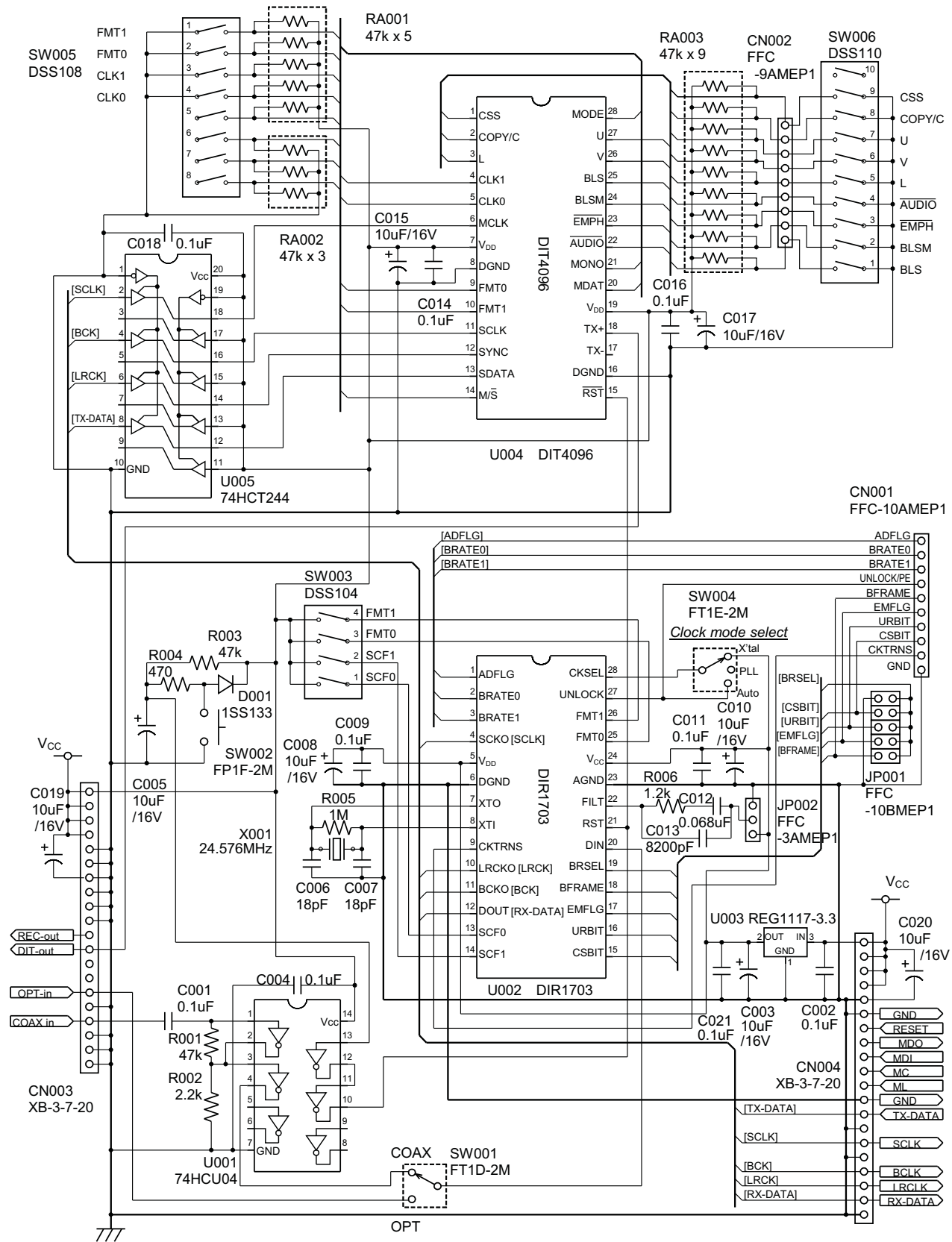


Figure 2-2. DEM-DAI3052A Digital Section (Digital Audio Interface)

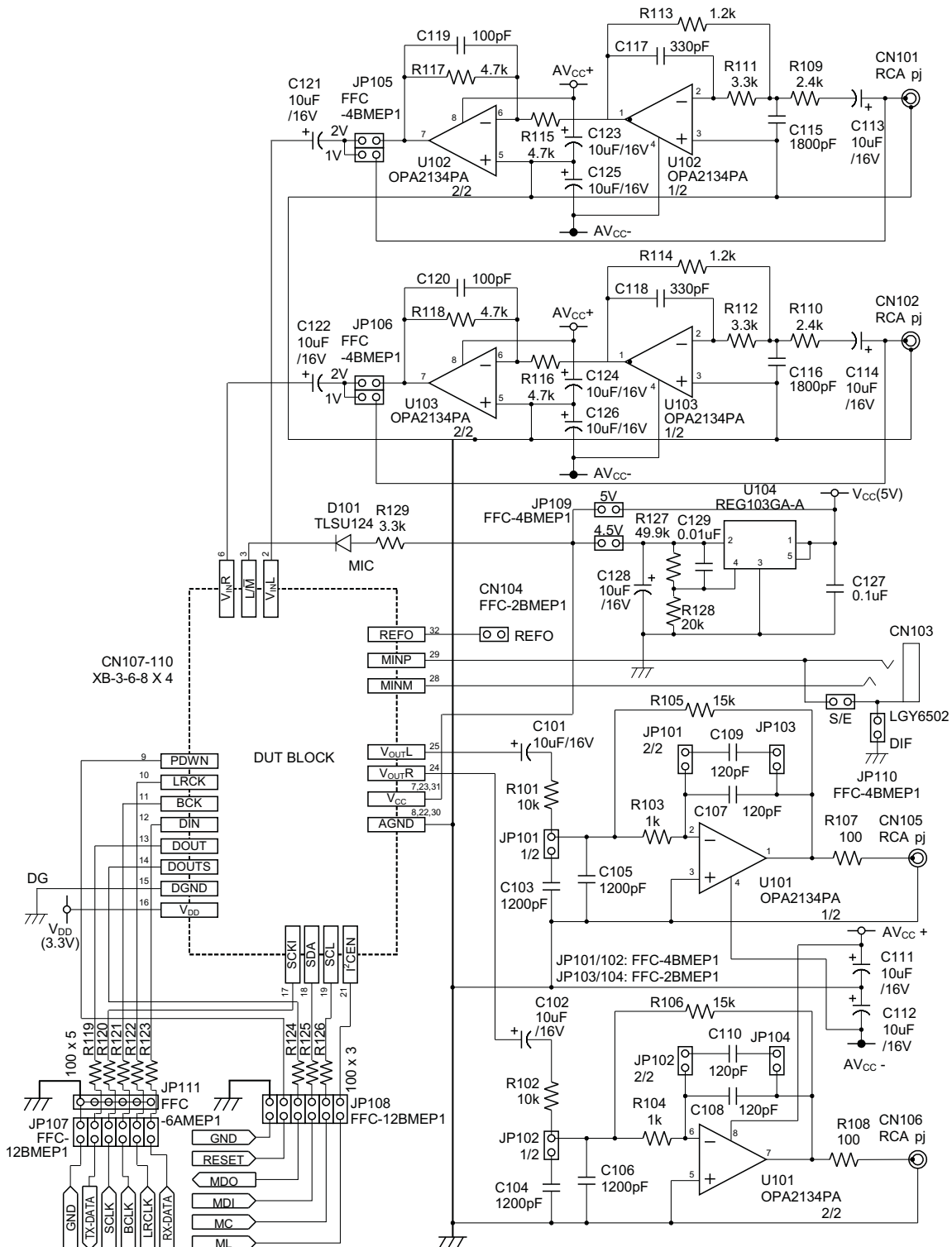


Figure 2-3. DEM-DAI3052A Analog Section

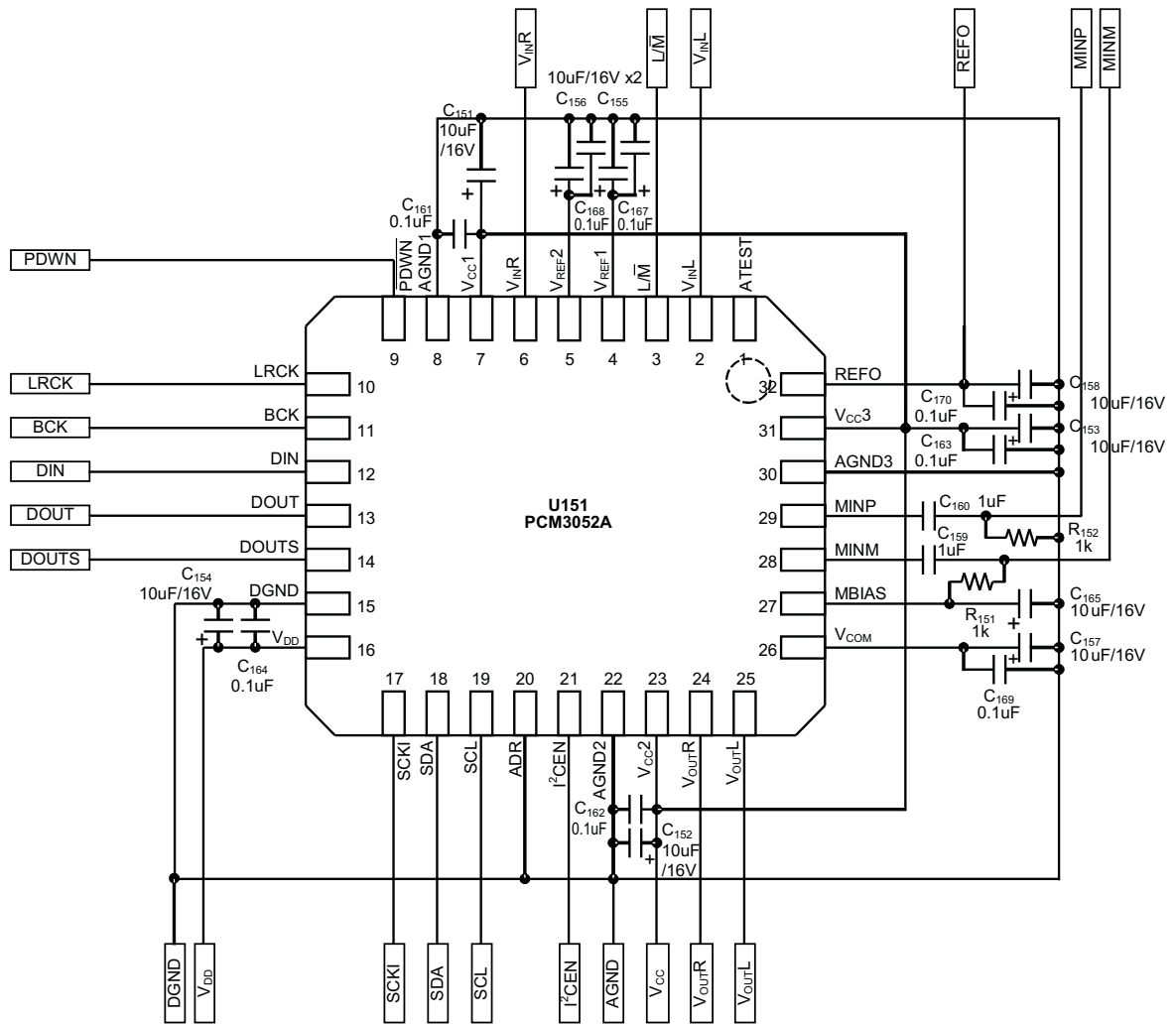


Figure 2-4. DEM-DAI3052A DUT Section

2.2 DEM-DAI3052A Bill of Materials (BOM)

REFERENCE DESIGNATORS	PART DESCRIPTION	MANUFACTURER PART NO.	SPECIFICATION	MANUFACTURER	QTY
D001, D051, D052, D053, D054, D055	Diode	1SS133		ROHM	6
D101	LED	TLSU124(F)		Toshiba	1
U001	Hex Unbuffered Inverter	SN74HCU04NS		TI	1
U002	Digital Interface Receiver	DIR1703DB		TI	1
U003, U051	3.3-V Regulator	REG1117-3.3		TI	2
U004	Digital Interface Transmitter	DIT4096PW		TI	1
U005	Octal Buffer Driver	SN74HCT244NS		TI	1
U052	TOSLINK Optical Transmitter	TOTX179P		Toshiba	1
U053	TOSLINK Optical Receiver	TORX179P		Toshiba	1
U054	Octal Buffer Driver	SN74LVC244ANS		TI	1
U101, U102, U103	Op Amp	OPA2134PA		TI	3
U104	Regulator IC	REG103GA-A		TI	1
U151	Stereo Audio Codec	PCM3052A	(DUT)	TI	1
X001	Crystal Resonator	HC-49/U-S-24.576 MHz	24.576 MHz	Kinseki	1
C001, C061	Polyester Film Capacitor	AMCF0050J104	0.1 uF	Nissei Electronic	2
C012	Polyester Film Capacitor	AMZF0050J683	0.068 uF	Nissei Electronic	1
C013	Polyester Film Capacitor	AMCF0050J822	8200 pF	Nissei Electronic	1
C103, C104, C105, C106	Polypropylene Film Capacitor	APSF0100J122	1200 pF	Nissei Electronic	4
C107, C108, C109, C110	Polypropylene Film Capacitor	APSF0100J121	120 pF	Nissei Electronic	4
C115, C116	Polypropylene Film Capacitor	APSF0100J182	1800 pF	Nissei Electronic	2
C117, C118	Polypropylene Film Capacitor	APSF0100J331	330 pF	Nissei Electronic	2
C119, C120	Polypropylene Film Capacitor	APSF0100J101	100 pF	Nissei Electronic	2
C002, C004, C018, C051, C055, C057, C059, C062, C127, C021, C064	Ceramic Capacitor	RPEF11H104Z2K1A01B	0.1 uF	Murata	11
C006, C007	Ceramic Capacitor	RPE2C1H180J2P1Z01B	18 pF	Murata	2
C129	Ceramic Capacitor	RPER11H103K2P1A01B	0.01 uF	Murata	1
C009, C011, C014, C016, C161, C162, C163, C164, C167, C168, C169, C170	Chip Ceramic Capacitor	GRM188B11E104KA01	0.1 uF/25 V 1608 type	Murata	12
C003, C005, C008, C010, C015, C017, C056, C058, C060, C063, C111, C112, C123, C124, C125, C126, C128, C151, C152, C153, C154, C155, C156, C157, C158, C165	Electrolytic Capacitor	R3A-16V100M	10 uF/16 V	ELNA	26
C052, C053, C054	Electrolytic Capacitor	ROA-16V101M	100 uF/16 V	ELNA	3
C101, C102, C113, C114, C121, C122	Electrolytic Capacitor	ROA-16V100M	10 uF/16 V	ELNA	6
C159, C160	Electrolytic Capacitor	UEP1H010MDT	1 uF, Bi-polar	Nichicon	2
R001, R003	Metal Film Resistor	MFS1/4CC-47kΩF	1/8 W, 47 kΩ	KOA	2
R002	Metal Film Resistor	MFS1/4CC-2.2kΩF	1/8 W, 2.2 kΩ	KOA	1

REFERENCE DESIGNATORS	PART DESCRIPTION	MANUFACTURER PART NO.	SPECIFICATION	MANUFACTURER	QTY
R004, R056	Metal Film Resistor	MFS1/4CC-470 ΩF	1/8 W, 470 Ω	KOA	2
R005	Metal Film Resistor	MFS1/4CC-1M ΩF	1/8 W, 1 MΩ	KOA	1
R006, R113, R114	Metal Film Resistor	MFS1/4CC-1.2kΩF	1/8 W, 1.2 kΩ	KOA	3
R051	Metal Film Resistor	MFS1/4CC-90.9ΩF	1/8 W, 90.9 Ω	KOA	1
R052	Metal Film Resistor	MFS1/4CC-374ΩF	1/8 W, 374 Ω	KOA	1
R053	Metal Film Resistor	MFS1/4CC-75ΩF	1/8 W, 75 Ω	KOA	1
R054, R055, R101, R102	Metal Film Resistor	MFS1/4CC-10kΩF	1/8 W, 10 kΩ	KOA	4
R103, R104, R151, R152	Metal Film Resistor	MFS1/4CC-1kΩF	1/8 W, 1 kΩ	KOA	4
R105, R106	Metal Film Resistor	MFS1/4CC-15kΩF	1/8 W, 15 kΩ	KOA	2
R107, R108, R119, R120, R121, R122, R123, R124, R125, R126	Metal Film Resistor	MFS1/4CC-100ΩF	1/8 W, 100 Ω	KOA	10
R109, R110	Metal Film Resistor	MFS1/4CC-2.4kΩF	1/8 W, 2.4 kΩ	KOA	2
R111, R112, R129	Metal Film Resistor	MFS1/4CC-3.3kΩF	1/8 W, 3.3 kΩ	KOA	3
R115, R116, R117, R118	Metal Film Resistor	MFS1/4CC-4.7kΩF	1/8 W, 4.7 kΩ	KOA	4
R127	Metal Film Resistor	MFS1/4CC-49.9kΩF	1/8 W, 49.9 kΩ	KOA	1
R128	Metal Film Resistor	MFS1/4CC-20kΩF	1/8 W, 20 kΩ	KOA	1
RA001, RA051	Resistor Array	M6-1-473J	47 kΩ × 5	Beckman	2
RA002	Resistor Array	M4-1-473J	47 kΩ × 3	Beckman	1
RA003	Resistor Array	M10-1-473J	47 kΩ × 9	Beckman	1
TR001	Pulse Transformer	DA-02		JPC	1
CN001	10-Pin Pin Header	FFC-10AMEP1		Honda Tsushin	1
CN002	9-Pin Pin Header	FFC-9AMEP1		Honda Tsushin	1
CN051	Banana Jack (Orange)	T-45 (Orange)		Sato Parts	1
CN052	Banana Jack (Green)	T-45 (Green)		Sato Parts	1
CN053	Banana Jack (Blue)	T-45 (Blue)		Sato Parts	1
CN054	Banana Jack (Red)	T-45 (Red)		Sato Parts	1
CN055	Banana Jack (Black)	T-45 (Black)		Sato Parts	1
CN056	2-Pin VH Connector	B2P-VH(LF)(SN)		JST	1
CN057	2-Pin Pin Header	FFC-2BMEP1		Honda Tsushin	1
CN058, CN059	RCA Connector (Yellow)	LPR6520-0804 (Yellow)		SMK	2
CN060	Ribbon Connector (Centronics)	57LE40360-7700(D3)-FA		DDK	1
CN101, CN105	RCA Connector (White)	LPR6520-0803 (White)		SMK	2
CN102, CN106	RCA Connector (Red)	LPR6520-0802 (Red)		SMK	2
CN103	3.5 mm Stereo Min Plug	YKB21-5274B		JALCO	1
CN104	2-Pin Pin Header	FFC-2AMEP1		Honda Tsushin	1
JP001	10-Pin Pin Header	FFC-10BMEP1		Honda Tsushin	1
JP002	3-Pin Pin Header	FFC-3AMEP1		Honda Tsushin	1
JP051	8-Pin Pin Header	FFC-8BMEP1		Honda Tsushin	1
JP101, JP102, JP105, JP106, JP109, JP110	4-Pin Pin Header	FFC-4BMEP1		Honda Tsushin	6
JP103, JP104	2-Pin Pin Header	FFC-2BMEP1		Honda Tsushin	2
JP107	18-Pin Pin Header	FFC-18NSM1		Honda Tsushin	1

DEM-DAI3052A Bill of Materials (BOM)

REFERENCE DESIGNATORS	PART DESCRIPTION	MANUFACTURER PART NO.	SPECIFICATION	MANUFACTURER	QTY
JP108	12-Pin Pin Header	FFC-12BMEP1		Honda Tsushin	1
	Short Plug	DIC-130		Honda Tsushin	28
SW001, SW051, SW052	Toggle Switch (DPDT)	FT1D-2M-Z		Fujisoku	3
SW002, SW054	Push Switch	FP1F-2M-Z		Fujisoku	2
SW003, SW053	DIP Switch	DSS104	4 elements	Fujisoku	2
SW004	Toggle Switch (DPDT With Neutral)	FT1E-2M-Z		Fujisoku	1
SW005	DIP Switch	DSS108	8 elements	Fujisoku	1
SW006	DIP Switch	DSS110	10 elements	Fujisoku	1

2.3 DEM-DAI3052A Printed Circuit Boards

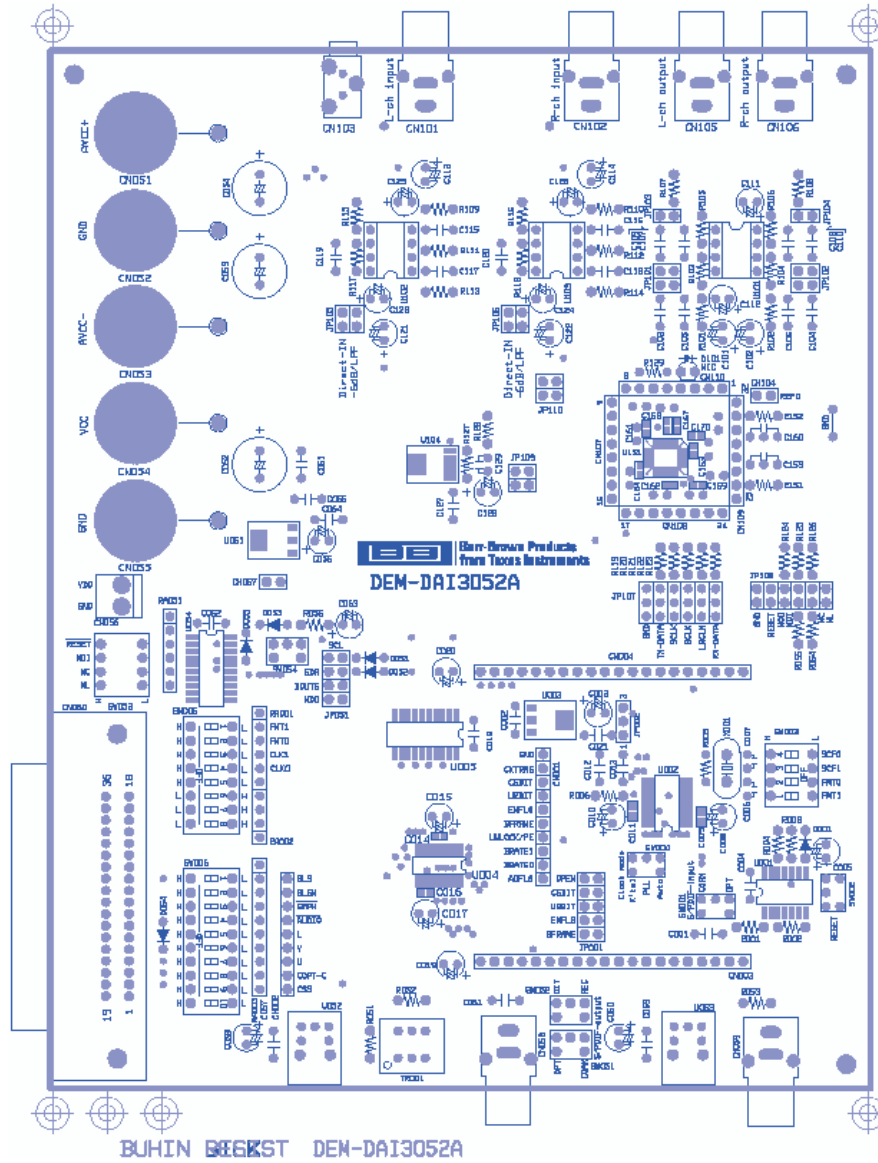


Figure 2-5. DEM-DAI3052A Top Silkscreen

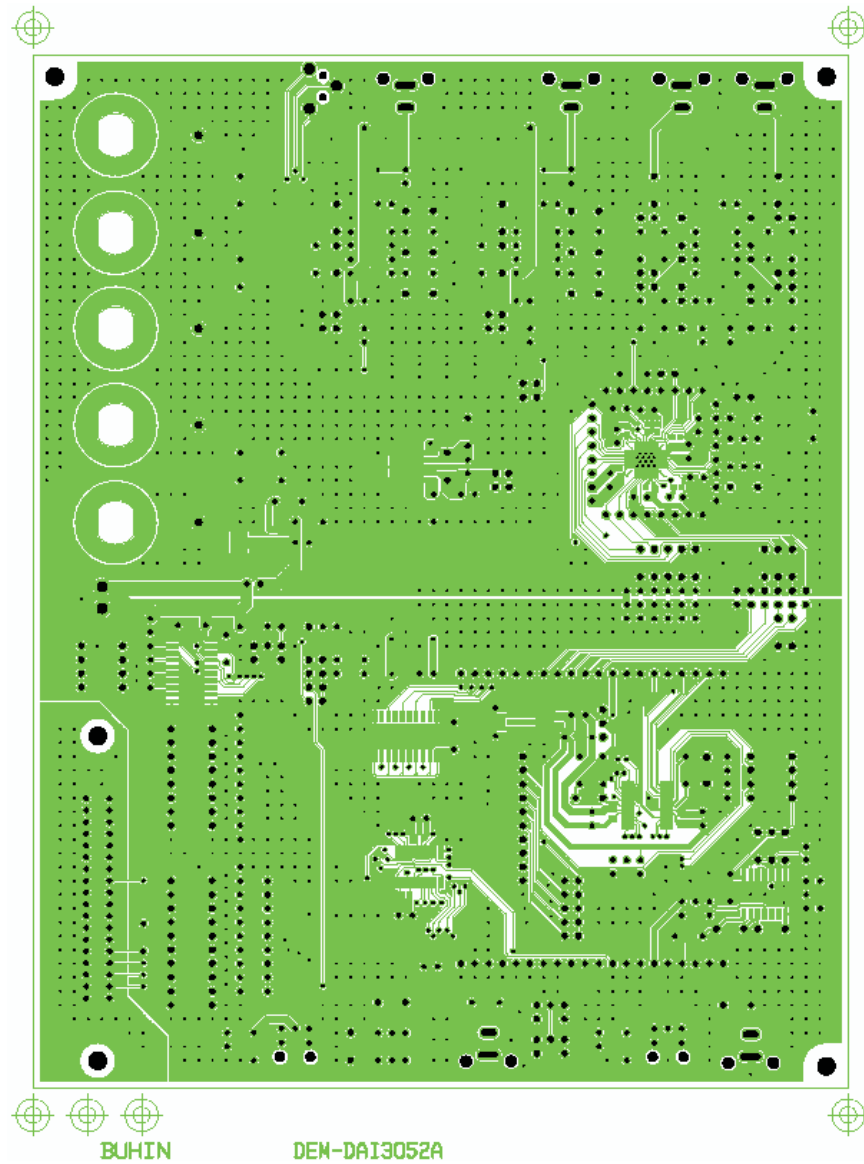


Figure 2-6. DEM-DAI3052A Top Copper

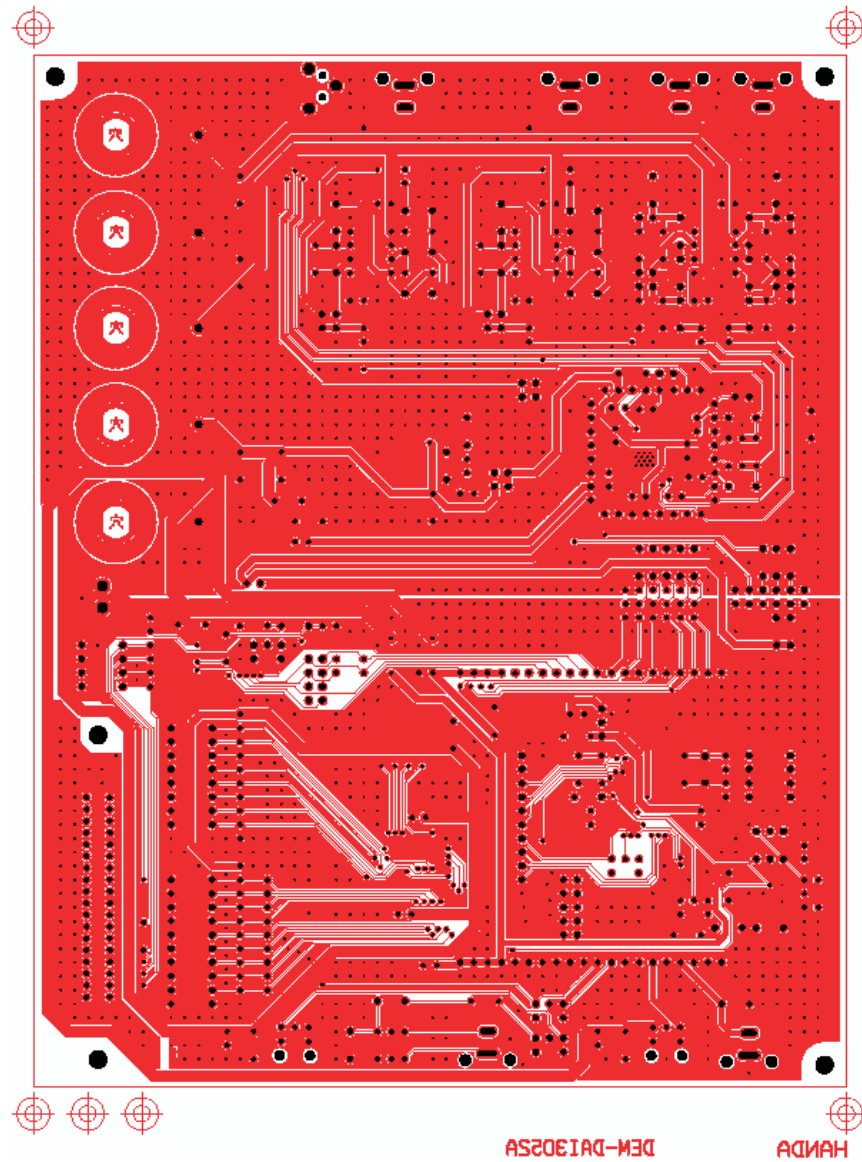


Figure 2-7. DEM-DAI3052A Bottom Copper

EVM TERMS AND CONDITIONS

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It is user's responsibility to ensure that persons handling the EVM and the product have electronics training and observe good laboratory practice standards.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range and the output voltage range that is less than 120% of the corresponding nominal voltage ranges described in the EVM user's guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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