This user’s guide describes the SN55LVCP22-CVAL evaluation module (EVM). The SN55LVCP22EVM-CVAL highlights the high-speed performance and functionality of the SN55LVCP22 2x2 crosspoint switch. This guide contains the EVM schematic, bill of materials, assembly drawing, and board layouts.

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1 Introduction

The SN55LVCP22 (LVDS output) is a high-speed 2x2 crosspoint switch. The four different functions that this crosspoint provides are shown in Figure 1. The functions are selected via pins SEL0 and SEL1. Control pins EN0 and EN1 enable or disable the outputs. The receiver has a wide input common-mode voltage range with an ability to accept LVDS, LVPECL and CML signaling levels.

![Figure 1. SN55LVCP22 Functional Configurations](image1)

![Figure 2. SN55LVCP22EVM-CVAL](image2)
1.1 Signal Paths

The signal paths on this EVM include 8 edge-launch SMA connectors (J8-J16) for high-speed data transmission, 2 jumpers for active switch logic control, 2 jumpers (J6 and J7) for enabling and disabling the outputs, and three banana jacks (J3, J4, J5) for power and ground connections. Note GND is tied to VCC01 to allow for proper common mode termination to 50-Ω loads. See Figure 10.
Setup and Equipment Required

The output characteristics of the SN55LVCP22 are specified in the TIA/EIA-644 standard. LVDS drivers nominally provide a 350-mV differential signal, with a 1.25-V offset from ground. These levels are attained when driving a 100-Ω differential line-termination test load. This requirement includes the effects of up to 32 standard receivers with their ground reference up to 1 V different from that of the driver. This common-mode loading limitation of LVDS drivers affects how they are observed and much of the test setup that follows.

The EVM is designed to support the SN55LVCP22 LVDS output device. By using the three power jacks (J3, J4, J5), as well as installing termination resistors (R3-R8 and R11-R16), different methods of termination and probing can be used to evaluate the device output characteristics. The typical setup for the SN55LVCP22 is shown in Figure 3.

![Figure 3. EVM Power Connections for SN55LVCP22 Evaluation - With LVDS Inputs](image)

2.1 Applying an Input

When using a general-purpose signal generator with 50-Ω output impedance, make sure that the signal levels are between 0 V and 4 V with respect to J5, device under test ground (DUT GND), designated as VCC01.

Inputs should be applied to the SMA connectors J8, J9, J10, and J11. Matched cable lengths must be used when connecting the signal generator to the EVM to avoid inducing skew between the noninverting and inverting inputs. The EVM comes with 100-Ω resistors installed across the differential inputs for LVDS termination. The simple 100-Ω terminations do not provide the necessary termination for LVPECL or CML (1) output structures. In order to interface the SN55LVCP22EVM-CVAL with CML or LVPECL drivers, external terminations are required. Figure 4 shows an example termination for LVPECL and CML output structures. Remove resistors R1 and R2 when using the external terminations.

(1) CML is not a standardized physical layer and therefore the output structures and required termination differ from vendor to vendor.
**Setup and Equipment Required**

The use of external resistors creates a significant stub between the termination and the actual device receivers. The user needs to verify that the transition time of the input signal, coupled with the stub length, does not lead to reflection problems. In normal applications, the termination would be placed as close as possible to the device inputs to minimize reflections.

The control lines SEL0 and SEL1 require LVTTL levels and are stimulated by the VCC power supply, via jumpers J1 and J2. Table 1 shows the different functions and the control line settings for each.

### Table 1. Crosspoint Function Table

<table>
<thead>
<tr>
<th>SEL0</th>
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### 2.2 Observing an Output

Direct connection to an oscilloscope with 50-Ω internal terminations to ground is accomplished without R3-R8 installed. The outputs are available at J12-J15 for direct connection to oscilloscope inputs. Matched cable lengths must be used when connecting the EVM to a scope to avoid inducing skew between the noninverting (+) and inverting (-) outputs.

The three power jacks (J3, J4, J5) are used to provide power and a ground reference for the EVM. The power connections to the EVM determine the common-mode load to the device. As mentioned earlier, LVDS drivers have limited common-mode driver capability. When connecting the EVM outputs directly to oscilloscope inputs, setting of the oscilloscope common-mode offset voltage is required, as the oscilloscope presents low common-mode load impedance to the device.

Returning to Figure 3, power supply 1 is used to provide the required 3.3 V to the EVM. Power supply 2 is used to offset the EVM ground relative to the DUT ground. The EVM ground is connected to the oscilloscope ground through the returns on SMA connectors J12-J15. With power applied as shown in , the common-mode voltage seen by the SN55LVCP22 is approximately equal to the reference voltage being used inside the device, preventing significant common-mode current to flow. Optimum device setup can be confirmed by adjusting the voltage on power supply 2 until its current is minimized. It is important to note that use of the dual supplies and offsetting the EVM ground relative to the DUT ground are simply steps needed for the test and evaluation of devices. Actual designs include high-impedance receivers, which do not require the setup steps outlined above.
If the outputs are to be evaluated with a high-impedance probe, direct probing on the EVM board is supported via installation of a 50-Ω resistor across the solder pads for R6 and R8, and another 50-Ω resistor across the solder pads for R3 and R5 for DUT1. Or, LVDS outputs can be observed by installing a 100-Ω resistor at R4, R7, R12, or R15. LVPECL outputs can be observed by installing R3, R5, R11, R13, R14, and R16 (49.9-Ω resistors) and setting power supply #2 to 1.3 V (note that power supply #2 must be able to sink current).

2.3 Typical Test Results

Figure 5 shows typical results obtained with the EVM setup. The DUT was configured to send the IN0+/IN0- inputs to the outputs OUT0+/OUT0- and inputs IN1+/IN1- to outputs OUT1+/OUT1- by setting EN0 and EN1 to a high level and by setting SEL0 to GND and SEL1 to VCC. The stimuli were a $2^{15}-1$ PRBS to J1 and J2 at 1.3 Gbps, and a 650-MHz clock to J3 and J4.

![Figure 5. Typical Test Results of the SN55LVCP22EVM-CVAL](image-url)
Board Layout

Figure 6. Silk Screen

Figure 7. Layer 2 – GND Plane
Figure 8. Layer 3 – PWR Plane

Figure 9. Bottom Layer
4 Schematic and Bill of Materials

The following pages contain the SN55LVCP22EVM-CVAL schematic and bill of materials.

Figure 10. SN55LVCP22EVM-CVAL Schematic
## Table 2. SN55LVCP22EVM-CVAL Bill of Materials

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<th>Manufacturer</th>
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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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