User's Guide
SLLU221–October 2016

SN65DSI83, SN65DSI84, and SN65DSI85 EVM User's Manual and Implementation Guide

This document describes how to use and configure the SN65DSI83, SN65DSI84, or SN65DSI85 EVM. Hereafter in this document, the SN65DSI83, SN65DSI84, and SN65DSI85 devices may be referred to as *SN65DSI8X*.

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1 Overview

1.1 What are the SN65DSI83, SN65DSI84, and SN65DSI85?

The SN65DSI8X is a MIPI DSI-to-LVDS bridge device that supports video modes in the forward direction. The SN65DSI8X is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. Use the SN65DSI8X between a GPU with DSI output and a video panel with LVDS inputs.

All three devices share the same pin out and package.

Table 1 is a summary of the feature sets on these devices:

Table 1. SN65DSI8X Features Summary

Part Name	Description	Max Resolution
SN65DSI83	Single-channel DSI to single-link LVDS	Suitable 1366×768/1280×60 fps at 24 bpp/18 bpp
SN65DSI84	Single-channel DSI to two single-link LVDS	1920×1200 60 fps at 24 bpp/18 bpp
SN65DSI85	Dual-channel DSI to two single-link LVDS	2560×1600 60 fps, 1920×1080p 120 fps at 24 bpp /18 bpp

NOTE: Each DSI channel has 4 DSI data lanes + 1 CLK lane. Each LVDS link has 4 data lanes + 1 CLK lane.

1.2 What is the SN65DSI8X EVM?

The SN65DSI8X EVM is a PCB created to help customers implementing SN65DSI83, SN65DSI84, and SN65DSI85 in system hardware. This EVM can be used as a hardware reference design for any implementation using the SN65DSI8X. The SN65DSI8X EVM is designed for use across all three versions of the DSI bridge devices - SN65DSI83, SN65DSI84, and SN65DSI85. PCB design and layout files are provided upon request to aid PCB design with a SN65DSI8X component. The layout files are used as a guideline to implement the SN65DSI8X with illustrations of the routing and placement rules. Please note that the EVM design includes test components to evaluate the SN65DSI8X which may not applicable for production.

This EVM includes on-board connectors for DSI input and LVDS output signals. These connectors connect MIPI DPHY-compliant DSI source and LVDS panels to the EVM. Refer to Section 2.1 and Section 2.2 for more information on the connectors.

CAUTION

A custom translator cable or card is required if this EVM is to be utilized for the evaluation of an implementation from the customer. Any other method of connecting to any DSI source or LVDS panel is not supported by this EVM. TI is not responsible for any issues or problems that may occur as a result of using connection methods other than what is recommended in this document.

NOTE: Some portions and components in the EVM or in this document may include the references to SN65DSI85 instead of addressing all three part numbers. The SN65DSI85 is replaceable with SN65DSI83 or SN65DSI84.

1.3 What is Included in the SN65DSI8X EVM?

The major components of the EVM follow:

- SN65DSI83, SN65DSI84, or SN65DSI85
- Backlight driver via J2 and J5
- Samtec QSH-type connectors on DSI and LVDS interfaces
- Hirose-type connector on DSI Ch A interface
- IPEX-type connectors on LVDS interfaces
- I^2C programming interface for external I^2C host connection

1.4 What Does This EVM Look Like?

Figure 1 illustrates the EVM.

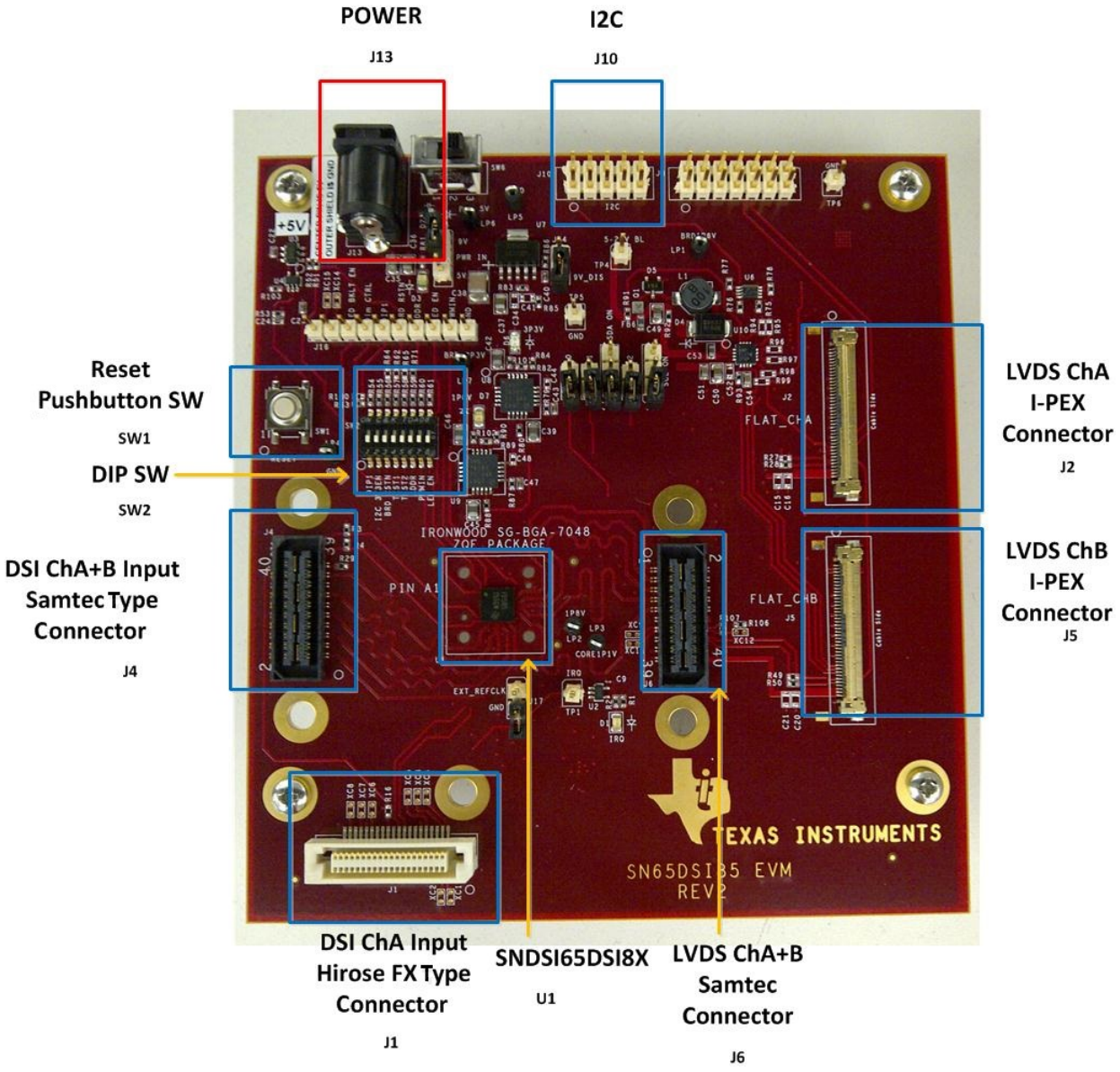

Figure 1. SN65DSI8XEVM

2 Hardware Description

Figure 2 shows the EVM block diagram.

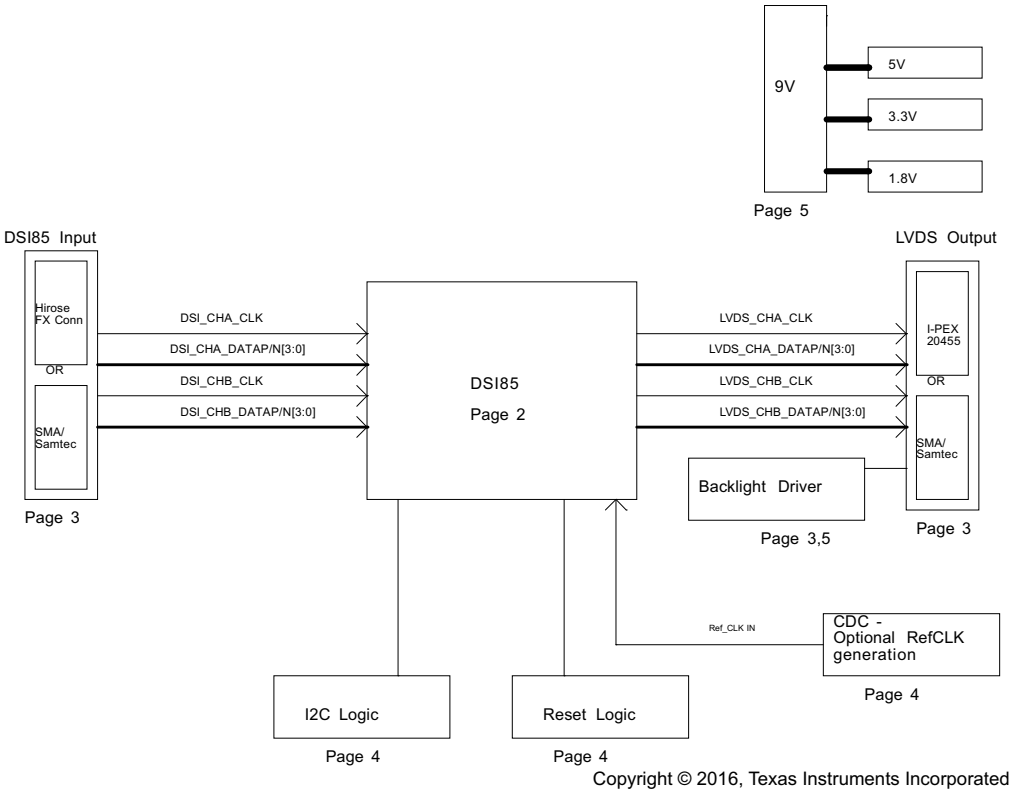

Figure 2. SN65DSI8X EVM Block Diagram

2.1 Connectors for DSI8X Input Ports

The EVM has two input options for DSI video. If a custom breakout board is to be designed using these options, a schematic and an allegro PCB symbol for either connector is provided by TI upon request.

(A) **J4 - Samtec QSH-type connector (P/N QSH-020-01-H-D-DP-A)**

J4 is a Samtec QSH-type connector that can be mated with a matching QTH-type connector on the top. It provides DSI input connections to both DSI Ch A and Ch B signals. It also provides access to I^2C and other miscellaneous signals such as IRQ. XC connections are open vias just in case there is a need for connection to other signals. The mating connector part number is QTH-020-01-H-D-DP-A. For an SMA-type connection, use the Samtec HDR-128291-XX breakout board. The HDR-128291-XX is a breakout board with a mating connector to J4 and standard SMA male connectors via cables. More information on this breakout board is provided upon request.

(B) **J1 – Hirose FX-type connector (P/N FX6A-40S-0.8SV2)**

J1 is a Hirose FX-type connector that can be mated with a matching FX plug on the top. The part number for the mating connector is FX6A-40P-0.8SV2. J1 provides DSI input connection only to the DSI Ch A signals. It also provides access to I^2C and other miscellaneous signals such as IRQ.

2.2 Connectors for DSI85 Output Ports

There are two output port options available on the EVM for the LVDS output signals. If a custom breakout board is to be designed using these options, a schematic and an allegro PCB symbol for either connector can be provided by TI.

(A) **J6 - Samtec QSH-type connector (P/N QSH-020-01-H-D-DP-A)**

J6 is a Samtec QSH-type connector that can be mated with a matching QTH-type connector on the top. It provides DSI input connections to both LVDS Ch A and Ch B signals. It also provides access to

the backlight power and its related signals. XC connections are open vias, in case there is a need to connect to other signals. The mating connector part number is QTH-020-01-H-D-DP-A. For an SMA-type connection, use the Samtec HDR-128291-XX breakout board. The HDR-128291-XX is a breakout board with a mating connector to J6 and standard SMA male connectors via cables. More information on this breakout board is provided upon request.

(B) **J2 and J5 – I-PEX-type connectors (P/N 20455-040E-12)**

J2 and J5 are I-PEX connectors widely used in LCD video panels with LVDS receivers. Connect J2 and J5 via an SGC-type cable with one-to-one pin mapping to a panel using the I-PEX20455-040E-12 connectors. J2 connects to the LVDS Ch A signals while J5 connects to the LVDS CHB signals.

2.3 I²C

Access to I^2C signals are provided via DSI input connectors J1 and J4 (as mentioned in Section 2.1) or J10. Note that I^2C signal levels should be at 1.8 V when the I^2C interface is accessed through connectors J1 or J4. A 3.3-V to 1.8-V voltage translation is provided when an I^2C host is connected through J10.

A stand-alone external I^2C host can be connected via J10 to debug.

2.4 Enable or Reset

There are three device enable or reset options to use with the EVM:

(A) **Supervisor circuitry option**

This is a default configuration. The enable (EN) signal is held low until the power good (PG) from the 1.8-V voltage regulator reaches a stable high voltage level, then it is released high.

(B) **RC timing option**

The C10 external capacitor and internal resistor are used to control the EN ramp time after the device is powered on. C10 is a DNI (Do Not Install option), by default. C10 needs to be installed and R52 needs to be uninstalled to enable this option.

(C) **External control option**

A push button (SW1) or a DIP switch (SW2.3) is available for the manual control of the EN signal. Install R64 to enable the DIP switch option.

2.5 Power

A 5- to 6-V power supply will operate the SN65DSI8X EVM. A plug to accept a 5- to 6-V wall power adapter is provided on the EVM (J13). The jumper on position 1-2 of J15 should be placed while J14 is left open. This should be the default configuration when the board is shipped.

The EVM is designed to accommodate up to maximum of 1.5 A current. The current consumption of the board without backlight driver enabled is about 70 mA + SN65DSI85 device power. The SN65DSI85 consumes about 50 mA at power on, approximately 80 mA to approximately 200 mA, depending on the system configuration. The total power consumption of the board could vary depending on LCD panels when the on-board backlight driver is used. When an LCD panel consumes more current than 1.5 A minus 70 mA + SN65DSI85 device power, an external backlight source should be used.

NOTE: Do not plug in any power source higher than the configured voltage (5 V or 6 V).

2.6 Backlight Driver

The SN65DSI8X EVM incorporates the LED backlight driver circuitry using the TI backlight driver device TPS61181A enabling use of the on-board backlight driver source. The default configuration of the EVM enables the on-board backlight driver.

If the external backlight driver is used, a connection is available via J3. Uninstall FB6 if external backlight driver is used.

2.7 Reference CLK Programmability

The SN65DSI8X EVM incorporates a programmable CLK circuitry using a TI-programmable device, CDCEL913. The output of the CDCEL913 is connected to the reference CLK of the SN65DSI8X. The default frequency of the reference CLK is 27 MHz. The CLK can be programmed via I^2C signals brought out to on-board connectors J9, J12, or J10. When J10 is used, place jumpers on J9 and J12. The reference CLK can be pre-programmed to a desired value, if requested prior to shipping.

2.8 DIP Switch Configuration

A DIP switch is provided to operate the device or EVM in different configurations. When the switch is in an open position, the corresponding signal is tied high. When the switch is in the ON (closed) position, the corresponding signal is tied to GND.

The signals in the greyed out region are not enabled unless a corresponding resistor is installed.

Table 2. DIP Switch Setting

DIP SW No	Signal Name	Description	Default Configuration	
			Open(Off) HIGH	Closed(On) LOW
SW2-1	DIP1 – Dimming CTRL or LED_BKLT_EN	Controls LED backlight driver enable in default configuration. Installing R100 and uninstalling R63 enables control on dimming control of the backlight driver. Always switch back to closed (ON) position prior to unplug or plug operation of the panel.	x	
SW2-2	I2C_3V3EN	Enables 3.3-V voltage translator for the I^2C signals	x	
SW2-3	BRD_RSTN	Controls the EN/RESET signal of the SN65DSI8X high or low	x	
SW2-4	RSVD1	Reserved		x
SW2-5	RSVD2	Reserved		x
SW2-6	ADDR	Controls the ADDR signal of the SN65DSI8X high or low	x	
SW2-7	PWMIN	Controls the PWMIN of J6 high or low	x	
SW2-8	LED_EN	Controls the LED_EN of J2 or J5 high or low This switch should be toggled high to enable the LED of the connected panel. Always switch back to closed (ON) position prior to unplug or plug operation of the panel.		x

3 Quick Start Guide

Quick-start instructions are provided in the following list:

1. Plug in a DSI source to J4
2. Plug in a LVDS video sink device on J2, J5 or J6
3. Plug in an I^2C host on J10 if an external I^2C host is used.
4. Make sure the DIP switch setting is in a correct configuration.
5. Apply power to the EVM. The following LEDs should light up: D3, D6, and D7. D1 may light up depending on the configuration.
6. Start video streaming on the DSI input
7. Configure the device for the desired mode of operation via I^2C. Video output should be observed after configuration is complete.

Figure 3 depicts the setup using an external I²C host, Samtec-to-SMA breakout board (HDR-128291-XX) for DSI ChA input and a 1024×600 video panel over an I-PEX connector.

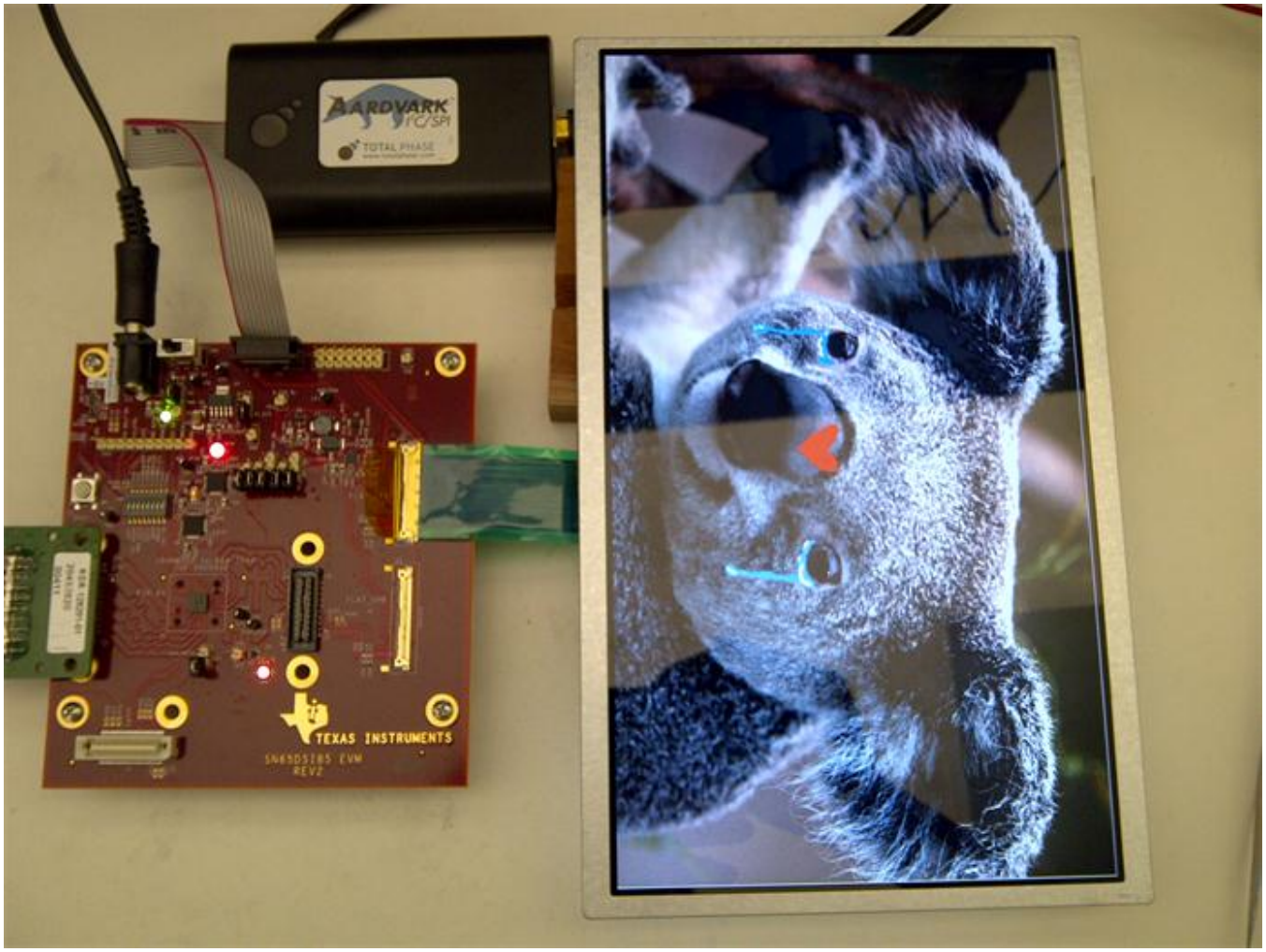

Figure 3. DSI EVM Example Setup

4 References

1. SN65DSI8X Datasheets (SN65DSI83 SLLSEC1), (SN65DSI84 SLLSEC2), (SN65DSI85 SLLSEB9)

5 EVM Schematics

Figure 4 through Figure 7 illustrate the EVM schematics.

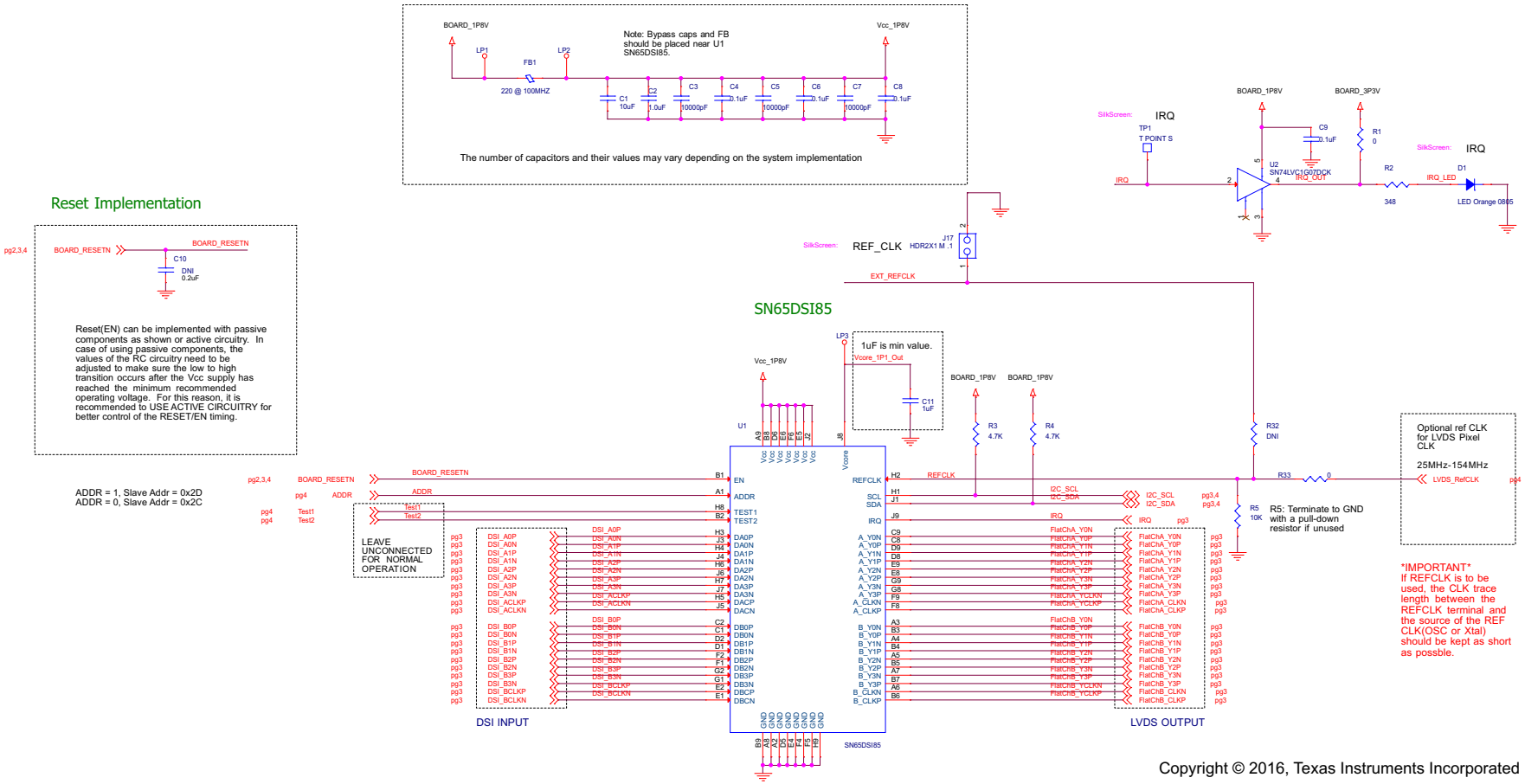

Figure 4. SN65DSI8X Schematic 1

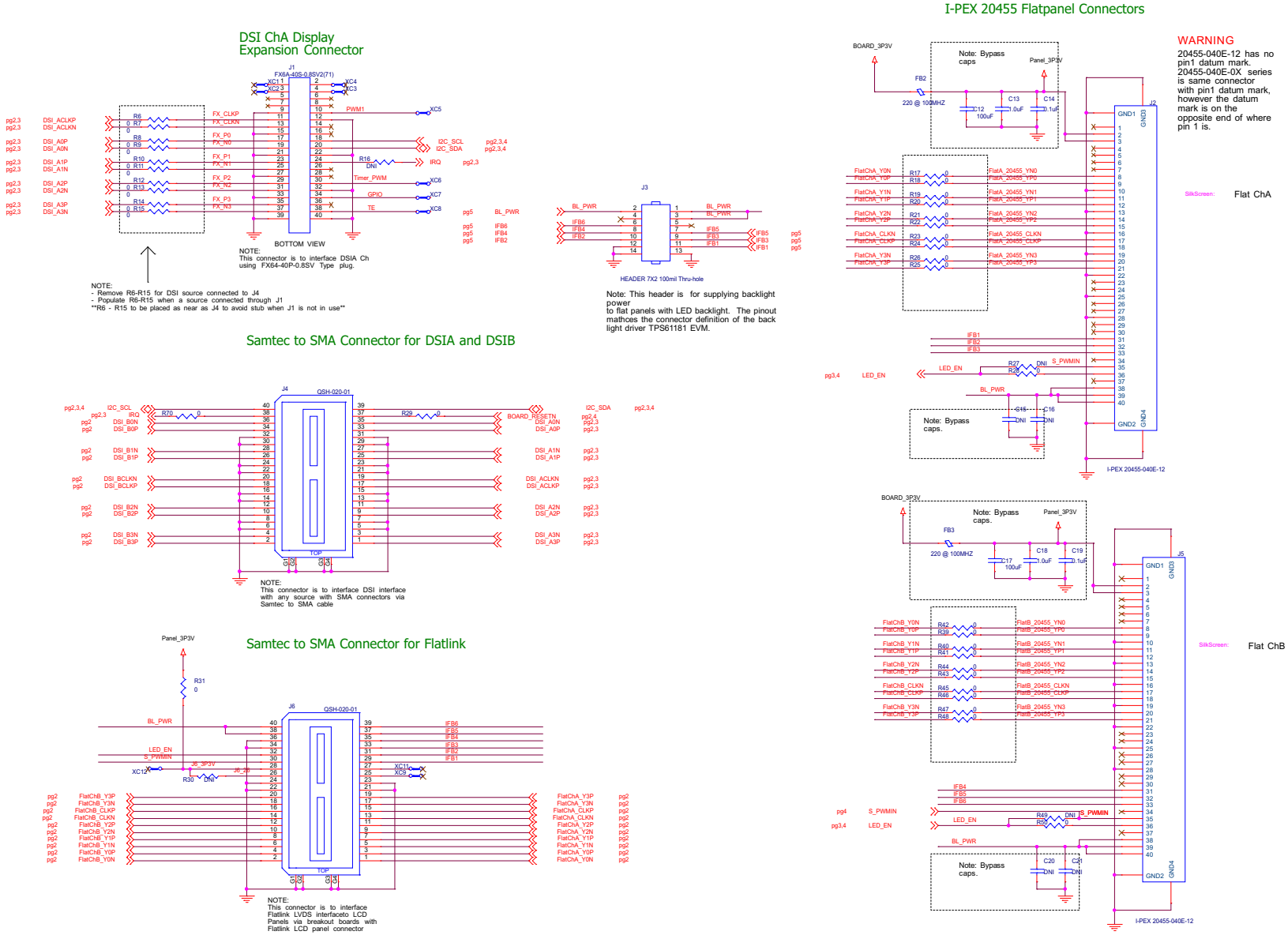

Figure 5. SN65DSI8X Schematic 2

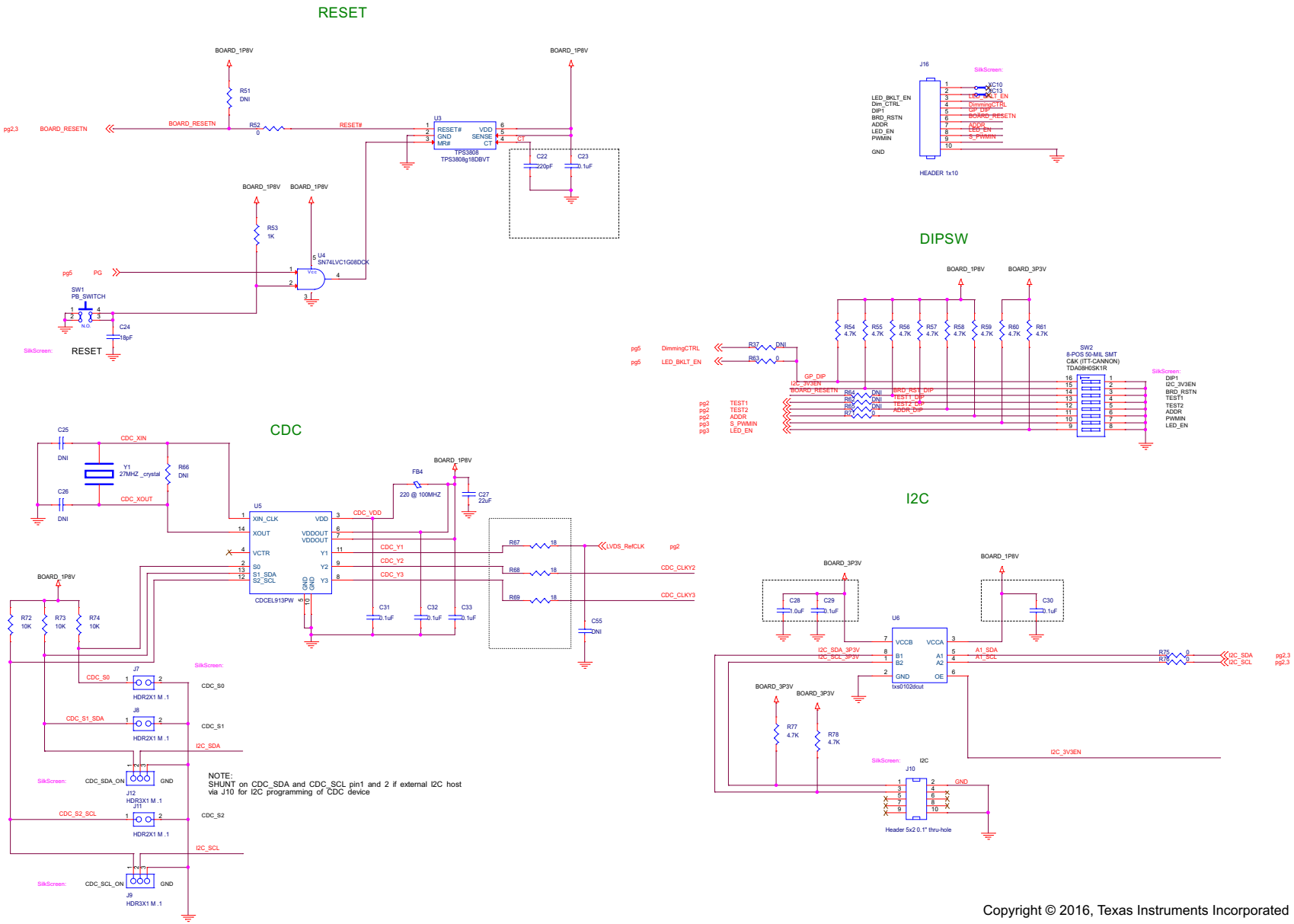

Figure 6. SN65DSI8X Schematic 3

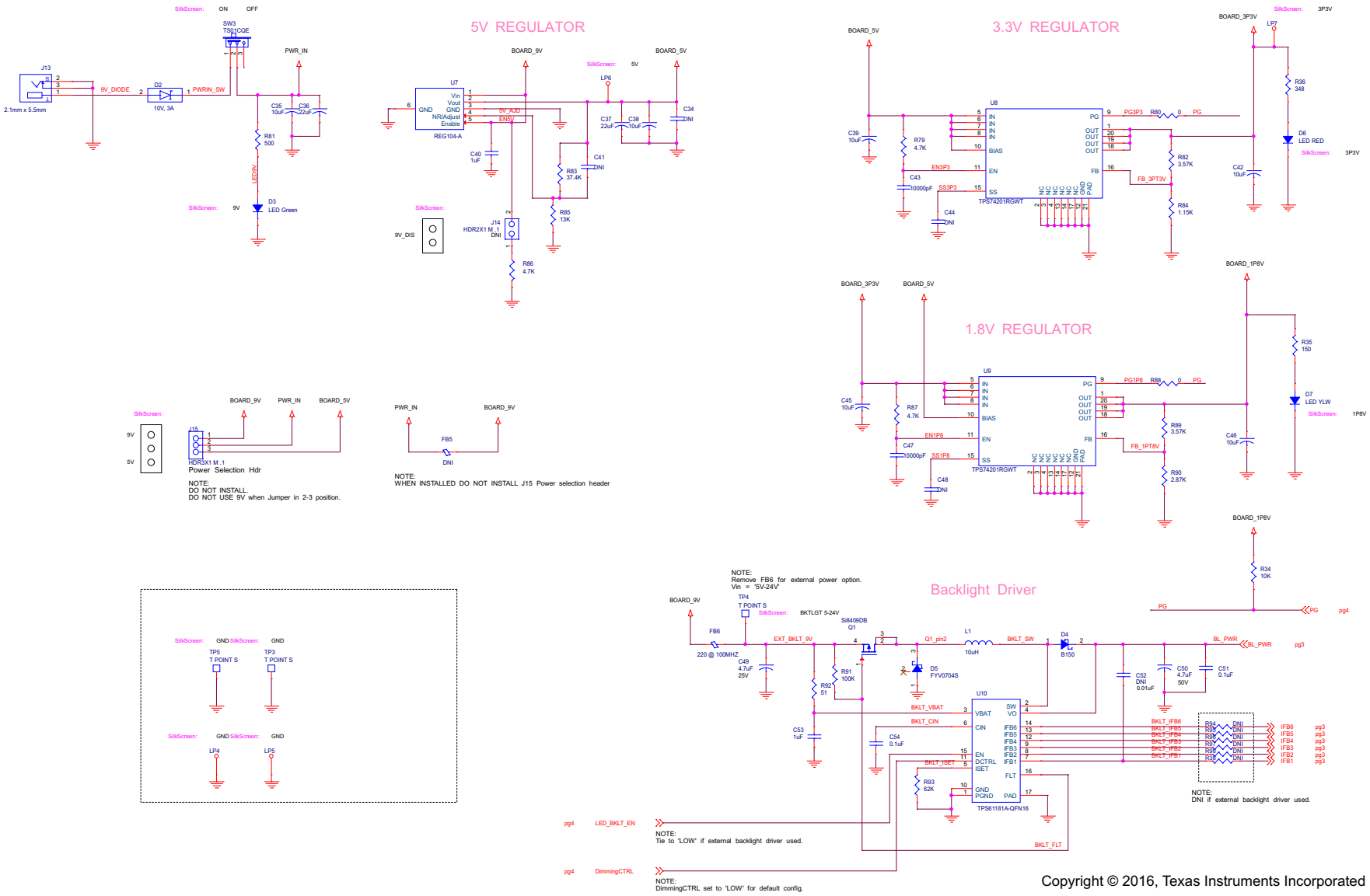

Figure 7. SN65DSI8X Schematic 4

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      CAUTION

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      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

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This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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