User’s Guide

ISO672x Dual-Channel Digital Isolator Evaluation Module

ABSTRACT
This user’s guide describes the ISO672x dual-digital isolator evaluation module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the TI dual-channel digital isolators in an 8-pin SOIC package.

CAUTION
This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0-V to 5.5-V recommended operating range.

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1 Introduction

This user’s guide describes EVM operation with respect to the ISO672x dual-channel digital isolators. However, the EVM may be reconfigured for evaluation of any of TI’s dual-channel digital isolators in an 8-pin SOIC package. This guide also describes the available channel configurations within the ISO6721 family, the EVM schematic, and typical laboratory setup. A typical input and output waveform is also presented.

2 Overview

The ISO672x is TI’s new digital isolator family capable of galvanic isolations up to 3000 V\textsubscript{RMS}. These isolators provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The ISO672x digital isolators have logic input and output buffers separated by a silicon oxide (SiO\textsubscript{2}) insulation barrier. Used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with, or damaging sensitive circuitry.

3 Pin Configurations of the ISO672x Dual-Channel Digital Isolators

Figure 3-1 shows the ISO672x dual-channel digital isolator pin configurations.

![Figure 3-1. Dual-Channel Digital Isolator Pin Configurations](image-url)
4 ISO6721 Board Block Diagram and Image

Figure 4-1 shows the board configuration for evaluation of the ISO6721 dual-channel digital isolator.

![ISO6721 EVM Configuration](image)

Figure 4-1. ISO6721 EVM Configuration

Figure 4-2 shows the 3D diagram of the EVM.

![ISO6721DEV 3D Diagram](image)

Figure 4-2. ISO6721DEV 3D Diagram
5 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 5-1 shows the configuration for operating the ISO6721 dual-digital isolator EVM using two power supplies.

![Figure 5-1. Basic EVM Operation](image)

Figure 5-2 shows typical input and output waveforms of the EVM for a 1-MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

![Figure 5-2. Typical Input and Output Waveform](image)
6 Bill of Materials

Table 6-1 shows the bill of materials (BOM) for this EVM.

<table>
<thead>
<tr>
<th>Item</th>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Quantity</th>
</tr>
</thead>
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<tr>
<td>1</td>
<td>C1, C4</td>
<td>CAP, CERM, 10 µF, 35 V, ± 10%, X5R, 0805</td>
<td>MuRata</td>
<td>GRM21BR6YA106KE43L</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>C2, C5</td>
<td>CAP, CERM, 1 µF, 50 V, ± 10%, X5R, 0603</td>
<td>MuRata</td>
<td>GRM188R61H105KAALD</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>C3, C6</td>
<td>CAP, CERM, 0.1 µF, 25 V, ± 5%, X7R, 0603</td>
<td>AVX</td>
<td>06033C104JAT2A</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>H1, H2, H3, H4</td>
<td>Bumpon, Hemisphere, 0.44 X 0.20, Clear</td>
<td>3M</td>
<td>SJ-5303 (CLEAR)</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>J1, J2</td>
<td>Header, 100mil, 4x2, Gold, SMT</td>
<td>Molex</td>
<td>15910080</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8</td>
<td>Test Point, Miniature, SMT</td>
<td>Keystone</td>
<td>5019</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>U1</td>
<td>Robust EMC, Low Power, Dual-Channel Digital Isolators, D0008B (SOIC-8)</td>
<td>Texas Instruments</td>
<td>ISO6721BQDRQ1</td>
<td>1</td>
</tr>
</tbody>
</table>

7 EVM Schematics and Layout

The ISO6721DEVM is designed to accommodate any of the ISO672x dual-channel devices in an 8-pin package. To evaluate any of the ISO672x dual-channel devices in an 8-pin package, replace ISO672x with the device of interest on the ISO6721DEVM PCB. No other component requires any modification. Figure 7-1 shows the ISO672x EVM schematic and Figure 7-2 shows the printed-circuit board (PCB) layout.

Figure 7-1. ISO6721DEVM EVM Schematic
Figure 7-2. PCB Layout

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