TAS54x4C Design Guide

The TAS5414C-Q1 and TAS5424C-Q1 devices are 4-channel class-D amplifiers in one integrated circuit (IC). The devices were developed for automotive use and are qualified in accordance with the AECQ100 specification. When designing the control code to operate the TAS5414B, TAS524B, TAS5414C, TAS5424C, and TAS5412 devices through I^2C, the unique device characteristics must be taken into account for proper system function. This design guide includes software development guidelines as well as hardware instructions to provide the necessary circuit topologies and part types to meet strict OEM-audio specifications and the EMI standards of CISPR25.

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1 TAS54x4C Hardware Design Guidelines

When designing an audio amplifier with the TAS5414C and TAS5424C class-D integrated devices, the details of the full system design are not included in the data sheet. This design guide supplements the data sheet with detailed hardware-related information on designing an audio amplifier product.

1.1 Circuit Design

1.1.1 Input

The input stage of the TAS5414C devices is single ended. The TAS5424C input stage is either differential or balanced. The audio input pins have a bias voltage of 3.25 VDC with a tolerance of 2.8 VDC to 3.7 VDC. Therefore direct coupling to the input pins is not possible. An input coupling capacitor must be used. The value of the capacitor is based on two criteria. The value of the capacitor must be large enough to pass low frequencies, but not so large that the charge time on this capacitor is too long which can cause pop and click noise at the output of the amplifier.

The input impedance of each input pin is 80 kΩ ±20 kΩ. Use Equation 1 to calculate the low-frequency cutoff frequency (–3 dB).

$$f_{co} = \frac{1}{2 \times \pi \times R \times C} \quad (1)$$

where

- f_{co} = cutoff frequency in Hertz
- R = 80 kΩ
- C = coupling capacitor

The recommended capacitor values for the TAS54x4C devices are 0.47 µF or 1 µF. For a 0.47 µF capacitor with 20% tolerance the highest cutoff frequency can be calculated using 60 kΩ and 0.38 µF. The worst-case cutoff frequency for this example is 7.1 Hz which allows for flat gain in the audio band.

The common mode rejection ratio, CMRR, is also affected by the input circuit. The balanced inputs of the TAS5424C must have equal-value capacitors so that the CMRR is maximized at lower frequencies.

The single-ended input of the TAS5414C must also have the proper input capacitors for good low-frequency common-mode performance. Because all four IN_P channels in the TAS5414C device share the IN_M pin, the capacitor from IN_M to ground should be close to the sum of the capacitors on the four IN_P pins. Additionally, a resistor in series with the IN_M capacitor should be placed between the IN_M pin and ground that is equal to the parallel equivalent of the input series resistance on all IN_P channels combined, including the output resistance of the DAC. For example, if 1-kΩ of series input resistance is on each channel of the TAS5414C, a 250-Ω resistor should be placed between the IN_M pin and GND in series with the IN_M capacitor. Following these guidelines will optimize noise performance. Figure 1 shows an example input circuit that follows this practice.

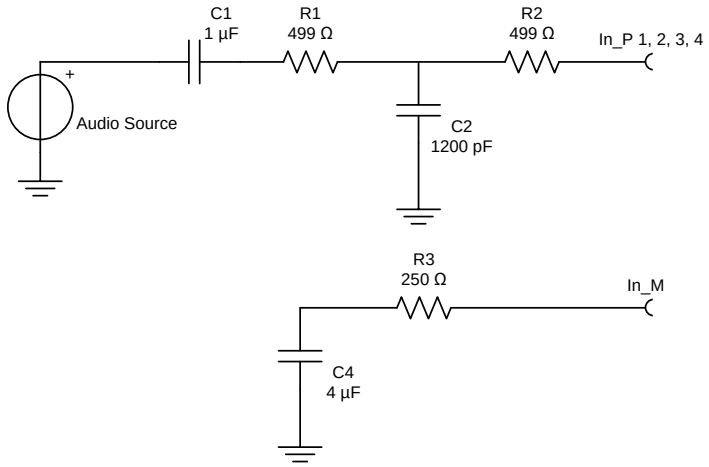


Figure 1. TAS5414C Input Circuit

During the turn-on of the amplifier, the input coupling capacitors must charge to the common mode voltage of 3.25 VDC. If the amplifier is passing a signal during this time, the speakers can have large excursions, pops, and click. The TAS54x4C devices have a precharge resistor on the inputs to quickly charge the coupling capacitors. After the capacitor is charged, the resistor is taken out of the circuit and the 80 kΩ resistor is in place. This worst-case value of the precharge resistor is 600 Ω. Equation 2 calculates the charge time using the worse case value from the example in Figure 1 of 1.2 µF and 600 Ω.

$$V_{I(x)} = V_{I(x)}max \times (1 - e^{-t / RC}) \quad (2)$$

The input capacitors should have good audio qualities as the audio input signal to the amplifier passes directly through it. A good-quality capacitor can be a film type or a very-low leakage electrolytic. Ceramic capacitors can be used, but can degrade the sound quality. Low leakage on the capacitor is important for low direct-current (DC) offset at the output of the amplifier. The TAS54x4C amplifiers provide gain at DC. Any leakage current will flow through the 80-kΩ input impedance and cause a small DC offset between the input pins. This small DC offset will be amplified by the gain setting.

1.2 I²C Communication

Three pins are associated with the I²C communication protocol. Both devices have the clock pin (SCL) and the data pin (SDA), while the address selection pin is labeled I2C_ADDR on the TAS54x4C devices.

1.2.1 Device Address Selection

The TAS54x4C devices have the capability of using four different I²C addresses. The devices in this family share the same I²C device addresses which allows for up to four TAS5414C and TAS5424C devices to be controlled by one I²C controller without I²C bus switches. The I²C address is determined by the DC voltage present on the address selection pin. The I²C-address pin voltage is sensed when the device is released from standby mode. This voltage is then latched at 300 µs. Therefore, any noise or voltage glitch cannot change the I²C address during operation. Because this pin latches when released from standby, a capacitor is not necessary on this pin. The charge time on the capacitor may cause an incorrect I²C address.

NOTE: Do not confuse the master-slave notation with a master-slave I²C.

A slave device must have an external oscillator connected to the OSC_SYNC pin (see Section 1.3.1).

Table 1. Oscillator Configuration and I²C Addresses

OSCILLATOR CONFIGURATION	I2C_ADDR PIN CONNECTION	I²C ADDRESS
Master	To SGND Pin	0xD8, 0xD9
Slave 1	35% DVDD (resistive voltage divider through D_BYP Pin and SGND Pin)	0xDA, 0xDB
Slave 2	65% DVDD (resistive voltage divider through D_BYP Pin and SGND Pin)	0xDC, 0xDD
Slave 3	To D_BYP Pin	0xDE, 0xDF

1.2.2 I²C Communications

The SDA and SCL pins communicate with an I²C controller. The SDA pin carries the data and the SCL pin carries the clock. The TAS54x4C devices are I²C slave-only devices. The device cannot start I²C transactions and cannot generate an I²C clock. The SCL pin is set for input signals only, whereas the SDA pin is bidirectional. The TAS54x4C devices send data when the I²C controller sends a read command. The SDA and SCL pins require pullup resistors to 3.3 VDC or 5 VDC because these pins are 5 VDC tolerant. A resistor value of 4.7 kΩ can be used for proper operation. The resistor value should be adjusted to the number of devices on the I²C bus according to the I²C specification.

The TAS5414C and TAS5424C devices have the capability to receive and send sequential data. All registers can be read sequentially except the fault registers. All registers with write capabilities can be written sequentially.

1.2.3 I²C Register Details

The TAS54x4C devices have several different types of registers. These registers can be broken into four basic categories: fault registers (0x00 to 0x01, 0x13), load diagnostic registers (0x02 to 0x03), status registers (0x04 to 0x07), and control registers (0x08 to 0x0D, 0x10).

The fault registers report any faults that occurred in the device. If the fault is no longer present when the register is read, the register will still report that a fault occurred in the past because these registers are latched. The registers will only clear the fault after the fault has cleared and being read.

The load diagnostic registers report the results of load diagnostics that are performed. These registers are also latched and will clear when a successful load diagnostic is run.

The status registers report the current status of the device including faults and the operational mode of each channel. These registers are not latched and report the present state in the device at all times.

The control registers allow the system to modify the settings of the device. Note that some settings may only be changed in hi-Z.

See Section 2 for more information about the proper usage of the registers.

1.3 Oscillator

The TAS54x4C devices incorporate an internal oscillator to provide all the necessary clocks and the output PWM switching clock. The oscillator frequency is set by the current on the REXT pin. The current is set by placing a resister between REXT and ground. The value of the resistor should be 20 kΩ with a tolerance of 1% for proper operation of the IC. This value sets the frequencies correctly as stated in the data sheet of the device.

The internal oscillator is 20 MHz which is then divided by 5 for 4 MHz, 6 for 3.33 MHz, or 7 for 2.85 MHz. These three frequencies synchronize the ICs and are present on the OSC_SYNC pin. This oscillator is then divided again by 8 to provide 500 kHz, 417 kHz, and 357 kHz switching frequency options. The divide ratio is set through the I²C.

1.3.1 Oscillator Synchronization

Some designs require more than one TAS54xx device. As previously mentioned in Section 1.2, one I²C bus can have up to four separate devices. One device is considered the master and the other devices are considered the slaves. The master provides an oscillator clock on the OSC_SYNC pin and the slave devices require an oscillator input on the OSC_SYNC pin. All devices are synchronized to avoid beat frequencies in the audio spectrum. If the clock is lost on the slave, the internal watchdog places the outputs into hi-Z.

To synchronize the devices, use the following procedure:

1. Bring all the devices out of standby and into hi-Z mode
2. Send the I²C command on the clock master to place the clock signal on the OSC_SYNC pin. Bit 7 in register 0x0B must be set to 1.

   The slave devices are not allowed to enter play mode until the master has sent a clock

For phase synchronization of the devices which minimizes harmonic crosstalk between devices, use the previous method to synchronize the devices and add these I²C commands after step 2:

1. Place the slave devices in sync-receive mode by changing bit 6 in register 0x0A.
2. Send a sync pulse from the master device by changing bit 6 on register 0x0A.

   Bit 6 automatically clears when the synchronization is complete on both the master and slave devices.

Phase synchronization applies to the switching phase and not the audio phase because the audio phase is always aligned. The inverter allows a new sync pulse between each of the devices to align the 45° or 180° switching phases.

To summarize, two options occur between the OSC_SYNC pin and synchronization of the devices.

1.3.1.1 Option 1: 45° Phase

Option 1 includes the following features:

- Eight switching phases in each output cycle (0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°)
- Device 1 switching phase: 0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°
- Device 2 switching phase: 22.5°, 67.5°, 112.5°, 157.5°, 202.5°, 247.5°, 292.5°, 337.5° (offset by 22.5° which is half of the switching phase)
- The best EMI performance out of all the options (16 switching phases per output cycle allows for more energy distribution)
- Reduced harmonic crosstalk because there is no 90° offset phase, but the performance of Option 2 is better

1.3.1.2 Option 2: 180° Phase

Option 2 includes the following features:

- Two switching phases in each output cycle (0° and 180°)
- Device 1 switching phase: 0° and 180°
- Device 2 switching phase: 90° and 270° (offset by 90° which is half of the switching phase)

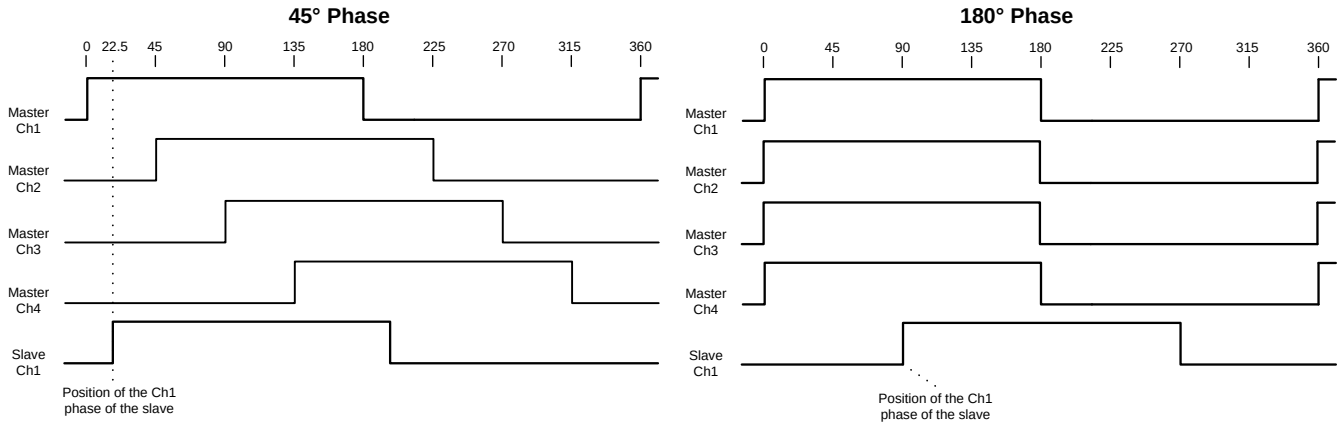


Figure 2. Clock Synchronization Options

NOTE: The PCB layout for the OSC_SYNC should be a direct route or the shortest route from the master to slave devices for best operation. A star connection is preferred instead of a daisy chain.

The REXT resistor that sets the 20-MHz oscillator must still be used in the slave devices. The 20-MHz oscillator is still needed to derive the clock for the internal state machine.

The REXT pin is sensitive. Caution should be used when taking any measurements at this point. Measurements should be taken with high impedance and low capacitance methods, because micro amperes of current can change the performance of the TAS54x4C devices.

An external oscillator can also be used to drive one or many TAS54x4C devices in a system. The oscillator must have a frequency between 2.85 MHz and 4 MHz to maintain proper functionality. To use all four I^2C addresses in a system and an external clock, a special I^2C register bit is available that allows the master address to use an external clock. In register 0x0B, set bit D6 to 1.

1.3.2 AM Mitigation

A potential issue in a radio is that a switching power supply or a switching amplifier may interfere with the AM radio reception. The interference is typically a tone that is found at a harmonic of the PWM frequency. The AM mitigation system provides a method to change the PWM switching frequency using I^2C commands. The controller that provides the I^2C commands would require the AM frequency information so that the correct PWM frequency could be selected. No noise, clicks, or pops occur during the frequency change so the frequency can be changed while audio is present. Table 2 lists the recommended switching frequencies and shows that the harmonics fall outside the associated AM frequency band which avoids tones in the AM band.

Table 2. Recommended Switching Frequencies for AM Mode Operation

US		EUROPEAN	
AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)	AM FREQUENCY (kHz)	SWITCHING FREQUENCY (kHz)
		522 to 540	417
540 to 917	500	540 to 914	500
917 to 1125	417	914 to 1122	417
1125 to 1375	500	1122 to 1373	500
1375 to 1547	417	1373 to 1548	417
1547 to 1700	357	1548 to 1701	357

1.3.3 Spread Spectrum Oscillator

Situations occur where the AM-tuned frequency is not available in the system. In these situations potential interference can be overcome by creating an oscillator that varies slightly over time which is typically called spread spectrum or dither. The oscillator in the TAS54x4C devices can be dithered by changing the current in the REXT pin. The current in the REXT pin can be varied by up to ±2.5% of the nominal value without sacrificing functionality. This variation moves the oscillator frequency enough to avoid the AM receiver from locking on the frequency and producing a tone. The next design characteristic for dither is to determine the dither frequency or how fast the REXT pin current changes. Any change in the PWM frequency is demodulated as an output signal. Because the TAS54x4C devices have feedback this change is reduced by the amount of feedback in the amplifier. The TAS54x4C devices have the greatest amount of open loop gain at DC and will therefore have the greatest amount of feedback at DC. Obviously, DC cannot work, so using a frequency close to DC, but not so low the AM interference is not eliminated. Testing proves that 15 to 20 Hz is a good frequency. The optimum dither oscillator shape is a triangle wave. The dithered oscillator tracks the voltage change of this low frequency oscillator. The linear ramps with the abrupt changes of a triangle wave will provide the best spread spectrum oscillator.

The EMI measurements can be improved with spread spectrum oscillators. The results vary depending on the type of measurement. Peak measurements typically do not show any improvements in the measurements, but quasi-peak measurements may improve the EMI by 6 to 10 dB.

1.4 Output

Class D amplifiers require special consideration when working with the output stages. These amplifiers require a proper demodulation filter in order to recover the audio signal with a flat frequency response. In the TAS54x4C devices the output stages are BTL so the demodulation filter must be a fully balanced filter. Another issue regarding the recovery of a quality audio signal is overshoot on the PWM signal. Overshoot can be reduced using snubbers.

1.4.1 Snubbers

A snubber is an RC network placed at the output of the amplifier to perform several tasks. The snubber will damp any ringing or overshoot on the PWM output waveform. Overshoot can over voltage stress the MOSFETs. The overshoot and ringing are also potential sources of EMI. The overshoot and ringing are caused by the stray inductance in the IC leads, IC bondwires, and PCB traces. The current stored in these inductances must have a low impedance drainage path to ground. If a path is not provided the stored current will find a path through parasitic capacitance on the PCB and cause the overshoot and ringing.

Another property of the snubber is the reduction of the total harmonic distortion (THD) of the amplifier. The overshoot and ringing at the output is present in the feedback signal to the amplifier. The amplifier must then try to eliminate this overshoot and ringing from the signal. The amplifier cannot completely remove this signal which is then present on the output as distortion.

To calculate the proper output snubber, measure the voltage spike at the output pin. Use section 4 in *Voltage Spike Measurement Technique and Specification*, SLEA025, as a reference on performing this measurement.

Figure 3 shows the basic output circuit. A bypass capacitor, $C_{(BYPASS)}$, must be included in the design because it is part of the current path for snubbing the inductance of the high-side FET. The terminals of $C_{(BYPASS)}$ must be close to the PVDD pins and the PGND pins of the IC. R*x* and C*x* should be close to the output pin and the PGND pins of the IC. This necessary to reduce the series inductance of the PCB traces. The current loops that are formed by R*x* and C*x* are labeled in Figure 3 as *High-side FET current-loop* and *Low-side FET current-loop*. If R*x* and C*x* are not present, the current stored in the drain, source, and lead inductances have no place to sink to during dead time. This current then flows through parasitic capacitances on the PCB and appears on the waveform as ringing. Good control of the high-side and low-side current loops is necessary for good over-voltage protection because of spikes and for good EMI results.

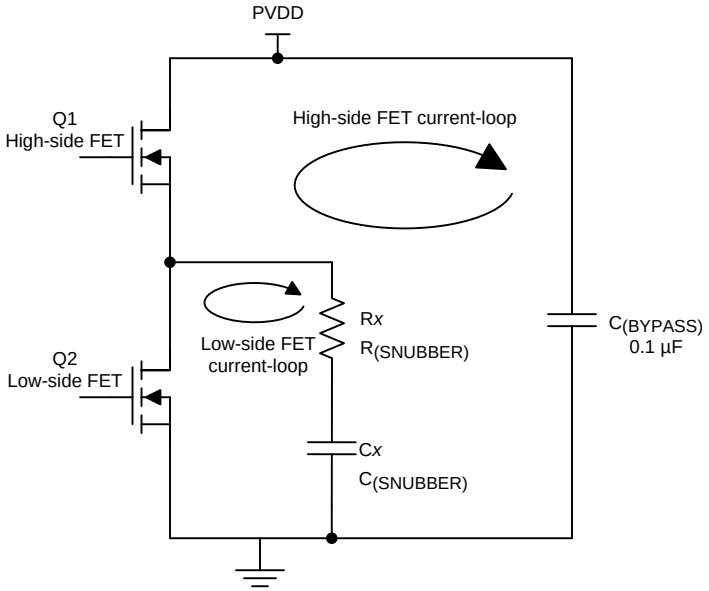


Figure 3. One-Half of the Typical Output Stage With Snubbers

Use a value of R*x* that is a little higher than the estimate value. A good starting R*x* value for the TAS5414C and TAS5424C device is 10 Ω. Use surface mounted devices (SMD) because the series inductance (ESL) is low.

For C*x* select a small value of 470 pF to 1000 pF. Also use SMD parts. Use the techniques listed in this design guide to measure the spike and the associated ringing. Measure the frequency of the ringing. If there is no ringing, use a higher value resistor for R*x* or a smaller capacitor for C*x*. The final C*x* should be labeled as C1 and the ringing frequency is $f1$.

Change C*x* to a value that is about 1.5 to 2 times the previous value. Keep R*x* the same. Again, measure the frequency of the ringing on the waveform. If no ringing is available to measure, change C*x* to a slightly smaller value. The value of C*x* should be labeled as C2 and the ringing frequency is $f2$.

Use Equation 3 to calculate the value for L.

$$L = \left[\frac{1}{(C2 - C1) \times 4 \times \pi^2}\right]\left[\frac{1}{f_2^2} - \frac{1}{f_1^2}\right] \quad (3)$$

where

- L is the value of the stray inductance that should be snubbed

L is a bulk inductance and is not any individual inductance.

Find the appropriate values of C*x* and R*x*. Use Equation 4 to calculate the appropriate R*x*.

$$Rx = 2 \times \pi \times fx \times L \quad (4)$$

where

- fx corresponds with the selected value of C*x*

If C1 is used then use $f1$, and if C2 is used, then use $f2$.

To account for tolerances and differences in production units, use a value that is 0.7 to 0.8 of the calculated R*x*. Too high a value for the R*x* could allow for a spike, but too low of a value for R*x* could cause the snubber to draw excessive current and overheat. Use Equation 5 to calculate the power loss in the resistor.

$$P = Cx \times V^2 \times f_S \quad (5)$$

where

- V is the voltage at PVDD
- f_S is the switching frequency

1.4.2 Demodulation Filter Design

An output LC-demodulation filter is required to reconstruct the audio signal and protect the amplifier. The components must be carefully selected for proper operation of the Class-D amplifier. The inductor is especially of concern because an improper inductor can cause a class-D amplifier to shutdown or fail.

The circuit consists of two inductors and three capacitors as shown in Figure 4. The main demodulation filter consists of the two inductors, L, and the difference mode capacitor, CDM. The two common mode capacitors, CCM, filter any common mode signals from the switching waveform.

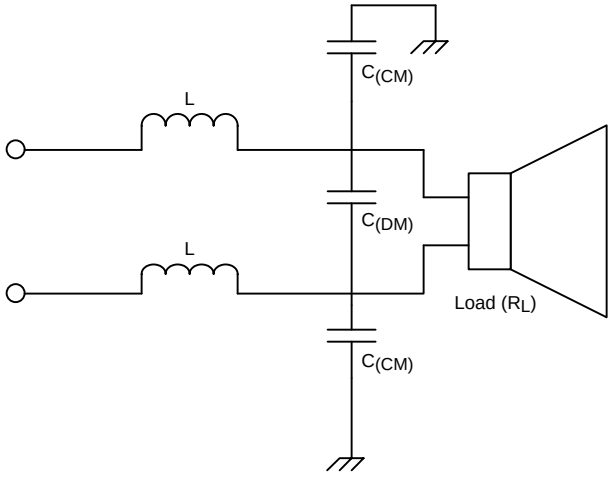


Figure 4. Typical Output Demodulation Filter

The calculation of these components is based on the nominal load impedance R_L and the desired frequency response. The frequency response is dependent on two values, the cutoff frequency and a characteristic of the roll-off.

$$C = \frac{2 \times Q^2 \times L}{R_L^2} \qquad L = \frac{R_L}{4 \times \pi \times f_{co} \times Q}$$

where

- Q = a characteristic of the f_{co} roll-off
- f_{co} = the cutoff frequency (6)

For a typical amplifier response the value of Q should be 0.7071

The unloaded condition of the TAS54xx family of devices must be understood. The Q of the filter is directly proportional to the load. In an unloaded condition the load resistance is infinity and therefore the value of Q would be infinity also. See Equation 7.

$$Q = \frac{R_L}{4 \times \pi \times f_{co} \times L} \quad (7)$$

The peak of the Q value is located at f_{co}. The signal at this frequency is greatly amplified and can be measured on an oscilloscope. This signal is seen as a sine wave and can be mistaken as an oscillating amplifier.

1.5 Component Selection

1.5.1 Inductors

When the inductance value has been determined, three additional specifications must still be considered when specifying an inductor. Aside from the inductance, the Q factor, current rating, and DC resistance (RDC) values must be considered. Do not confuse the inductor Q with filter Q; these are two different parameters.

The inductance value is usually specified at 0 A which is typically called the initial inductance. A typical tolerance is 20%. As current increases through the inductor, the inductance eventually decrease because of the Q Factor.

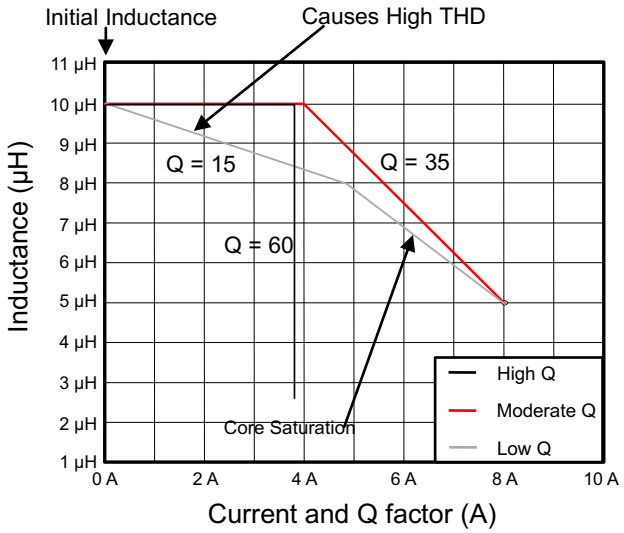


Figure 5. Inductance Versus Current and Q Factor

The Q factor is defined as the ratio of the total energy in a system to the energy lost per cycle. Therefore, depending on the Q factor, inductance will vary with current in different ways. This variation gives both high-Q and low-Q inductors certain advantages that ultimately become trade-offs or constraints in a design. As an example, Figure 5 shows three inductance curves for three inductors with different Q factors.

A high-Q inductor has little change in inductance before the inductor saturates. While a high-Q inductor provides flat inductance versus current response and good idle current, it can saturate too quickly. As a result, the inductance value may drop too low and cause the switching current to increase rapidly which possibly triggers the current protection circuitry prematurely.

A low-Q inductor does not saturate quickly. Instead, a low-Q inductor stores more energy but becomes hotter than a high-Q inductor. The inductance value begins dropping immediately with current. The filter characteristics change with current, the switching frequency is not attenuated as well, and the idle current will be higher. A low Q is found to have an adverse effect on the THD of an amplifier.

A good Q value is often somewhere between a high-Q and low-Q inductor, so that the inductance is stable up to a high current level and does not have the THD effects of a low-Q device. The core saturation occurs but not quickly, allowing for proper filtering and amplifier functionality during high current peaks.

The current rating is typically defined as the current where the inductance falls to 20% of the initial inductance. Ensure that the inductance does not drop below a minimum value (approximately 20% of the value) at the maximum current of the amplifier. If the current-rating value is not tested by the manufacturer, testing is required to determine if the inductor can be used.

The DC resistance (RDC) is the series resistance of the copper wire at room temperature. This resistance increases with temperature. As this resistance increases, less power is delivered to the loudspeakers and more power is dissipated in the voice coil creating more heat in the voice coil, increasing RDC further. The RDC is determined by the amplifier power and nominal speaker impedance. A 25-W rated amplifier into a 4-Ω speaker should use an inductor with a maximum RDC of 25 mΩ. When either amplifier power increases or speaker impedance decreases, the RDC of the inductor must decrease.

Other losses occur that decrease the power that is delivered to the speaker. The ferrite or powdered iron core loses a small amount of power in the core to generate the flux or B-field which is called core loss. The core loss is constant over the current rating of the inductor. Typically, the core loss is the dominating loss at idle and is also temperature dependent.

Parallel impedance can provide an indication of the idle power losses. Parallel impedance is a measurement that can indicate the lumped losses in the inductor which includes the core loss. A high resistance indicates a better inductor. An inductor with a parallel resistance of 50 Ω is not a good inductor for Class-D amplifier use, whereas an inductor with 250 Ω is considered a good inductor. This parameter is typically measured with an impedance bridge set in the parallel mode.

Now that the inductor can be specified, the specifications over temperature must be understood by the user. At high current, the inductance typically decreases dramatically as temperature increases. Temperature rise is because of self-heating from copper wire loss and core loss. The inductor can also be heated from external heat sources. Therefore, evaluating the inductor for the specifications over temperature is necessary.

1.5.2 Capacitors

The capacitor material for the LC filters must create a stable capacitance over voltage and temperature. The best materials are the film and foil, and metalized film. These types of capacitors offer the best stability, but unfortunately can be large and costly. Ceramic capacitors with X7R materials function just as well as film capacitors over voltage and temperature and have a much better cost and size.

1.6 Protection

1.6.1 Voltage Protection

In an automotive environment the typical power supply voltage, PVDD, is the car battery. The battery voltage can have large voltage swings during the normal operation of the vehicle. The possibility of unusual events such as load dump are also present. The TAS54x4C devices have protection against over voltage on the PVDD pin up to 50 V. Undervoltage protections exists on the PVDD, AVDD, DVDD, and CP pins. The CP and AVDD undervoltage protections are related. If a CP under voltage occurs, the AVDD voltage is turned off for safety and an AVDD under voltage occurs. In this case, both CP and AVDD undervoltage bits will be set and the real undervoltage fault is CP.

1.6.2 Over Temperature

The over temperature protection has two modes. One mode is a warning that the device temperature is high, and the other mode is a shutdown to protect the device from a thermal failure.

NOTE: The TAS5414C and TAS5424C must have the OTW enabled with I^2C in register 0x0A, so that the $\overline{\text{CLIP\_OTW}}$ pin will report an overtemperature warning.

The warning mode has three levels. The first warning level triggers the $\overline{\text{CLIP\_OTW}}$ pin on the TAS54x4C and sets a bit in the I^2C registers. This first warning level triggers at 125°C with a ±13°C. The second level triggers at 135°C, the third level triggers at 145°C. The temperatures of the levels track to 10°C of each other with a ±2°C tolerance. For example, if the first level triggers at 115°C, which is inside the tolerance, then the second level will trigger at 125°C with a tolerance of ±2°C and the third level will trigger at 135°C with a tolerance of ±2°C.

If the temperature reaches over temperature shutdown near 155°C the device will place the outputs in hi-Z mode. The I^2C continues to operate. The tolerance of the temperature is the same as in the above example.

The overtemperature warning can be used to adjust the volume level or reduce bass in the system, so that the amplifier will not produce more heat. This warning can also be used to turn on a system fan.

1.6.3 DC Offset

In a car environment with extreme temperature and humidity changes, electronic components such as electrolytic capacitors can become leaky over time. If this capacitor is used in series with the input signal and it becomes leaky and DC offset at the speaker outputs could occur. Many other factors cause DC offset to occur in an audio system.

The DC offset protection monitors the DC output of the amplifier by measuring the width of the pulses over time. The patented circuitry continuously measures the output, even when a signal is present. The audio signal does not affect the DC offset measurement. DC offset is necessary in the car environment to protect against an over-heated voice coil in a speaker. By default the DC offset protection activates the $\overline{\text{FAULT}}$ pin and places the channel in hi-Z. A bit can be disabled with I^2C to allow for the channel to remain in play, but indicate a fault on the $\overline{\text{FAULT}}$ pin and in the fault registers.

1.6.4 Over Current

The TAS54x4C devices provide two types of overcurrent protection. The first is current limiting. The current-limit method is a straight-line current-limit that is independent of the power supply voltage. Current limiting is necessary if the output current into the load exceeds a safe level for the device. Instead of shutting the channel off, the output is limited to the maximum current. The signal to the speaker appears to be voltage clipped. If the output current-limit is detected continuously for 100 ms then the channel is placed in hi-Z mode.

The second method in overcurrent protection is a shutdown which places the faulty channel in hi-Z, but does not turn off the I^2C. This second method occurs if either amplifier output, post LC filter, is shorted to the PVDD pin or ground. This protection is not ensured if the IC output pin is shorted to the PVDD pin or ground.

1.6.5 $\overline{\text{FAULT}}$ Pin

The $\overline{\text{FAULT}}$ pin is an open drain output that asserts low when a fault is present in the device. This pin requires a 47-kΩ pullup resistor to operate correctly. When using multiple TAS54x4C devices in a system the pins can be simply paralleled together with a single pullup resistor.

1.6.6 $\overline{\text{CLIP\_OTW}}$ Pin

The $\overline{\text{CLIP\_OTW}}$ pin on the TAS54x4C devices indicates when the output is clipping. Clipping is determined when the PWM output is at 100% modulation. At 100% modulation the PWM misses a pulse. When a pulse is missed a signal is sent to these pins. The THD level can be determined by the number of pulses that are on these pins over a certain time period or by using a RC filter a voltage can be measured.

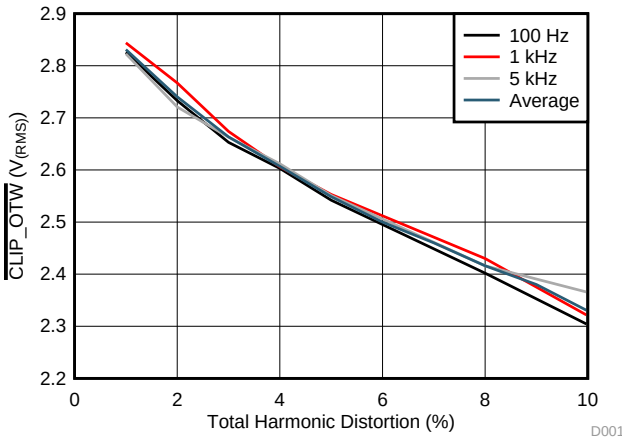


Figure 6. $\overline{\text{CLIP\_OTW}}$ Pin Voltage Versus % of THD

1.7 Load Diagnostics

One feature that is required in automobile assembly and in system debugging is the ability to test each channel for the proper load or speaker connection. Four potential problems can occur at the speaker output. The speaker could not be present or connected properly (open load), the speaker or speaker wires could be shorted (shorted load), the speaker wires could be shorted to ground, and the speaker wires could be shorted to power or battery. The TAS54x4C devices have the ability to test all of the channels at the same time or each channel individually for a proper load. The load diagnostics are instigated through an I^2C command. See Figure 13 for a flowchart of the load diagnostics.

In the situation where at least one channel is not in hi-Z mode, only the short to ground and short to power are tested. The shorted load and open load cannot be tested because the $\overline{\text{MUTE}}$ pin is used to create the signals for these tests. These pins must remain stable for the channels that are not in hi-Z.

When running these tests the test stops on first failure on the channel with the failure. The other channels continue to test and also stop on the first failure. This type of failure may not catch a double fault. For example, assume a channel has a short to ground and is an open load. The load diagnostics would detect the short to ground and set the bit in the load diagnostics register, but it would not detect the open load. The open load would be detected after the short to ground was fixed and another load diagnostic was run.

Figure 7 shows the load diagnostic waveform according to the TAS54x4C data sheet.

1.7.1 Understanding Load Diagnostics Timing

Load diagnostics consists of four testing phases and two non-testing phases. Table 3 lists the duration of the tests. Changing the values bit 3 and 4 in register 0x10 changes the duration of the tests or adds a pause between the S2P test and the OL test.

The need for the longer duration allows for larger common mode capacitors in the output filter. To prevent false or inconsistent short indications the total capacitance on each output pin to ground for the S2G and S2P should not exceed 680 nF.

Table 3. Load Diagnostic Timing

PHASE	DEFAULT SETTINGS (ms)	EXTENDED TIME SETTING (ms)	LDP SETTING (ms)
Sync	20	20	20
S2G	20	80	20
S2P	20	80	20
LDP	0	0	20
OL	150	150	150
SL	250	250	250

The first phase is the sync phase. This time allows the channels to synchronize the test sequence before the test begins. The next two phases test the 8 output terminals for shorts to ground or power. Both outputs are pulled to the PVDD pin or ground with current sources and not the power FETs. A short to ground failure occurs if any output does not reach either PVDD pin. Likewise, if any output does not reach the ground, a short-to-power failure occurs. If a boosted PVDD is used, the S2P test can still detect a short to battery. The OL and SL tests derive the signal by charging and discharging the $\overline{\text{MUTE}}$ capacitor. This signal is directed to the output pins. The signal is measured differentially across the two outputs pins of the channel. If the correct amplitude is not measure either a SL or OL fault is created.

Any faults determined during the load diagnostic will be displayed in I^2C registers 0x02 and 0x03. These values persist in the registers until a new load diagnostic is performed or a reset is performed.

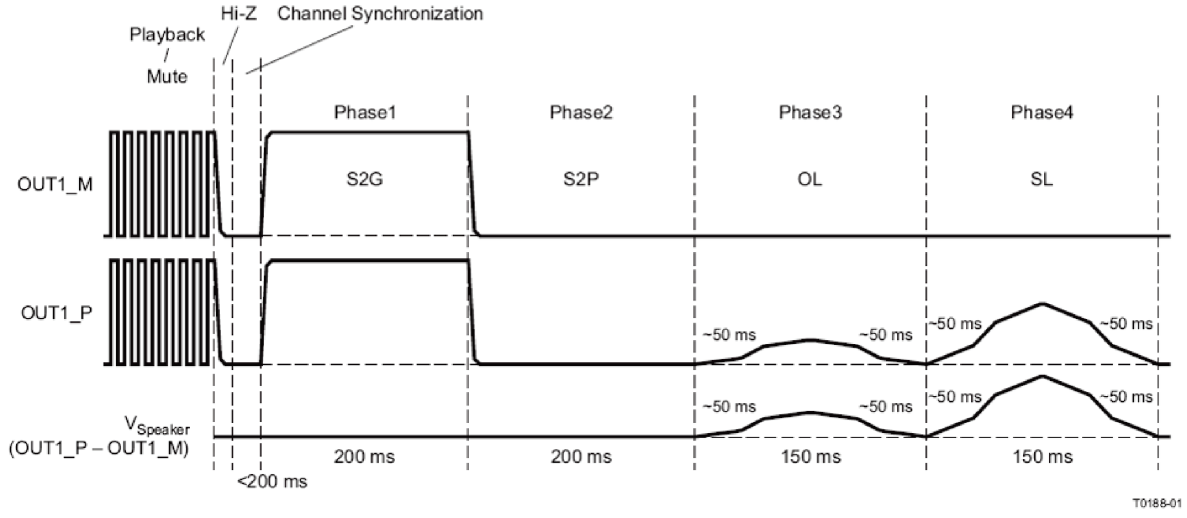


Figure 7. Load-Diagnostic Output-Waveforms Timing Diagram

NOTE: Note that these waveforms are presented in this form to emphasize how the load diagnostic signal is being applied by the device. The actual amplitude of the applied signals in Phase 3 (open load) and in Phase 4 (shorted load) are highly load dependent, and may have a greatly decreased amplitude compared to those shown in Figure 7 when a load is properly connected.

1.7.1.1 S2G and S2P Detection With and Without Loads

Softer shorts on S2G and S2P can be detected with no load as opposed to with a load. The minimum resistance for S2G and S2P detect increases by a factor of 2 (and thereby increasing the threshold) when no load is present than when a load, specifically 4 Ω, is added to the output.

1.7.2 Tweeter Detect or AC Load Diagnostics

The regular load diagnostic uses DC to perform the detection functions. To detect a capacitor-coupled tweeter a tweeter-detection circuit is needed. The TAS54x4C devices use a special detection threshold of the current limiter circuitry and therefore required an audio signal to trigger this circuitry. This signal must be at a frequency and signal level where the tweeter impedance is the nominal. The crossover or capacitor increases the load impedance at lower frequencies. The output LC filter can increase the load impedance at high frequencies.

For example, a DC connected woofer and a capacitor-coupled tweeter are in parallel. In a typical installation the capacitor is connected within the tweeter terminal as a pretested module. The load diagnostics test the presence of the woofer and the integrity of the speaker wires, but cannot test the presence of the tweeter. In this case tweeter detect is used to check that the tweeter is connected properly.

An issue in accurately measuring an unloaded capacitor-coupled tweeter can occur when a DC-coupled woofer is not in parallel with the capacitor coupled tweeter. An unloaded LC filter can cause a resonance to occur in the TAS54x4C and falsely trigger the tweeter detection circuitry.

1.8 Power Supply

The power supply for the TAS54x4C family of devices does not need to be regulated and therefore the power supply can be the battery of the vehicle. These devices have feedback around the class D amplifier to provide a fixed gain. As in many class D amplifiers the gain is dependent on the power supply voltage, but with feedback this is not the case. Additional circuits have been added to improve the power-supply rejection ratio (PSRR) further. The need for wideband PSRR is to remove high frequency, but audible, noises from the speaker outputs, such as alternator whine.

The power supply or PVDD needs proper PCB layout for proper performance. The PVDD pins are in two groups. Place a bulk capacitor of 470 µF or greater near each group of pins. Also a 1-µF bypass X7R ceramic capacitor must be placed as close to each group of PVDD pins and the PGND pins as possible for good bypassing. These capacitors are necessary to provide high frequency stability on the PVDD. The placing of the capacitors at each group of pins is needed because the internal connection between the two groups in not a high current connection. Therefore, good current carrying capability to all the PVDD pins is needed.

1.9 Charge Pump

The charge pump, CP, is necessary so that the high-side output N-channel FETS have the proper gate voltage. The charge pump voltage is above PVDD. The function of the charge pump is optimized for the 1-µF / 50-V capacitors as shown in the data sheet. Changing these values is not needed. The charge pump is a capacitor-coupled switch-mode supply that pumps up the charge on a capacitor. If either of the two 1-µF capacitors is not connected the charge-pump voltage will not be available for the high-side FETS. A CPUV fault will place all the amplifier output stages in hi-Z. Also, the AVDD pin will be turned off so that the output FETS do not try to function without the charge pump voltage, so an AVDDUV fault will be present in the I^2C fault registers.

1.10 EMI and PCB Layout Considerations

Electromagnetic interference (EMI) only relates to the TAS54x4C devices and the PCB layout. This section also includes some discussion on the critical filtering component. Car manufacturers require a strict electromagnetic compliance (EMC). Most manufacturers use the requirements for, or base their requirements on the CISPR25 specification. The TAS54x4C devices can be part of a system that meets these requirements. The devices already have many characteristics designed into them to eliminate the emission of EMI. There are two types of tests for EMC emissions, conducted and radiated. Conducted tests measure the EMI on the power and ground wires directly. Radiated test are performed with a series of antennas.

1.10.1 PCB Layout Concerns

The PCB layout for the TAS54x4C devices must satisfy function, performance, and EMC. The devices have the signal input and control pins on one side of the IC package and the output and power pins on the other side to ease PCB layout.

A good ground plane is required for EMC and proper function of the TAS54x4C devices. All the GND pins must be connected to the same ground plane. Preferably a ground plane should be on the top and bottom of the PCB with many vias tying the two planes together. The ground plane should encase all of the traces on the PCB so that the ground plane reaches all the edges of the PCB. Vias should be placed 10 mm apart near the edge tying the ground plane together to create a Faraday cage.

For proper function all the bypass capacitors on the D_BYP, A_BYP, CP, and PVDD pins must be as close to the pin as possible. The ground side of the bypass capacitors should be directly connected to the ground plane. The bypass capacitors for PVDD should be connected to the ground plane close to the GND pins to produce a low inductance path. The RC snubbers on the output pins should have the corresponding ground connected to the ground plane as close the GND pins to improve the effect.

The best solution for EMC is to use a four-layer PCB with all the traces with high current or clocks on the inner layers with vias to connect them to the parts. The outer layers are reserved for ground planes which creates a Faraday cage around the whole PCB reducing the EMI emanated from the PCB.

1.11 Filtering

1.11.1 Power Supply Filtering

The power supply is tested for both conducted and radiated emissions. The first test is for conducted emissions. If EMI is not conducted on the power wire, then it cannot radiate. On the TAS54xx device the majority of the conducted EMI is *differential mode*. To remove differential mode EMI a series inductor with a capacitor to ground is used. A second inductor in series can also be used for further reduction of conducted EMI to form a *T* filter. The values for the inductors are from 10 µH to 40 µH. The capacitor used is a parallel combination of two 4.7µ, 0.082µF, and 2.2nF capacitors. This combination extends the effectiveness above 100 MHz. For *common mode* EMI a four layer PCB can be used. The two outside layers are the ground plane with the power traces on one of the inner layers. The two ground layers are connected together with many vias which forms a pseudo coaxial cable and blocks the common mode EMI from entering the power traces.

1.11.2 Output Filtering

The outputs of the TAS54x4C devices have a large PWM waveform with a large current. These pins and traces connected to the output pins produce the largest amount of EMI in the system. The EMI is dominated by difference mode and therefore the LC filter described in the data sheet provides the most reduction. The PCB traces between the TAS54xx device and the inductor in the LC filter must be as short as possible. If a four-layer PCB is used, these traces should be on an inner layer with the ground plane on the two outer layers. The previously described snubbers also reduce the EMI on these traces.

After each inductor, place two 470nF capacitors to ground for common mode EMI reduction. The ground for these two capacitors should be at the same ground plane point. If they are not grounded at the same point the common mode EMI reduction is decreased.

At the output connector, on each output pin, place a capacitor shunt to ground. This capacitor shunt placement removes high-frequency common-mode EMI that can contaminate the PCB traces between the LC filter and the output connector. Again, this placement works on common mode so the ground connection to the ground plane should be at the same point which improves EMI above the 50 MHz region.

1.11.3 Input Filtering

The input pins and PCB traces are part of a high impedance node that can be easily contaminated with EMI from inside the device or from radiated EMI inside the amplifier package. TI recommends an RC filter with the R in series with the signal and the C in shunt to ground. An RCR filter may be needed so that the capacitor does not directly load the signal source (see Figure 1).

NOTE: For best system noise performance use the smallest resistor values possible. If the resistor value is too high noise will increase.

1.12 Paralleling Outputs

The TAS54x4C devices can have the channels placed in parallel to increase the current capability to drive lower impedance loads. Some simple rules can be followed to correctly place the channels in parallel. The outputs must be paralleled after the inductors. The outputs cannot be paralleled before the inductors because the turn on and turn off times of the output FETS can be different on each channel.

NOTE: New to the TAS54x4C devices is the ability to parallel channels 1 and 2, and 3 and 4. When channels 1 and 2 are paralleled, the output must still be paralleled after the inductors, and the input signal is placed on channel 2. The channel 1 input can be left disconnected. When channels 3 and 4 are paralleled the input signal is placed on channel 3 and the input on channel 4 can be left disconnected.

The power is still voltage limited. To increase the power specification, a lower load impedance is necessary. For example, one channel into a 4 Ω load at 14.4 VDC can provide 28W at 10% THD. By paralleling two channels, one channel still has 23 W at 1% into 4 Ω, but 46 W into 2 Ω. If three channels are in parallel, the amplifier provides 69 W into 1.33 Ω. Four channels in parallel can provide 92 W into 1 Ω.

Another example where this practice works well is near the maximum PVDD. One channel into 4 Ω at 21 VDC can provide 58 W at 10% THD. One channel into 2 Ω at 21 VDC is not recommended because of thermal limitations, but two paralleled channels into 2 Ω can provide 116 W at 10% THD. By sharing the current with two channels the losses because of $r_{DS(on)}$ are reduced and therefore the thermal limitation is reduced. Four channels into 1 Ω would provide over 232 W at 10% THD.

1.13 Mute

Muting is performed by ramping the gain from the I^2C gain setting to zero. The time to perform this ramp is determined by the capacitor that is on the $\overline{\text{MUTE}}$ pin on the TAS54x4C devices. The specified capacitor value is 220 nF. The ramp time can be reduced by decreasing the value of the capacitor.

1.14 Standby

The transition from standby mode to active mode should be quick. A slow transition from standby to active mode can cause a pop or click in the speakers. A quick transition does not have this issue. Therefore, placing a capacitor on this pin is not recommended. The transition time from 0 V to 3.3 V and from 3.3 V to 0 V should be less than 25 µs.

1.15 Line Output

The TAS54x4C devices have a gain setting of 12 dB that is created if the device is used as a line driver. As a line driver the PWM signal must still be demodulated to produce a clean signal. An LC circuit can be used with lower-power rated inductors. A proper load is required in order to ensure that the frequency response is flat. Another option is an RC circuit, but signal loss caused by the series resistor may preclude using this. Using the RC with an operational amplifier (op-amp) can remove the signal loss issue but with additional costs. With a line output, the load diagnostics may detect the load as an open.

1.16 Harmonic Crosstalk

The TAS54x4C devices exhibit a small amount of harmonic crosstalk. Harmonic crosstalk means that the crosstalk gain of the second, third, fourth, and additional harmonics is larger than expected compared to the harmonic content at the output of a channel with a fundamental tone applied. As an example, the second harmonic of a victim channel in a crosstalk experiment is only 10 to 15 dB less than the fundamental tone, as opposed to the 70-dB reduction from fundament to second harmonic that is expected if the tone were applied directly to the channel. Therefore, the harmonic frequencies typically have a crosstalk gain of –70 to –80 dB on the victim channel.

The harmonic crosstalk is most prevalent on channels that have the respective switching frequencies 90 degrees out of phase. This situation arises on alternate channels of the TAS54x4C devices when the default switching phase of 45 degrees between adjacent channels is selected. With this default phase setting the pairings of channels 1 and 3 and of channels 2 and 4 exhibits the most noticeable harmonic crosstalk effects. Figure 8 shows the harmonic crosstalk on the output of channel 3 when a 1-kHz aggressor signal is applied to channel 1.

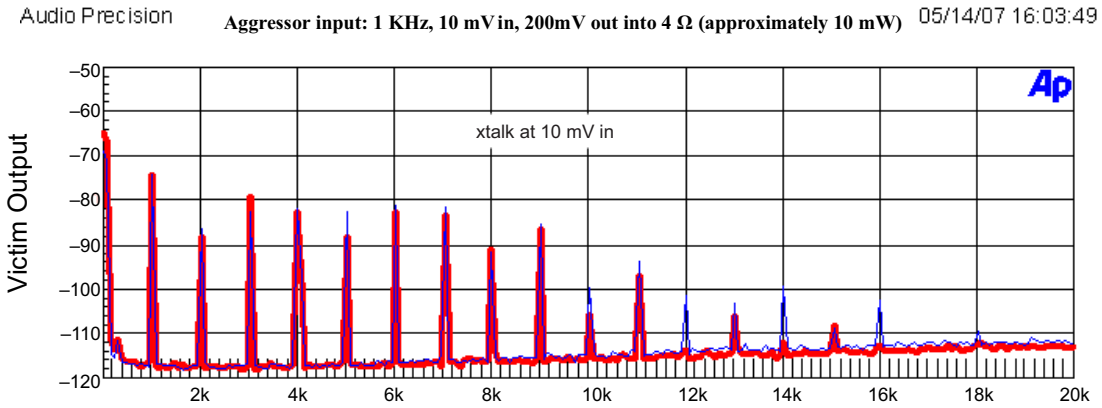


Figure 8. Channel 1 → Channel 3 Harmonic Crosstalk With Default Switching Phase Settings

As shown in Figure 8, an FFT sweep of the output of the victim channel is needed to properly quantify the effects of harmonic crosstalk. This issue is hidden by standard frequency-selective crosstalk sweeps.

1.16.1 Harmonic Crosstalk Work Around

Because the harmonic crosstalk issue is worse on channels that have their respective switching frequencies 90 degrees out of phase, the issue can be greatly improved by changing the relative switching phase of adjacent channels from the default setting of 45 degrees to 180 degrees. This adjustment can occur through I^2C commands in register 0x0A.

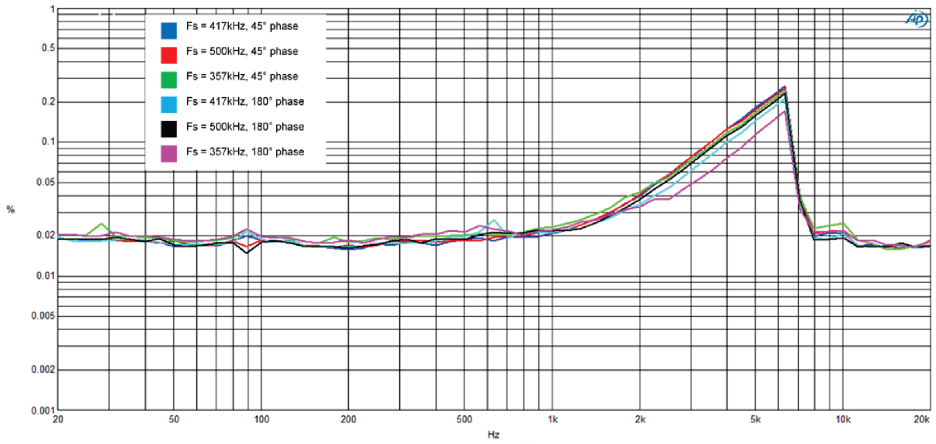
One potential downside to changing this setting is that it can adversely affect EMC performance. In particular, the second harmonic of the switching frequency can increase on radiated emissions measurements. Any audio system in which this switching phase change is made should be EMC tested with this change implemented to ensure that all EMC requirements are met.

1.17 THD+N Versus Frequency

THD plus noise versus frequency is usually measured with f_s = 417K Hz at 45° phase difference and crosstalk enhancement disabled (default). The following are two options to reducing THD measurements:

1. Lower the switching frequency. A lower switching frequency results in fewer samples taken of incorrect data.
2. Switch to 180° phase difference. The amount of cross talk and feedback from other channels are reduced.

These options can be incorporated individually or together. Therefore the best THD+N versus frequency data would be to incorporate all of the options at once (for example: f_s = 357K HZ at 180° phase shift). Figure 9 shows a graphical representation of these options.



$V_{(PVDD)}$ = 14.4 V R_L = 4 Ω P_O = 1 W
T_A = 25°C

Figure 9. THD+N vs Frequency Improvements

2 TAS54x4C Software Design Guidelines

The programming of the control system for the device can be broken down into separate functions to make the programming easier. Use this design guide along with the data sheet.

2.1 Definitions

To following definitions will help the user understand the flowcharts and operation of the device. The H-bridge output stage has five operating modes:

Hi-Z mode — The output stage is not switching. All four FETs in the output stage are off and the output appears as a high impedance or hi-Z state.

Mute mode — The output stage is switching at 50% duty cycle. The modulated signal is not connected to the output stage.

Play mode — The output stage is switching with the modulated signal connected to the output stage.

Low-low mode — The inductive nature of an audio speaker is capable of some current storage (back EMF). At turn off the stored current must be controlled before the output stage proceeds to the hi-Z mode. The low-low mode pulls the output stage to ground to drain the stored current.

Load diagnostics mode — The output stage in this mode is controlled internally through special states to measure the condition of the external amplifier load.

Gain and common mode ramps — In addition to the five operating modes for each H-Bridge output stage there are also ramps to reduce pops and clicks. During the ramps the status registers report that the device is not in any of the five operating modes previously listed.

$\overline{\text{MUTE}}$ pin — The $\overline{\text{MUTE}}$ pin has a capacitor that controls the timings required to reduce the potential pop and click at amplifier turn on and turn off. This pin can also be used for an emergency mute if it is pulled to ground. By pulling this to ground and then proceeding with I^2C commands to transition to hi-Z mode the device is unable to transition between states because the ramps are prevented until the emergency mute is released.

2.2 Power Up and Initialization

Every time the device is powered up or returns from a POR (power on reset) event, an initialization procedure must occur. Figure 10 shows a flowchart of this procedure. Load diagnostics can run at every power up to determine that the output connections to the speakers are normal.

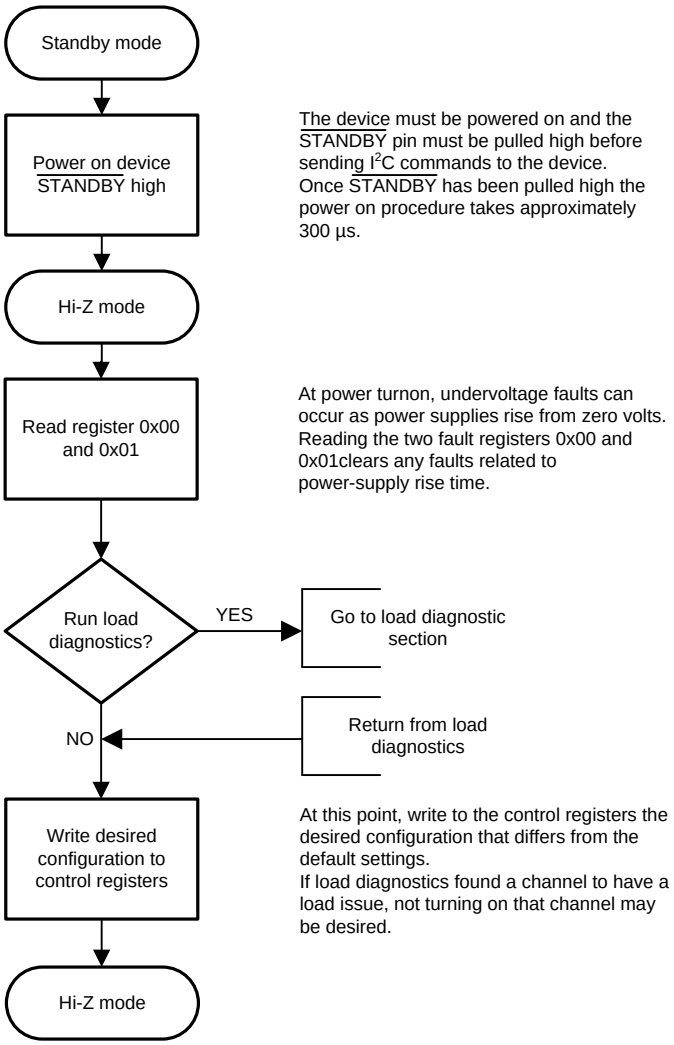


Figure 10. Power Up and Initialization

2.3 Using the Device to Play Music

The device is now powered on, load diagnostics may have run, and the device is configured. The output stages are in hi-Z mode. The output stages must transition from hi-Z mode to mute mode, and then into play mode to minimize pops or clicks in the speakers.

The register values shown in Figure 11 are for all four channels. If any channels do not to follow this sequence the values must be adjusted accordingly.

NOTE: Pop and click reducing ramps are not available if any channels are already in mute mode or play mode.

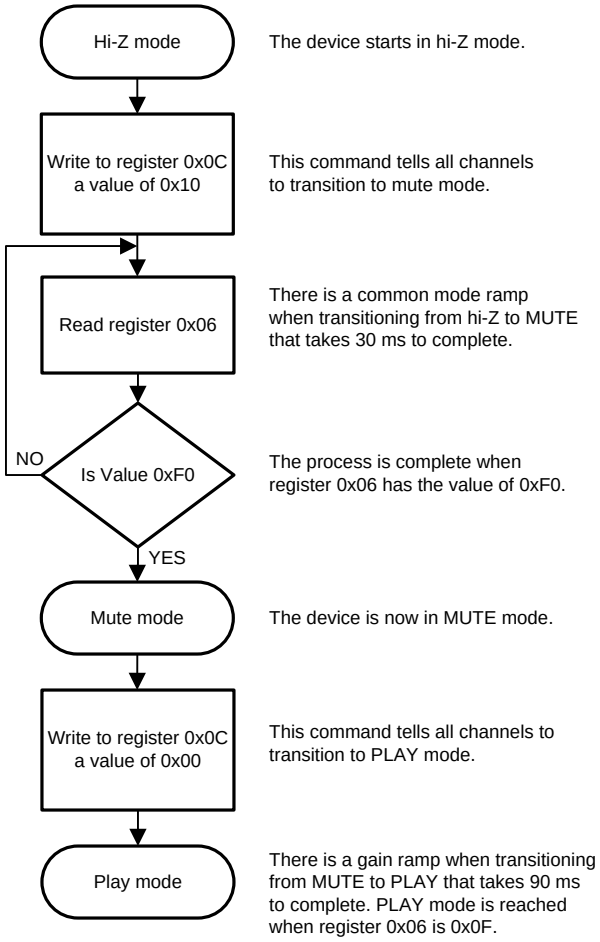


Figure 11. Turnon flowchart

2.4 Using the Device to Stop Playing Musing

The device requires one command to place all channels into hi-Z mode from play mode. The device still executes several ramps and transitions during the process as in Figure 12. If desired by the user, the device can also be commanded to any state separately but this command is not required.

The register values shown in Figure 12 are for all four channels. If any channels do not follow this sequence the values must be adjusted accordingly.

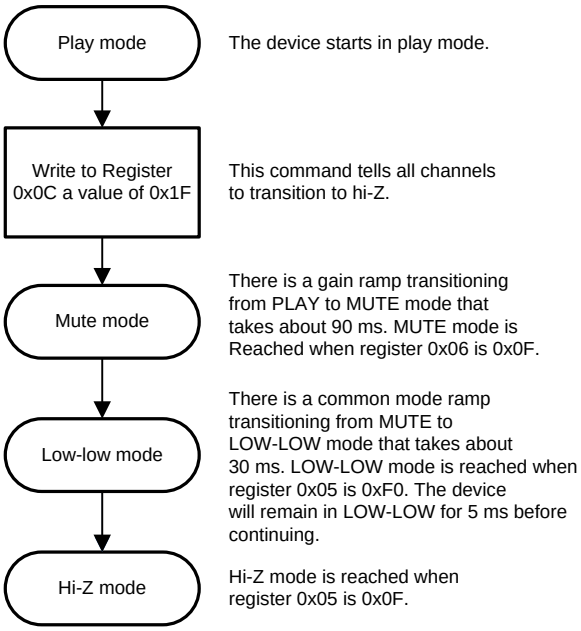


Figure 12. Turnoff Flowchart

2.5 Load Diagnostics

In automotive applications, testing the system for speaker wire shorts to the chassis (ground), speaker wire shorts to the battery, open speaker wires, or shorted speaker wires may be necessary. Load diagnostics can be a factory or dealer test, or can be run every time the audio system is turned on.

This test can also be run if a channel fault condition is detected. In this case only the single channel can run while the other channels are still playing. In this mode only a speaker-wire shorts to battery and speaker-wire shorts to ground are run, but the flow is still the same. The total time for load diagnostics is about 450 ms.

Load diagnostics can be started using the flow shown in Figure 13 from any state (play, mute, hi-Z, or low-low). If any channel needs to transition to hi-Z prior to load diagnostics it does so automatically and all pop and click ramps are executed and load diagnostics will take longer to start. All channels are run at the same time so if some channels are already in hi-Z these channels remain in this mode until all channels are ready.

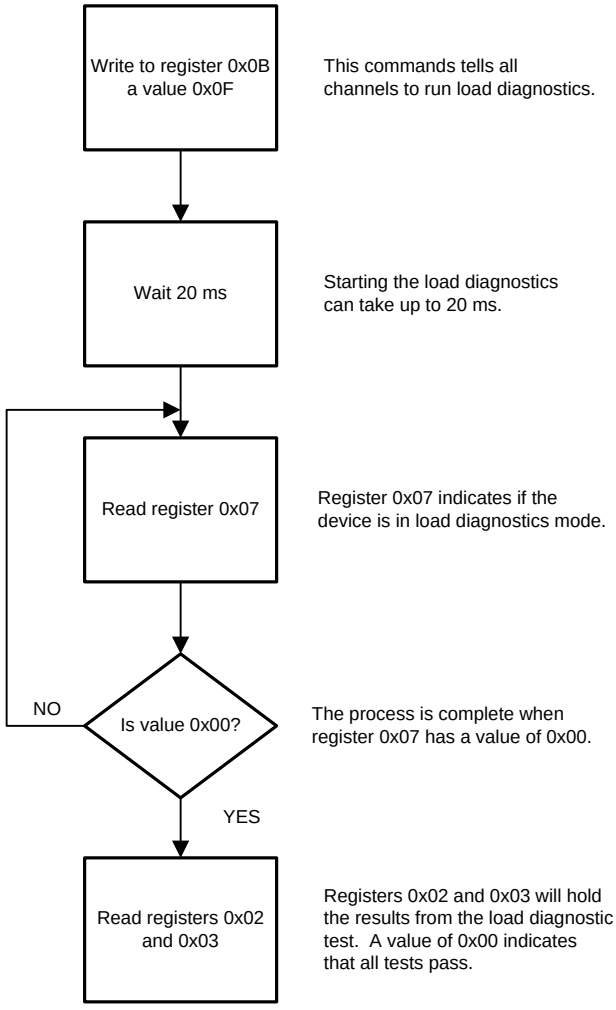


Figure 13. Load Diagnostics, Four Channels

2.6 Fault Handling

2.6.1 Global Faults

Global faults place all channels in hi-Z mode and assert the $\overline{\text{FAULT}}$ pin low. These faults are the undervoltage, overvoltage, and overtemperature faults.

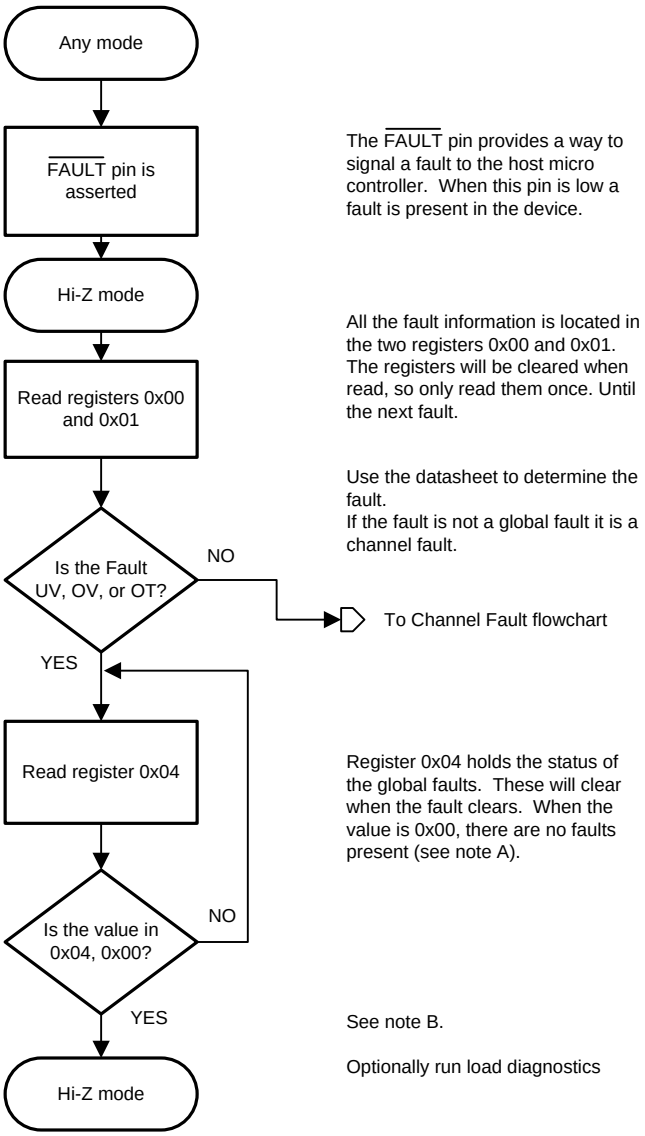


Figure 14. Global Fault Handling

2.6.2 Channel Faults

Channel faults are faults that occur on an individual channel. These faults are DC offset, overcurrent, and local overtemperature faults. Only the channel that experienced the fault is placed in Hi-Z. The other channels remain playing. The other difference between channel faults and global faults is that the fault is no longer detectable when the channel is in hi-Z mode. Load diagnostics must be run to detect if there is a system level error.

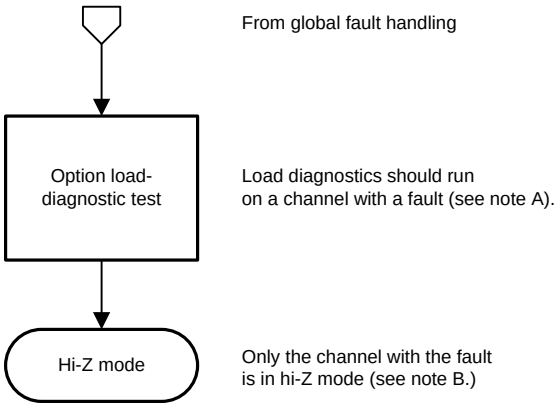
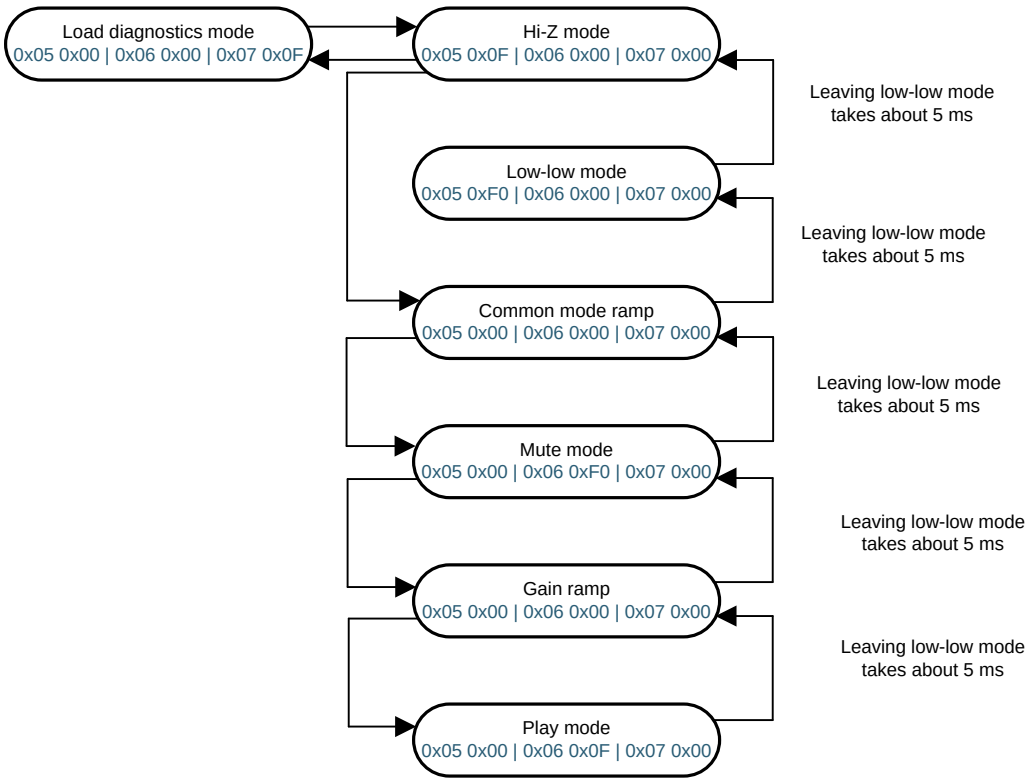


Figure 15. Channel Fault Handling

2.7 Device Mode Summary



Status register values are shown in blue text.

Figure 16. Mode Summary, Excluding Faults

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