PCB Layout Guidelines for Power Controllers

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1   Scope

Power layouts require a few basic rules. This guideline for power controller layout addresses:

- The supply of sufficient current to the load.
- Noise immunity for the load and sense circuits.
- Accurate current sensing.

Reference the controller datasheet for helpful applications information such as component selection, set point calculations and thermal considerations. The power controller datasheet may have specific bypass capacitor information. Other times it may be necessary to perform system measurements and tests to determine the optimum bypass values.

Treatment of other high frequency system signals such as clocks are not discussed here and usual good practice rules for layout and manufacturability apply.

2   Description

2.1   General

The power controller, MOSFET and sense resistor operate together to deliver power to the slot. These components should be located together at the slot.

The sense resistor is sized to select the current supplied on a given slot voltage. Because of the tolerance on the controllers comparator input voltage, the circuit design and layout must consider the high end of the current range for etch runs and vias. A circuit that is design for 12 A minimum, often supplies current to a maximum of 18 A. Use 18 A for all the etch and via calculations.

2.2   PCB Etch

Table 1 is helpful to determine the current carrying capacity of PCB etches. The table assumes:

- 1oz/sq foot copper (0.035mm thickness).
- 10°C rise on outer layers, 20°C inner layers
- Groups of high current tracks are de-rated
- Tracks are not near or over heat sink areas

Table 1. Current Capacity PCB Etch

WIDTH	CURRENT CAPACITY
0.010"	0.8 A
0.015"	1.2 A
0.020"	1.5 A
0.050"	3.2 A
0.100"	6.0 A

From Table 1, each doubling of copper thickness allows an increase of sqrt(2) (about 1.4) in the current capacity. Each doubling of a single track width increases current capacity by a factor of 1.65.

For our 12-A minimum output example, the etch run should be designed for 18 A. Using 1 ounce copper, an etch width of 0.35 inches is minimum for a 10°C rise on the outer layers.

2.3 Vias or Feedthrus

Vias limit the current and add inductance between the power supply and load. Layouts are usually done with 10-mil inner ring feedthrus. At this size, current capability is about 1 A per feedthru. To access power from the inner layer plane to the MOSFET input in our example requires 18 feedthrus

Bypass capacitors should be located on the same side of the board as the target component as close to the component as possible. If feedthrus are used, the design must consider the inductance of the feedthru. It may require multiple feedthrus just to reduce the inductance. Multiple capacitors may be required for bulk or low or high frequency filtering. At higher operating frequencies, the inductance is a more sever problem. Bypassing a 100-MHz signal is extremely difficult with feedthrus in the circuit. High frequency bypassing is best done on the component plane with no vias.

2.4 Sense Resistor Wiring

The sense resistor is as much as possible a direct connection between the MOSFET output and the slot power. Similar to the MOSFET circuits, the sense resistor etch must be sized to the maximum current requirement. The sense etch should be connect between the resistor bond pads and run as a differential pair to the hot plug controller. In this way, the sense voltage is measured directly across the sense resistor and is not influenced by other circuit board etch. The Kelvin connection is shown in Figure 1. Accuracy of the sense resistor measurement will be compromised if these details are not met.
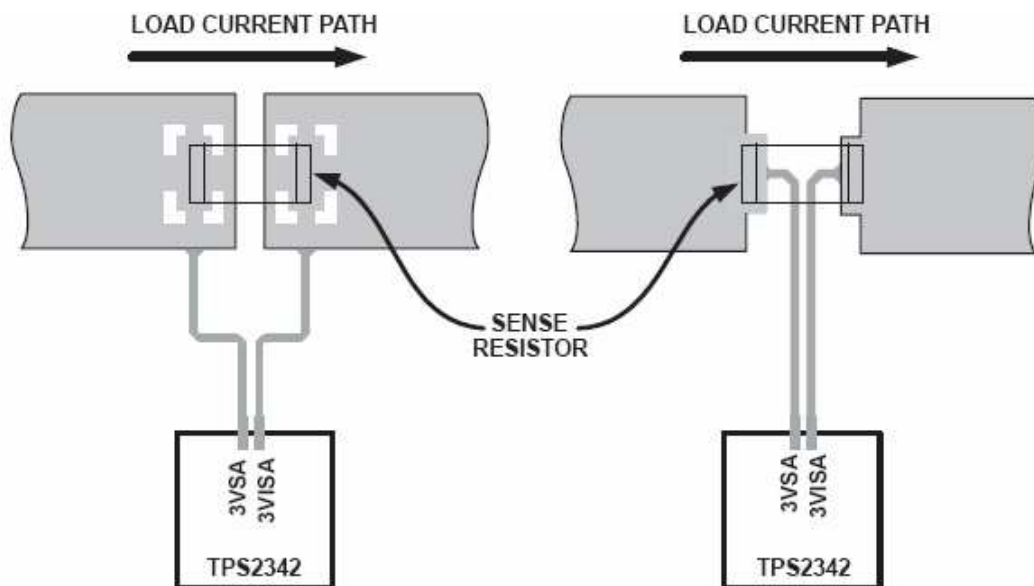
Figure 1. Kelvin Connection

2.5 Sense Resistor Bypass

Power circuits often have high current transients. These transients can cause voltage spikes across the sense resistors that can trip the hot plug controller. Bypassing across the sense resistor inputs to the hot plug controller may be required. A 1-nF capacitor located at the controller on the sense resistor input pins is usually sufficient to filter noise above 1 MHz. The capacitor value is selected based on the Impedance vs Frequency graph, Figure 2. Other filtering schemes may be necessary. Common mode noise may be better addressed with capacitors on each side of the sense resistor to ground. Adequate bypassing of the power to the FET and to the load is very important because the sense resistor and FET should not see high frequency current fluctuations.
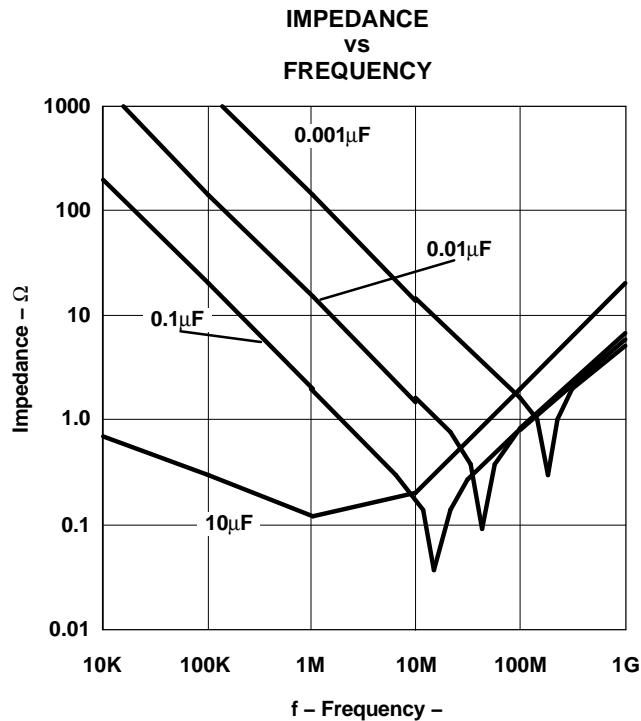

Figure 2.

2.6 Supply Bypass

Ground noise can be a major problem on backplanes with high current switching. The switching current from the PCIX and PCIX-2 transceivers with an all 1's pattern to all 0's can be 3.2 A per slot from the transceivers alone. The logic adds additional noise which can be measured across the ground plane and slot power. The noise may be coupled into sense lines or other signals through bypass capacitors not grounded close to the part that they are bypassing.

2.7 *Bulk Capacitance*

A bulk capacitor adds stability to the power supply voltage because it can supply surge current to the load. Adequate bulk capacitance for the input supply voltage should be located at the MOSFET input. Sense resistor output voltage to the slot should have bulk capacitance and high frequency bypass located at the slot. Bulk capacitance can be calculated by $C = I \times \Delta t / \Delta V$; where I is the surge current, ΔV is the voltage drop that can be tolerated, and Δt is the duration of the surge.
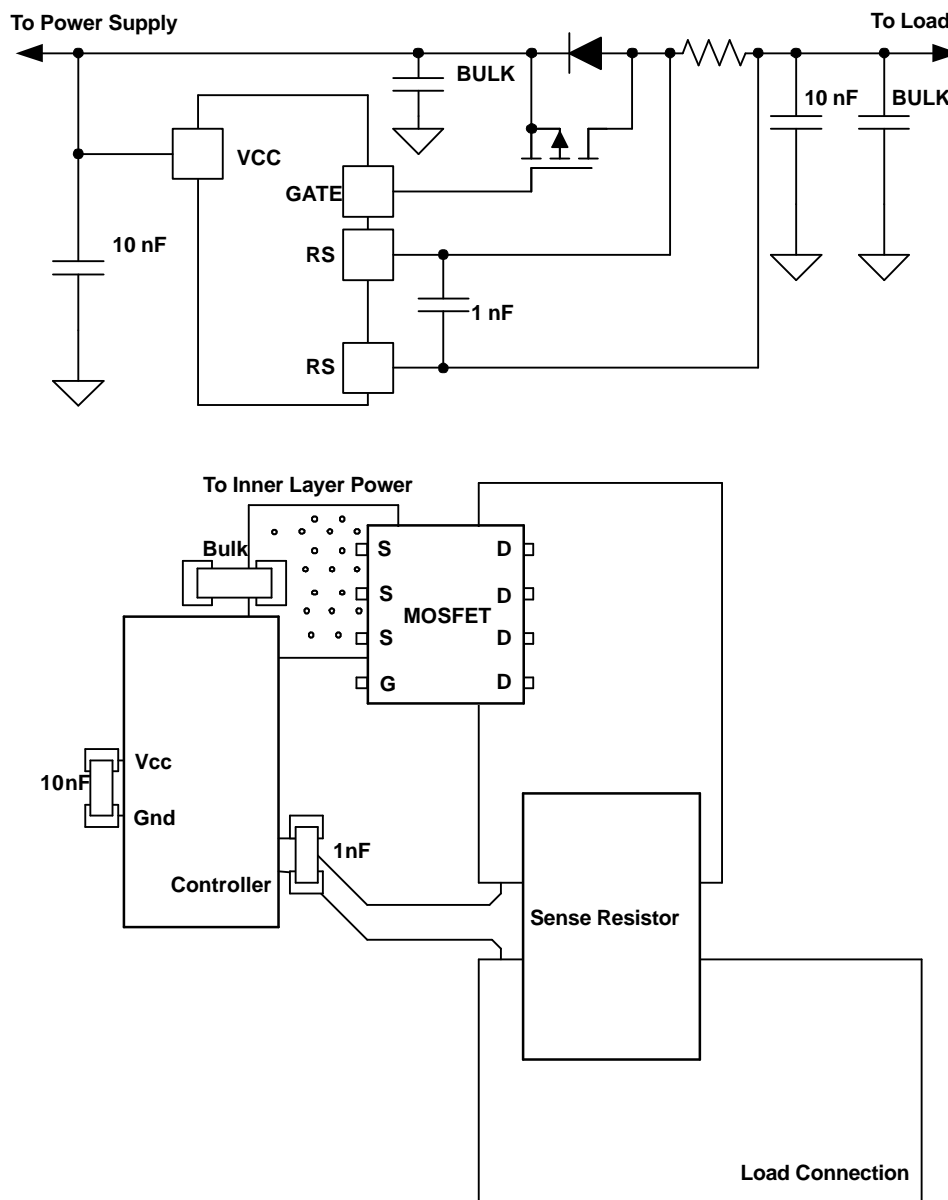
Figure 3. Sample Schematic and Layout

2.8 *Summary*

Providing the correct etch width, number of vias and adequate bypassing will reduce the debug time and speed the time to market. Noise and supply problems generate random errors that are often hard to track down, which take a lot of time. Following a basic set of power rules will reduce test time and time to market.

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