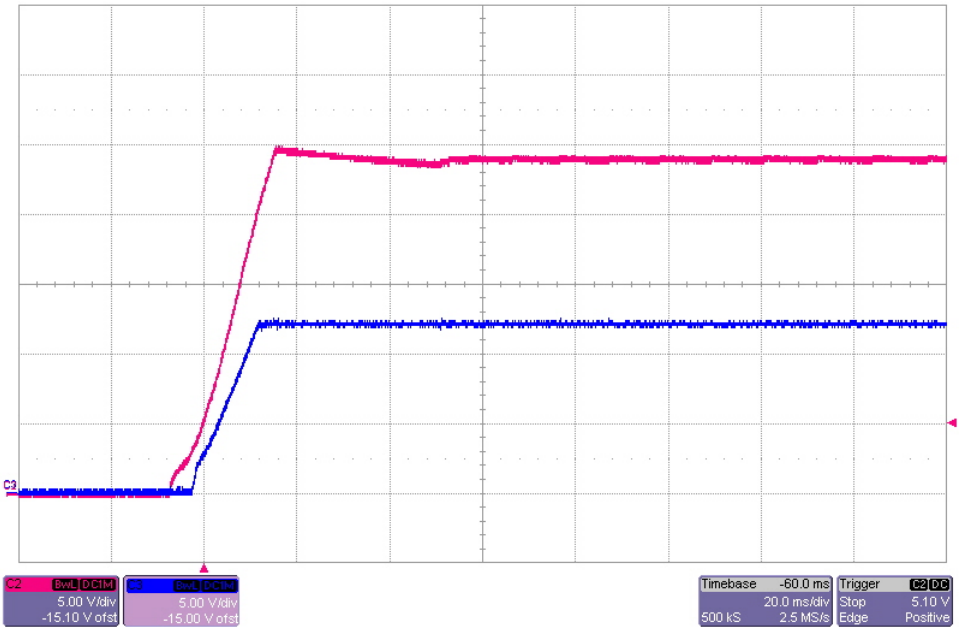
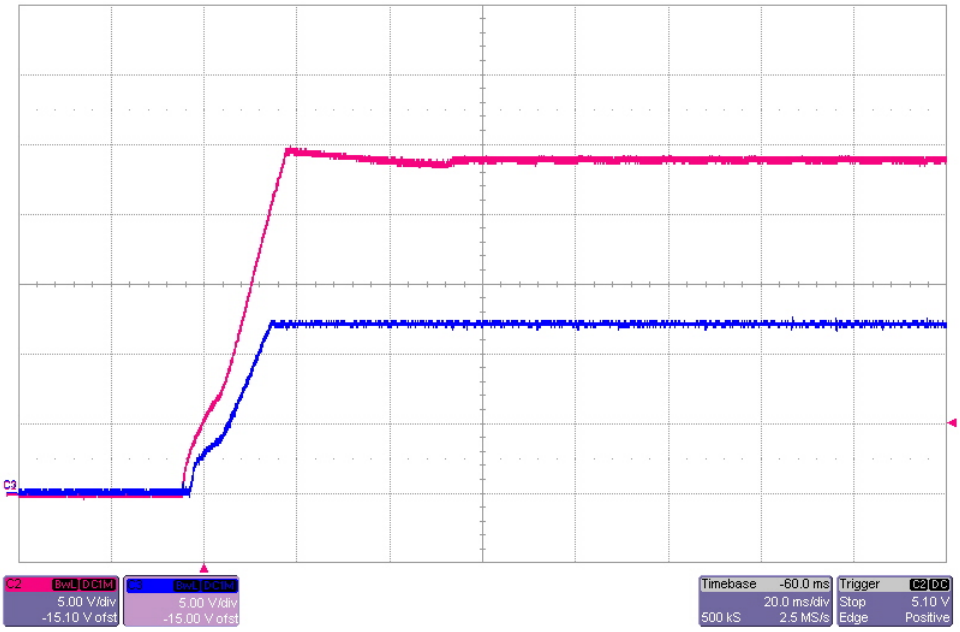
1 Startup

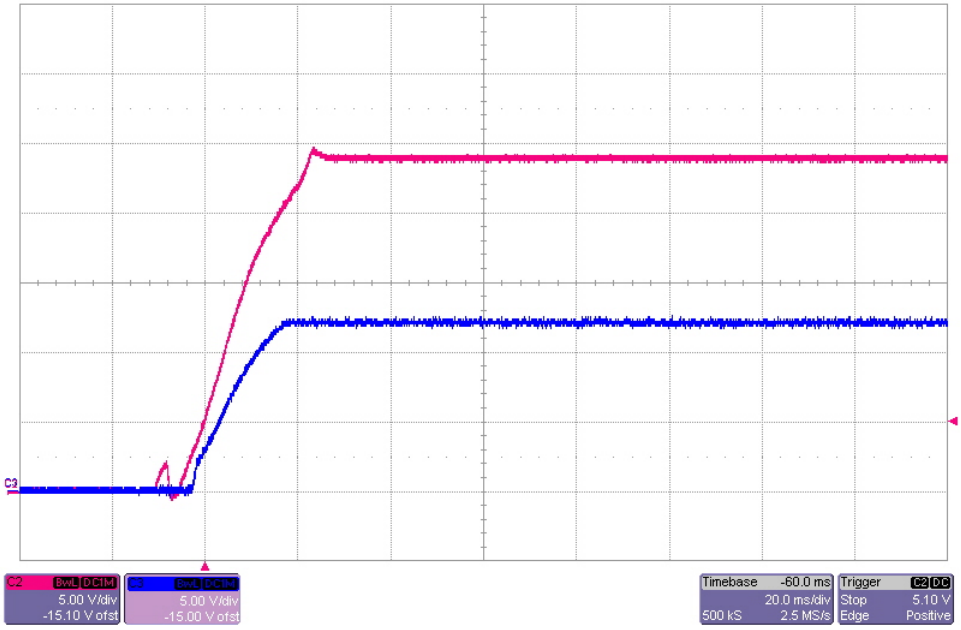
The photo below shows the 24V and 12V output voltage startup waveforms after the application of 115Vac. The outputs were loaded to 0A. (5V/DIV, 20mS/DIV)



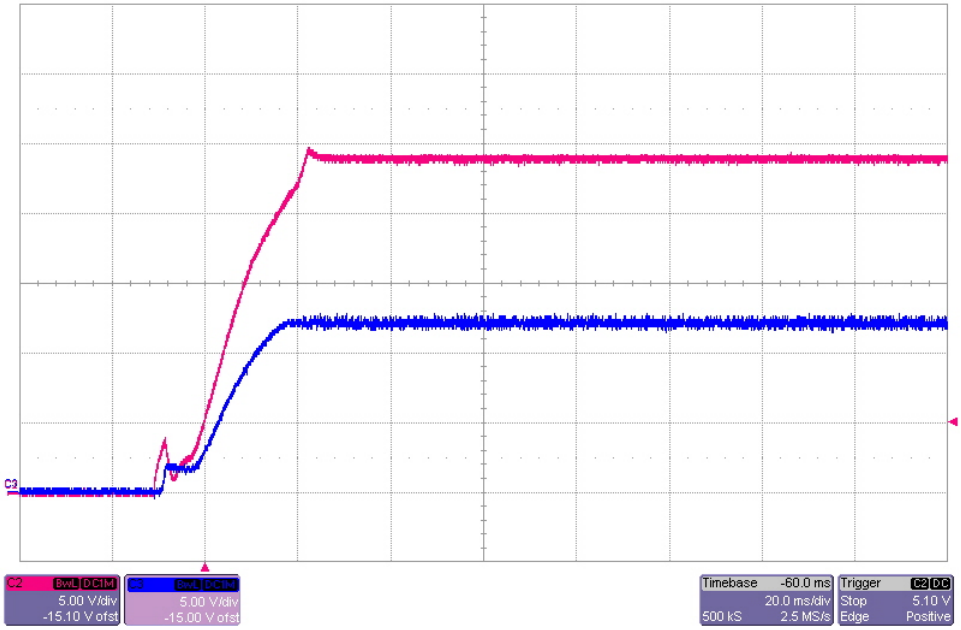
The photo below shows the 24V and 12V output voltage startup waveforms after the application of 230Vac. The outputs were loaded to 0A. (5V/DIV, 20mS/DIV)



The photo below shows the 24V and 12V output voltage startup waveforms after the application of 115Vac. The outputs were loaded to 80mA each. (5V/DIV, 20mS/DIV)

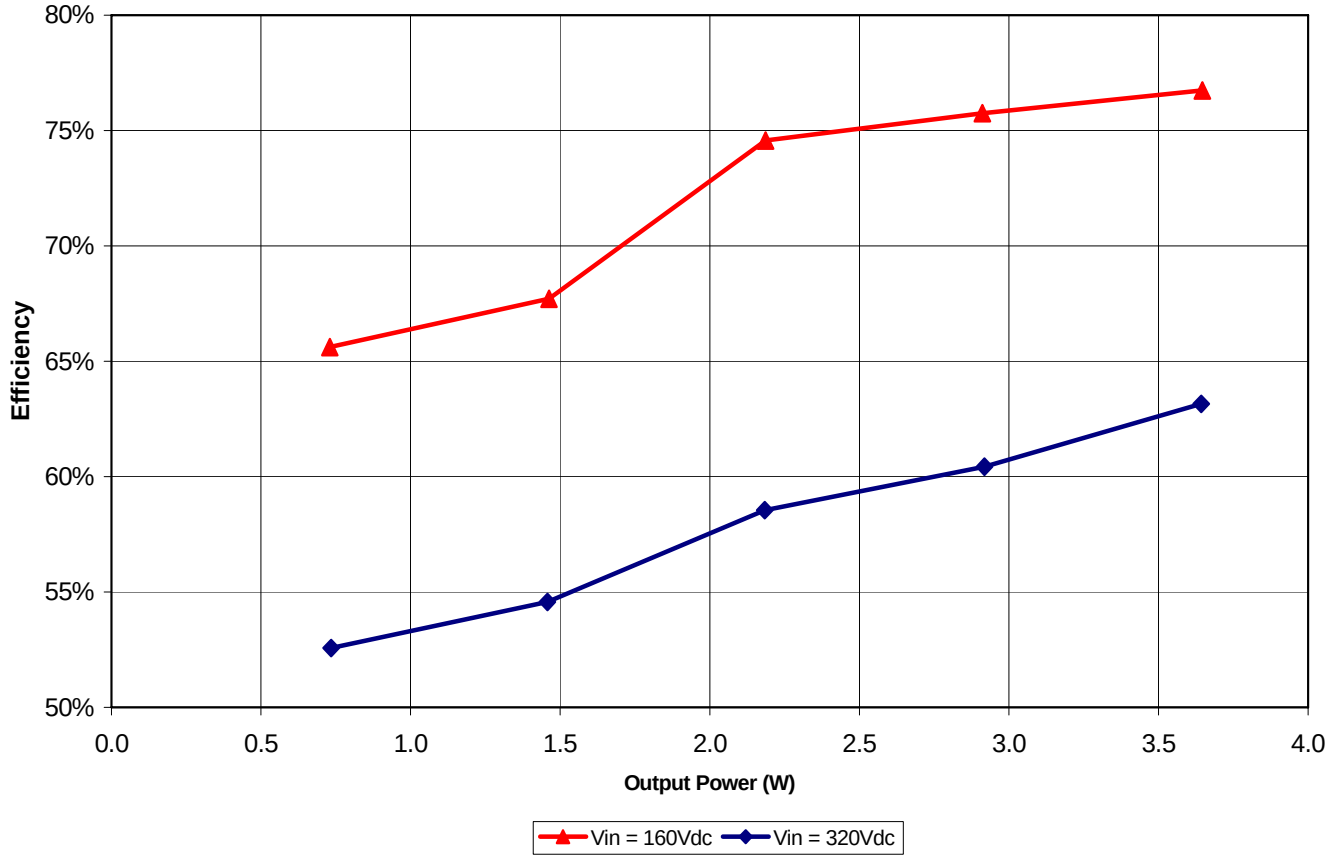


The photo below shows the 24V and 12V output voltage startup waveforms after the application of 230Vac. outputs were loaded to 80mA each. (5V/DIV, 20mS/DIV)



2 Efficiency

The converter efficiency is shown in the figure below. Both outputs were loaded equally.

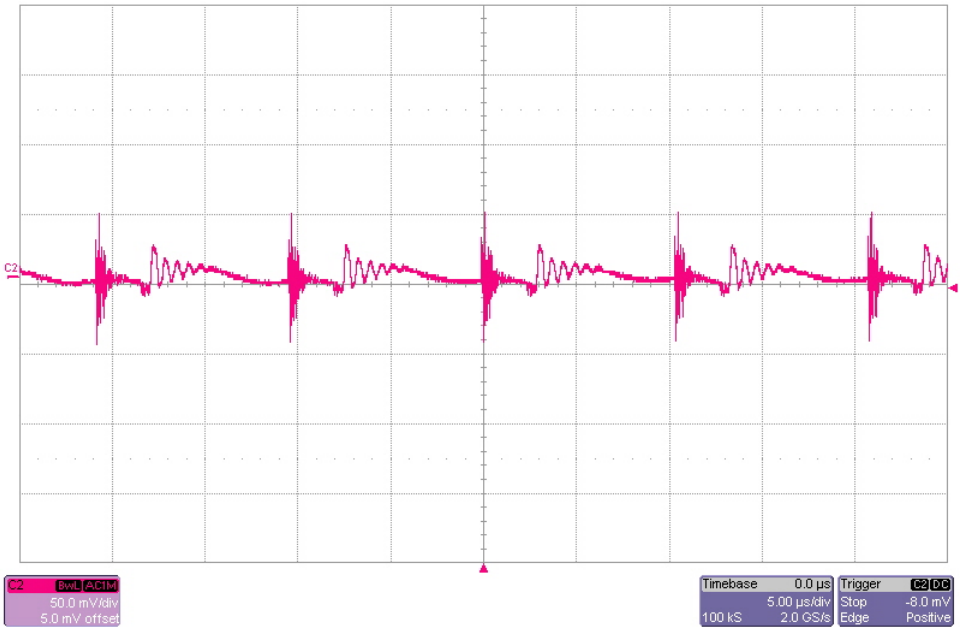


Cross Regulation Data

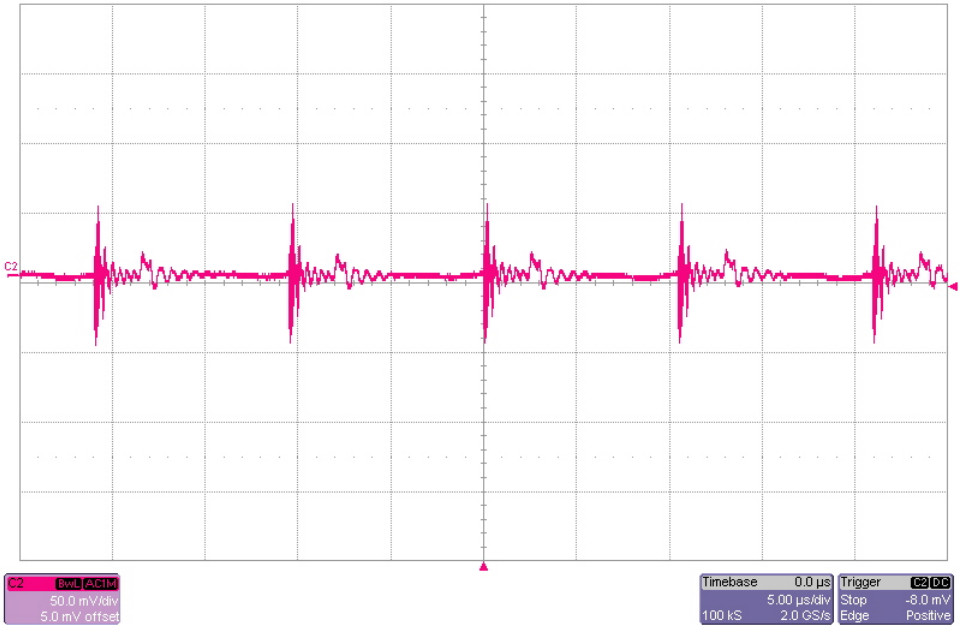
Vin = 115Vac				
24V output	**24V current**	**12V output**	**12V current**	**12V LDO input V**
24.22V	0A	12.04V	20mA	12.93V
24.22V	0A	12.10V	0A	14.79V
24.21V	80mA	12.09V	20mA	14.55V
24.21V	80mA	12.10V	0A	15.99V
24.21V	1.5mA	12.08V	100mA	12.58V
24.23V	0A	dropout	100mA	Dropout
Vin = 230Vac				
24V output	**24V current**	**12V output**	**12V current**	**12V LDO input V**
24.22V	0A	12.07V	20mA	13.00V
24.22V	0A	12.10V	0A	14.87V
24.20V	80mA	12.09V	20mA	14.54V
24.20V	80mA	12.10V	0A	15.91V
24.21V	2.5mA	12.05V	100mA	12.75V
24.22V	0A	dropout	100mA	Dropout

3 Output Ripple Voltage

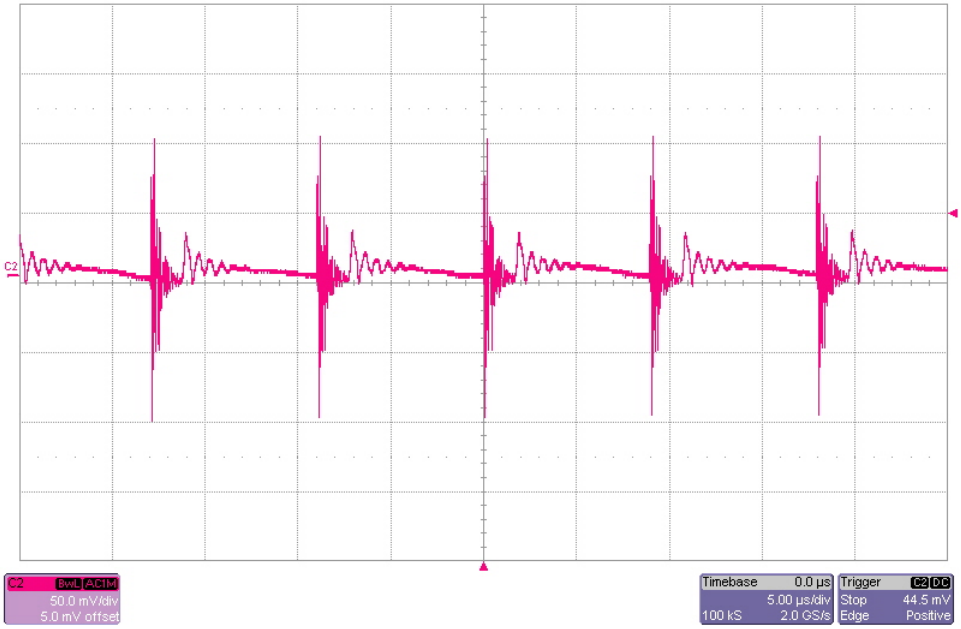
The 24V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 80mA and the input voltage set to 115Vac. (50mV/DIV, 5uS/DIV)



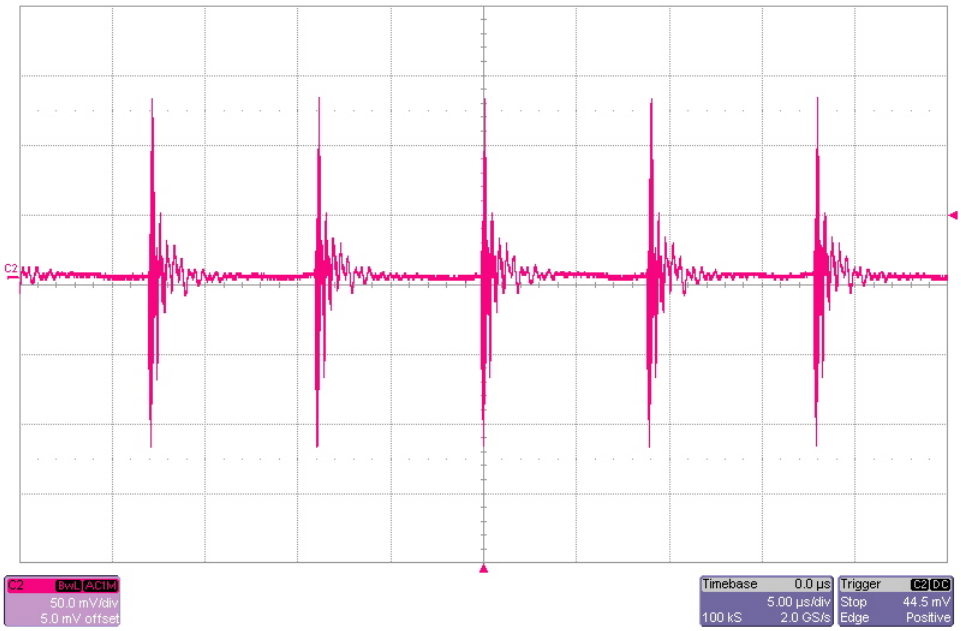
The 12V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 80mA and the input voltage set to 115Vac. (50mV/DIV, 5uS/DIV)



The 24V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 80mA and the input voltage set to 230Vac. (50mV/DIV, 5uS/DIV)

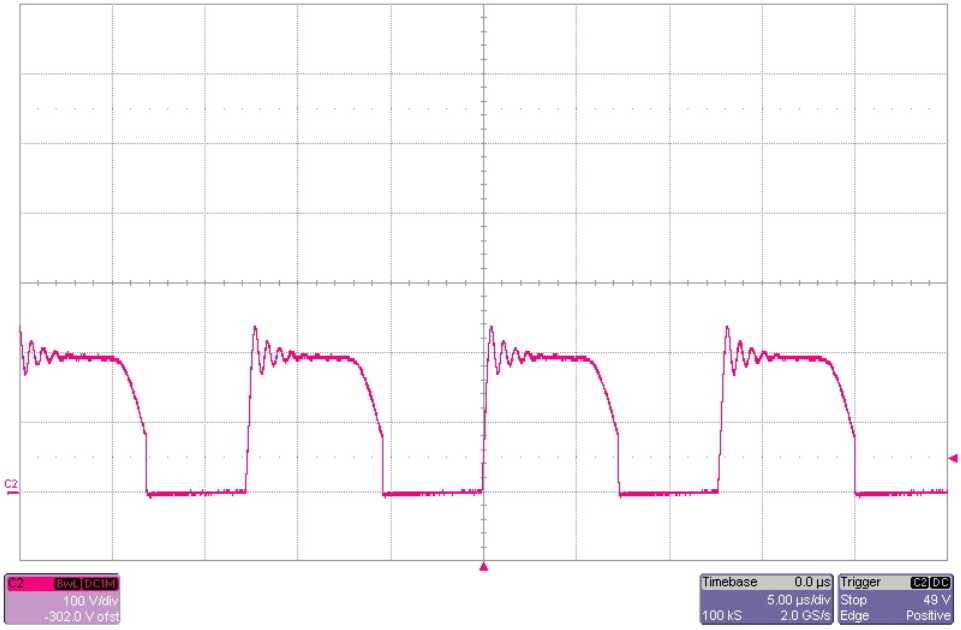


The 12V output ripple voltage is shown in the figure below. The image was taken with the output loaded to 80mA and the input voltage set to 230Vac. (50mV/DIV, 5uS/DIV)

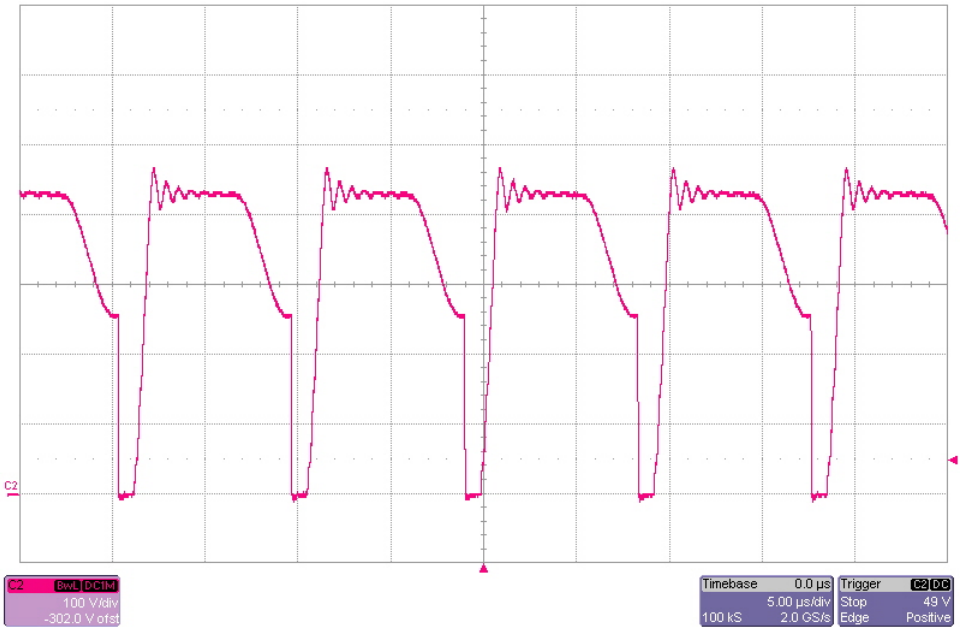


4 Switch Node Waveforms

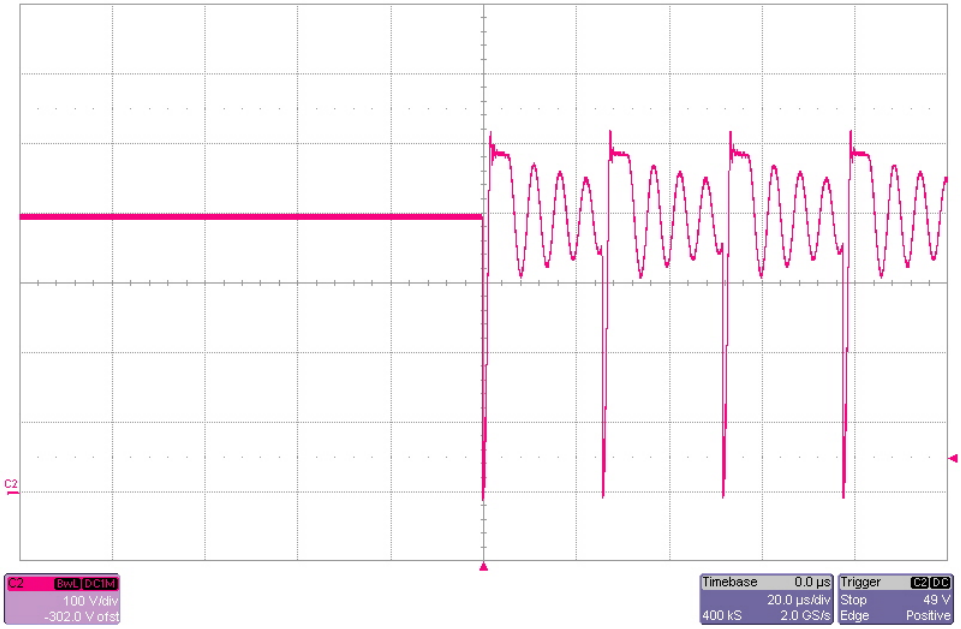
The photo below shows the switch node voltage of FET Q1 measured at TP11. The input voltage is 85Vac and the outputs are loaded to 80mA each. (100V/DIV, 5uS/DIV)



The photo below shows the switch node voltage of FET Q1 measured at TP11. The input voltage is 230Vac and the outputs are loaded to 80mA each. (100V/DIV, 5uS/DIV)

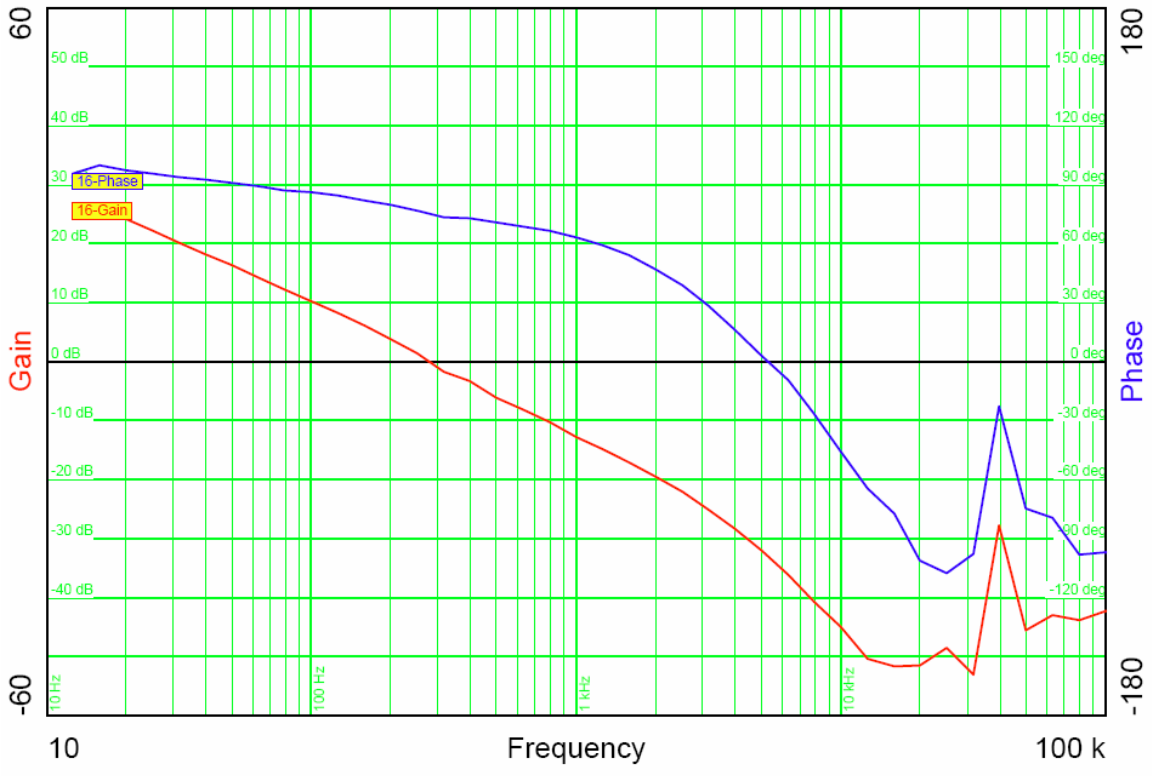


The photo below shows the switch node voltage of FET Q1 measured at TP11. The input voltage is 264Vac and the outputs are unloaded (0A). The controller is operating in skip mode. (100V/DIV, 20uS/DIV)



5 Control Loop Gain / Stability

The plot below shows the loop gain and phase margin with the input voltage set to 120Vdc and each output loaded to 80mA each. Band Width = 300Hz Phase Margin = 75 degrees



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