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TPS40002/3 Controllers Enable BUCK Converter Operating From 2.5-V Supply, (PR072)

Reference Design

TPS40002/3 Controllers Enable BUCK Converter Operating From 2.5-V Supply, (PR072)

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1 Introduction

The TPS40002 and the TPS40003 are voltage-mode, synchronous buck PWM controllers that utilize TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters operating from low 2.5-V logic power supplies. These controllers provide a bootstrap circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This reference design provides details on a 5-A buck converter that converts 2.5 V down to a 1.2-V level utilizing the TPS40003 controller, with less than 1 square inch board area.

A schematic for the board is shown in Figure 1. The list of materials is provided in section 6.

Specifications for the board follows:

- V_{IN} = 2.25 V to 3.3 V
- V_{OUT} = 1.2 V
- I_{OUT} = 0 A to 5 A
- Efficiency > 91% with a load from 1 A to 2 A, >87% at 4 A
- Output voltage ripple < 2% V_{OUT}
- Physical size < 1 square inch circuit area

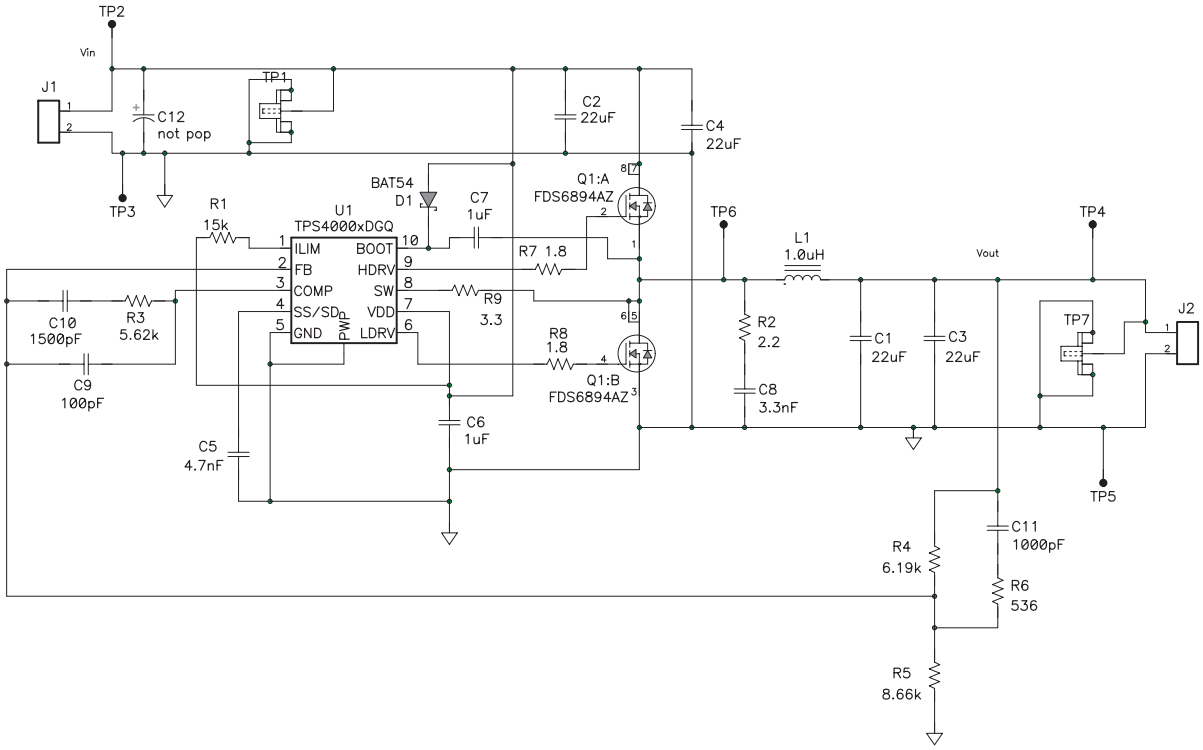


Figure 1. Application Diagram for the TPS40002/3

2 Design Procedure

2.1 TPS4000X Family Device Selection

The TPS4000X family of devices offers four selections to encompass the frequency and output current mode choices. The TPS40003 is selected for two major factors. First, the internal oscillator components set a fixed switching frequency of 600 kHz. This allows minimally sized filter components in this compact design. The second choice related to the TPS4000X family involves the selection of discontinuous current mode (DCM) operation or continuous current mode (CCM) operation at lighter loads. In this design, the TPS40003 is selected to keep the current continuous all the way to zero load, providing the most robust control characteristics.

2.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. The inductor value is calculated by equation (1).

$$L_{MIN} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \left(1 - \frac{V_{OUT}}{V_{IN(max)}} \right) \quad (1)$$

in which I_{RIPPLE} is chosen to be 25% of I_{OUT}, or 1.25 A in this example. This calculates to a value of 1.0 μH.

2.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this converter, a capacitor is required to supply the current required during the top MOSFET on-time while keeping ripple within acceptable limits. For this power level, input voltage ripple of 150 mV is reasonable, and the minimum capacitance is calculated in equation (2).

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{5\ A \times 606\ ns}{0.15\ V} = 20\ \mu F \quad (2)$$

To meet this requirement with the lowest size and cost, a single 22-μF, X5R ceramic capacitor can be considered. Although these capacitors have an extremely small resistance, the datasheet indicates that the part undergoes a 30°C temperature rise with 2-A_{RMS} current at 500 kHz. With V_{IN} = 3.0 V, our circuit requires nearly 2 A_{RMS} of current, so for a conservative design two capacitors are selected to allow for current derating. These capacitors function as power bypass components and should be located near the MOSFET package, to keep the high-frequency current flow in a tight loop. The low impedance characteristics of the dual ceramic capacitors help to reduce noise on the V_{DD} supply of the device. Specifically, the high-side MOSFET current sense is referenced to this point, so noise at the device must be kept to a low level.

2.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple, as given in equation (3).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \quad (3)$$

In this design, $C_{OUT(min)}$ is 10-µF. However, this only gives the capacitive component of the ripple voltage. In general, the voltage component due to the capacitor ESR must be considered, as in equation (4).

$$C_{ESR} \leq \frac{I_{RIPPLE}}{V_{RIPPLE}} \quad (4)$$

To allow margin in the output ripple voltage, two 22-µF ceramic capacitors are fitted in parallel. In this configuration the total ESR is below 3 mΩ, and contributes a negligible ripple component.

2.5 MOSFET Selection

The small physical size of this design requires the use of a single SO-8 package which contains dual N-channel MOSFETs. For this low input voltage application the MOSFETs should be capable of operation at gate-source voltages below 2.5 V. Also, Schottky diode D1 is added to enable the boostrap voltage to be nearly as large as V_{IN}. The $R_{DS(on)}$ for the MOSFETs is selected to be approximately 15 mΩ to 20 mΩ to keep the conduction losses to a manageable amount at full load.

2.6 Short Circuit Protection

The TPS40003 implements short circuit protection by comparing the voltage across the topside MOSFET while it is on to a voltage dropped from VDD by R_{LIM} due to an internal current source of 15 µA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET on-voltage versus temperature, the short circuit level can only protect against gross overcurrent conditions, and should be set larger than rated load. In this particular case, R_{LIM} is selected in equation (5).

$$R_{LIM} = R1 = \frac{3 \times \left(I_{OUT}\right) \times R_{DS(on)}}{15\ \mu A} \quad (5)$$

For this design, R_{LIM} = 15 kΩ, and the factor of 3 in the equation accounts for the variations in initial component tolerances and variations over temperature, especially in the power MOSFET. The high currents that are switched under short circuit conditions may cause SW pin 8 to be driven below ground several volts, possibly injecting substrate current which can cause improper operation of the device. A 3.3-resistor has been placed in series with this pin to limit its excursion to safe levels.

2.7 Compensation Design

The TPS40003 uses voltage mode control in conjunction with a high frequency error amplifier. The loop crossover frequency is set at 1/10 f_S, or 60 kHz. The power circuit L-C double pole corner frequency f_C is located at 24 kHz, and the output capacitor ESR zero is way out of the picture above 1 MHz. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve dc regulation.

The first zero is placed at approximately 2/3 f_C, 18.9 kHz,

$$f_{z1} = \frac{1}{2 \times \pi \times R_3 \times C_{10}} \tag{6}$$

The second zero is selected at f_C,

$$f_{z2} = \frac{1}{2 \times \pi \times \left(R_4 + R_6\right) \times C_{11}} \tag{7}$$

The two poles are place at one-half the switching frequency,

$$f_{p1} = \frac{1}{2 \times \pi \times R_3 \times \left[\frac{C_9 \times C_{10}}{\left(C_9 + C_{10}\right)}\right]} \tag{8}$$

and

$$f_{p2} = \frac{1}{2 \times \pi \times R_6 \times C_{11}} \tag{9}$$

Figure 2 shows the plots for the closed loop gain and phase with V_{IN} = 2.5 V and I_{OUT} = 2.2 A. At the crossover frequency of 58 kHz the phase margin is approximately 45 degrees.

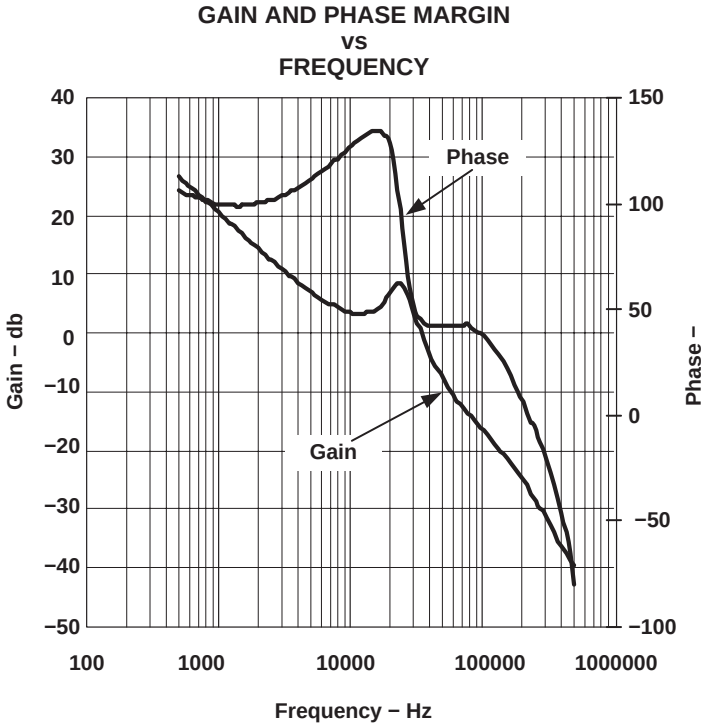


Figure 2.

2.8 Snubber Component Selection

The switch node where Q1 and L1 come together is very noisy. An R-C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q1:B. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit, Predictive Gate Drive™, and DCM control functions.

As a starting point, the snubber capacitor C8 is generally chosen to be five to eight times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q1:B. Since C_{OS} is 440pF for Q1:B, C8 is chosen to be 3.3 nF. R2 is empirically determined to be 2.2 Ω, which minimizes the ringing and overshoot at the switch node. With low input voltages the power loss, ½ CV^2f , is relatively small at 24 mW.

3 PowerPAD™ Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, the integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The leadframe die pad is exposed on the bottom side of the package, and can be soldered to the PCB using standard solder flow techniques when maximum heat dissipation is required. However, in many applications the PowerPAD™ does NOT have to soldered to the PCB.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package whether the package needs to be soldered or not. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this would reduce the copper area to transfer heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical construction would utilize one or two vias of 0.013" diameter plated with 1 ounce copper in the land under the TPS40003. A typical land pattern is shown in Figure 3, but does not include the copper encompassing the vias above and below the device. These vias can increase the heat dissipation but are not always necessary.

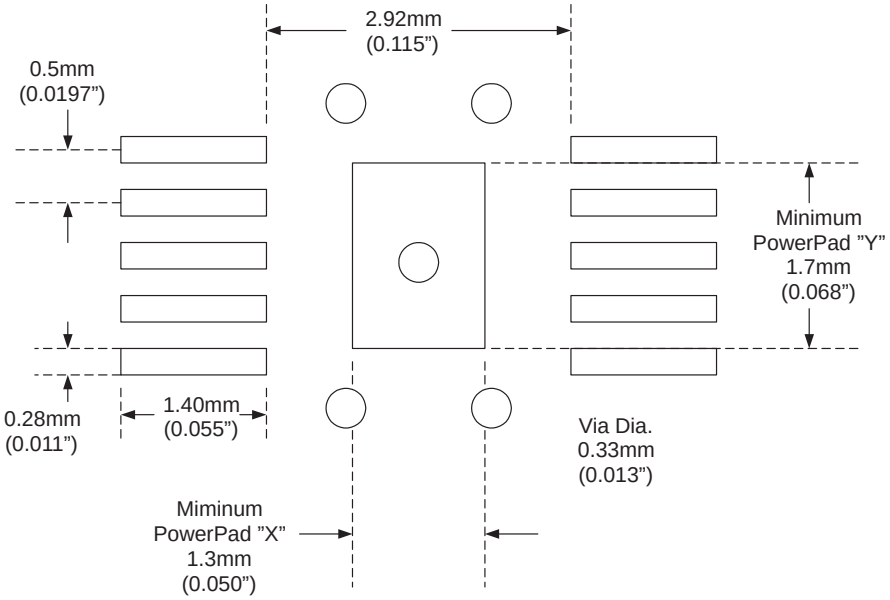


Figure 3. PowerPAD PCB footprint information

The exas Instrument document, *PowerPAD ™ Thermally Enhanced Package Application Report* (TI Literature Number SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

4 Test Results/Performance Data

Typical efficiency curves are shown in Figure 4 for a nominal 2.5-V input.

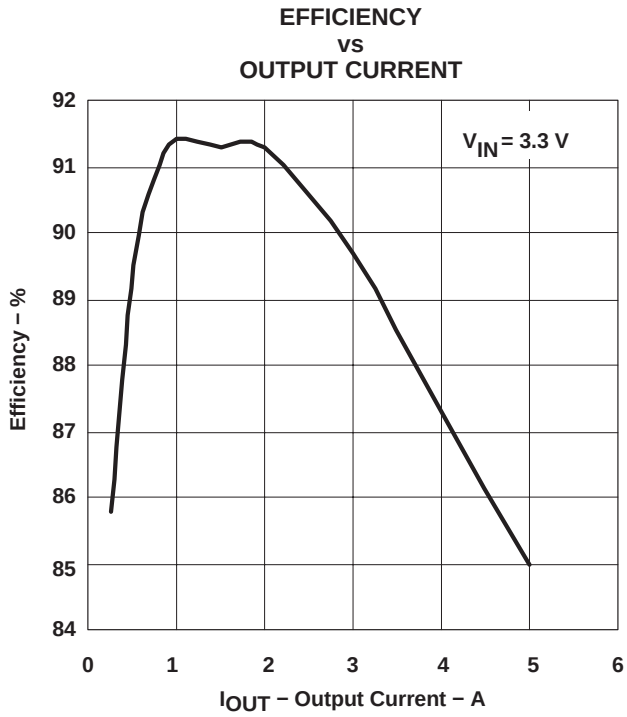


Figure 4.

Figure 5 shows the switch node during typical operation at full load. Note that this 600-kHz design has very minimal body diode conduction in the bottom MOSFET as a result of using the Predictive Delay™ control implementation. This technique is able to dynamically change the delays in the MOSFET drive circuit to account for variations in line, load, and between devices.

TYPICAL SWITCH NODE WAVEFORM

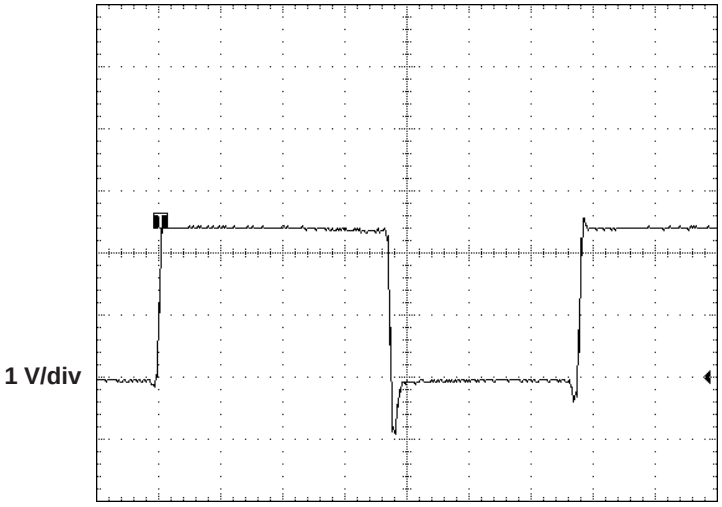


Figure 5.

The output voltage ripple is shown in Figure 6.

OUTPUT VOLTAGE RIPPLE

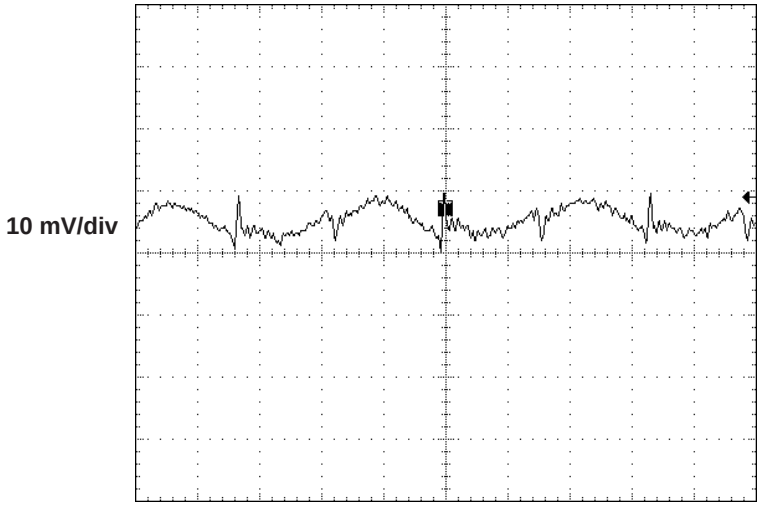
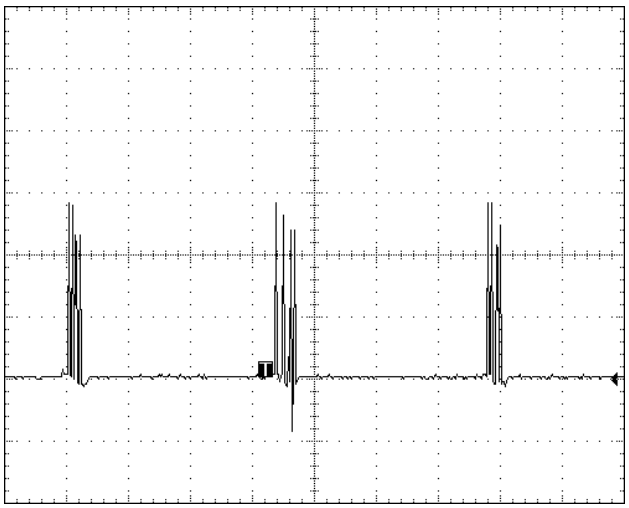


Figure 6.

Operation during a short circuit fault is shown in Figure 7. Note that there are six softstart intervals between successive groups of pulses when the power devices are not switched. This leads to an extremely low input power level for the duration of the fault, and the power circuit is not overstressed.

SHORT CIRCUIT RESTART INTERVAL



t − Time − 2 ms/div

Figure 7.

5 PCB Layout

PCB layout details are available in both Gerber and PCAD formats.

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