Texas Instruments

Using the Optical Network Hot Swap Power Manager Reference Design

Reference Design

Using the Optical Network Hot Swap Power Manager Reference Design (TPS2346)

Andy Ripanti *Power Interface Products*

ABSTRACT

The TPS2346 optical network hot swap power manager (HSPM) provides highly integrated supply control of three positive (3.3-V, 5-V, and 5.15-V) and one negative (–5.2-V) supply rails with a minimum number of external components. A linear current amplifier (LCA) in each of the four device channels provides closed-loop control of load current during insertion and extraction events. This allows the designer to configure the plug-in card's maximum inrush slew rate and magnitude according to the requirements of the system power supplies. This document describes the use of an available reference design board to evaluate the TPS2346 device.

CONTENTS

1 Introduction

This reference design describes the use and features of the optical network hot swap power manager reference design. This board features the Texas Instruments (TI) TPS2346 optical network hot swap power manager integrated circuit, a four-supply controller used to enable hot swap capability in systems needing to swap up to four power supplies across a connector interface. The device features programmable inrush current control, electronic circuit breakers, power-up and power-down sequencing, logic enable input, and load fault indicator. The optical network (ONET) hot swap reference design is a PCB-based tool used to demonstrate the performance and operation of the TPS2346 device in simulated live insertion and removal actions.

1.1 Features

The following list highlights some of the features of the TPS2346 device.

- Enables hot swap in high availability optical network systems
- Programmable current slew rate
- Power supply sequencing
- Peak current (IMAX) programmable via sense resistors
- Overcurrent circuit breaker at 2x IMAX
- Precharge output
- Logic low power good output
- Logic low enable input
- On-chip charge pump
- Low sleep mode current
- Undervoltage lockout (UVLO)
- 24-pin TSSOP package

1.2 Description

The TPS2346 optical network hot swap power manager (HSPM) provides highly integrated supply control of three positive (3.3-V, 5-V, and 5.15-V) and one negative (–5.2-V) supply rails with a minimum number of external components. A linear current amplifier (LCA) in each of the four device channels provides closed-loop control of load current during insertion and extraction events. This allows the designer to configure the plug-in card's maximum inrush slew rate and magnitude according to the requirements of the system power supplies.

After an add-in card insertion, once all input supplies are above undervoltage levels, and the $\overline{\text{ENABLE}}$ input is a logic low, the TPS2346 will begin application of power to the back-end power planes. Switching of the back-end power is achieved via four external N-channel MOSFETs. Current to each supply plane is ramped at a programmed rate set by a capacitor on the current ramp pin (IRAMP), with supplies sequenced in the order 5.15 V, 5 V, 3.3 V and –5.2 V. The peak charging current on each channel is limited to an individually programmable value, or IMAX. If the IMAX level is achieved during insertion events, charging of the card's input bulk capacitance completes at that current level, as required.

As each back-end voltage is ramped in turn, its level is validated to ensure it is within the established tolerances. A timer, also derived from the current ramp capacitor, sets a time limit for ramping each channel, protecting systems from start-up into faulted loads. If all four supplies reach a known-good state, the $\overline{\text{PG}}$ output is pulled low to allow enumeration of the add-in card. At this point, all four gate outputs are driving to an internal supply rail in order to fully enhance the external MOSFETs, producing a low-impedance power path for each load. An on-chip charge pump circuit boosts the Channel 1 input supply to provide sufficient gate overdrive to achieve minimum on-state resistance.

To further protect the backplane power bus, electronic circuit breakers provide continuous protection for the system supplies during plug-in operation. If any channel trips its circuit breaker, all supply outputs will be rapidly turned off, and remain latched off. Also, the $\overline{PG}$ output becomes high impedance. The TPS2346 can be reset by cycling either the $\overline{ENABLE}$ input or power to the device.

Controlled shutdown and power isolation of a plug-in is initiated by pulling the $\overline{ENABLE}$ pin high during a healthy supply state. The TPS2346 responds by ramping down each back-end voltage in the reverse order of the turn-on sequence.

The precharge output pin (PRECHG) provides a 1-V bias supply. This supply can be used for precharge of the module's address and data lines during insertion (and extraction) events, to help minimize perturbations of the bus signals. The precharge circuitry is active whenever the 5-V supply is applied to the VIN2 input.

2 The Optical Network Hot Swap reference design Kit

The optical network reference design kit is a two-board platform that enables designers to rapidly learn about the TPS2346 operation, and evaluate its performance during hot swap events. The main evaluation board (TI board number SLUP156) is divided into two sections, one simulating the backplane side of a target application system, and one containing the power interface section of a plug-in card as it may be implemented on a hot swap capable ONET card. On the main PCB, the two subsections are essentially isolated. The jumper card (TI board number SLUP159), when inserted into the main board's P1 connector, provides a mechanism for simulating hot swap events by abruptly applying power, ground and control signals on the backplane side to their corresponding inputs on the plug-in side.

2.1 The Optical Network Hot Swap Reference design Main Board

2.1.1 Module Description

The optical network reference design main board is divided into two separate circuits. When oriented such that the board nomenclature is upside right to the user, the left side of the board represents the backplane side of the hot swap interface; the right side represents the plug-in module side. This half contains the power isolation and control electronics comprising a TPS2346-based hot swap interface. In addition, the right side of the main board contains some additional switches and components that can be used to facilitate device testing and for quick modifications of the plug-in characteristics. The two PCB sections connect to a 44-pin PCB edge connector (P1). Mate and demate of the plug-in is accomplished by inserting and removing the jumper card.

The backplane side of the main board contains banana jacks and PCB headers for the connection of the user's power supplies for the four input supply voltages: 5.15 V, 5 V, 3.3 V, and –5.2 V. Each input supply plane also contains some amount of bulk capacitance. Providing some bulk capacitance in close proximity to each slot connector generally improves hot swap performance.

The plug-in side of the main board contains the TPS2346 optical network HSPM device, four power MOSFET switches, and some configuration capacitors. Two through-hole patterns are provided for each of the four back-end planes for the installation of large-value aluminum electrolytic capacitors. These capacitors simulate the input bulk capacitance that may be found on the target module's back-end supply nodes. Jumpers are provided for the quick connection or disconnection of these capacitors to the individual back-end nodes, for easy reconfiguration of the load characteristics. Table 9 lists the default capacitor values supplied with the board.

In addition, banana jacks and PCB headers are provided on the back-end planes for easy hook-up of the user's resistive or electronic loads for simulation of the target application's load current levels, if desired.

The pictorial of the optical network hot swap board top assembly is shown in Figure 1.

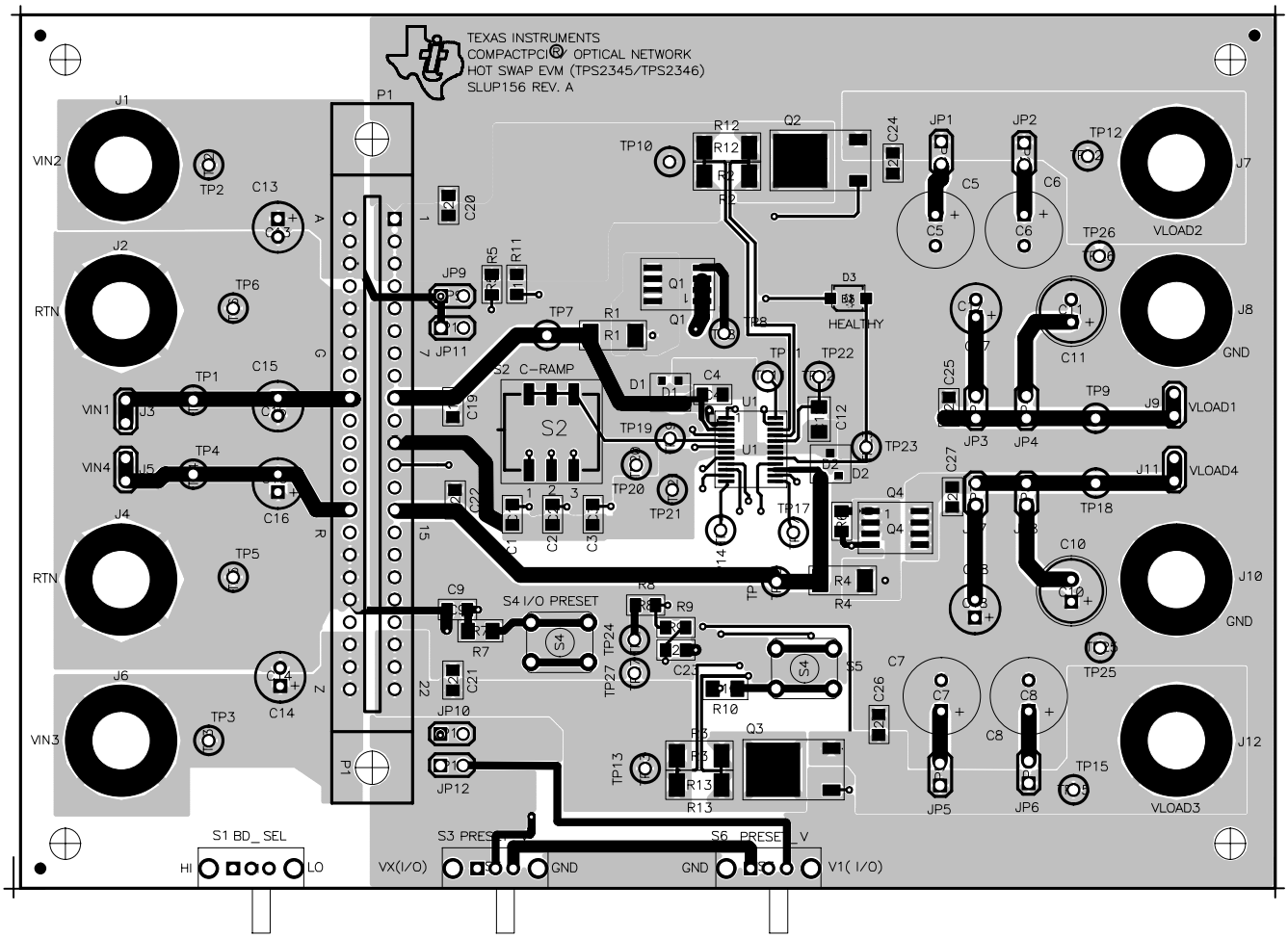

Figure 1. Reference Design Main Board Top Assembly

Load current slew rate programming of the TPS2346 device is achieved with a single external capacitor on the IRAMP pin. On the reference design, this is accomplished by selecting from among three pre-installed capacitors. The capacitors are easily selected or disconnected via the individual DIP switches of S2.

The TPS2346 contains an on-chip regulator which can be used as a bias supply for precharging the bus I/O lines if required. The reference design plug-in section contains circuitry to demonstrate the precharge output, including jumpers to select the V(I/O) level (5 V or 3.3 V), and components to simulate I/O line RC characteristics.

Test points are provided throughout the circuit for waveform monitoring. The test point connections are listed in Table 8.

2.1.2 Reference design Schematic Diagram and List of Materials

The reference design main board schematic diagram is shown in Figures 2 and 3.

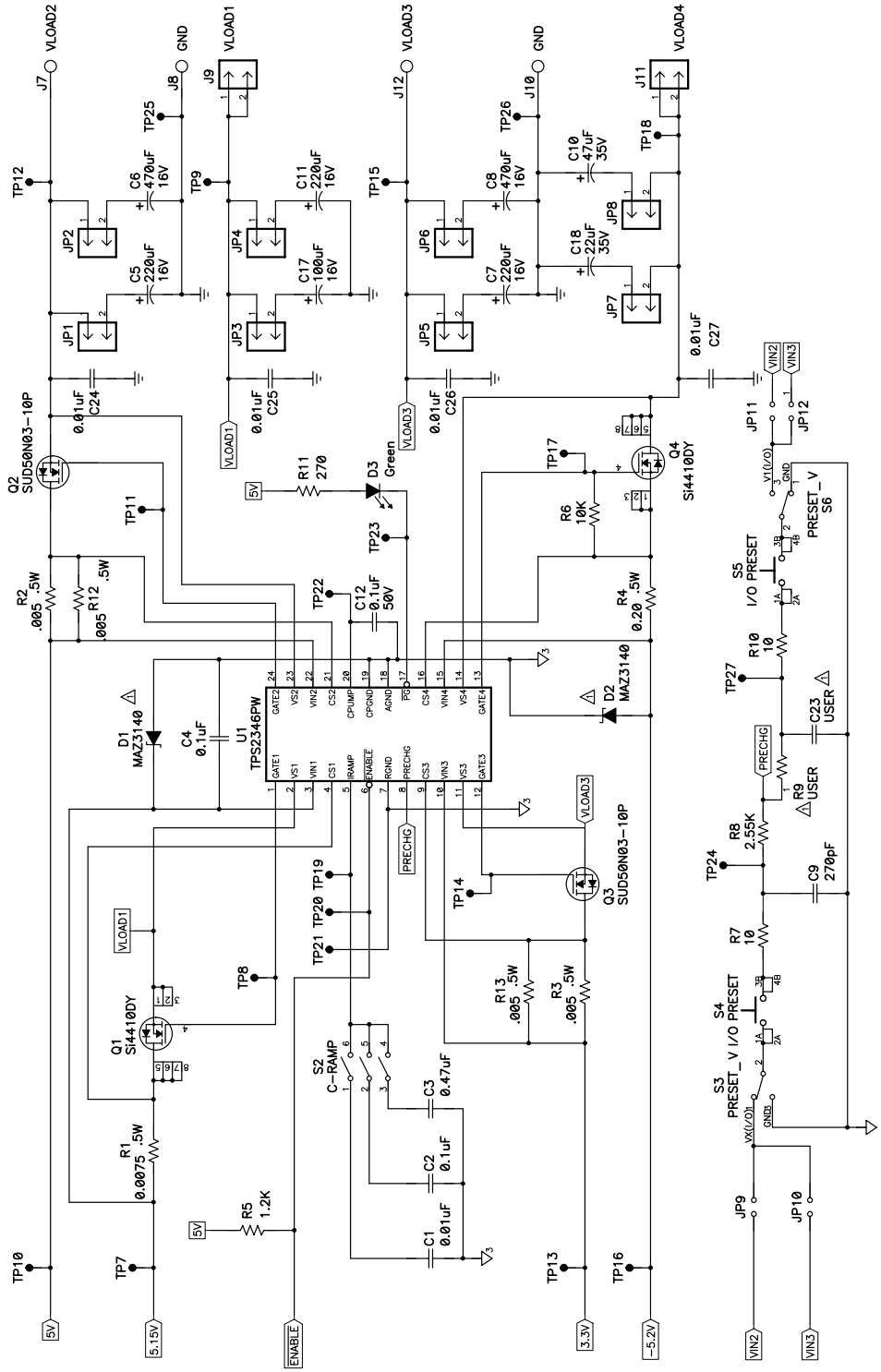

Figure 2. Optical Network Hot Swap Power Manager Reference Design Schematic (Sheet 1)

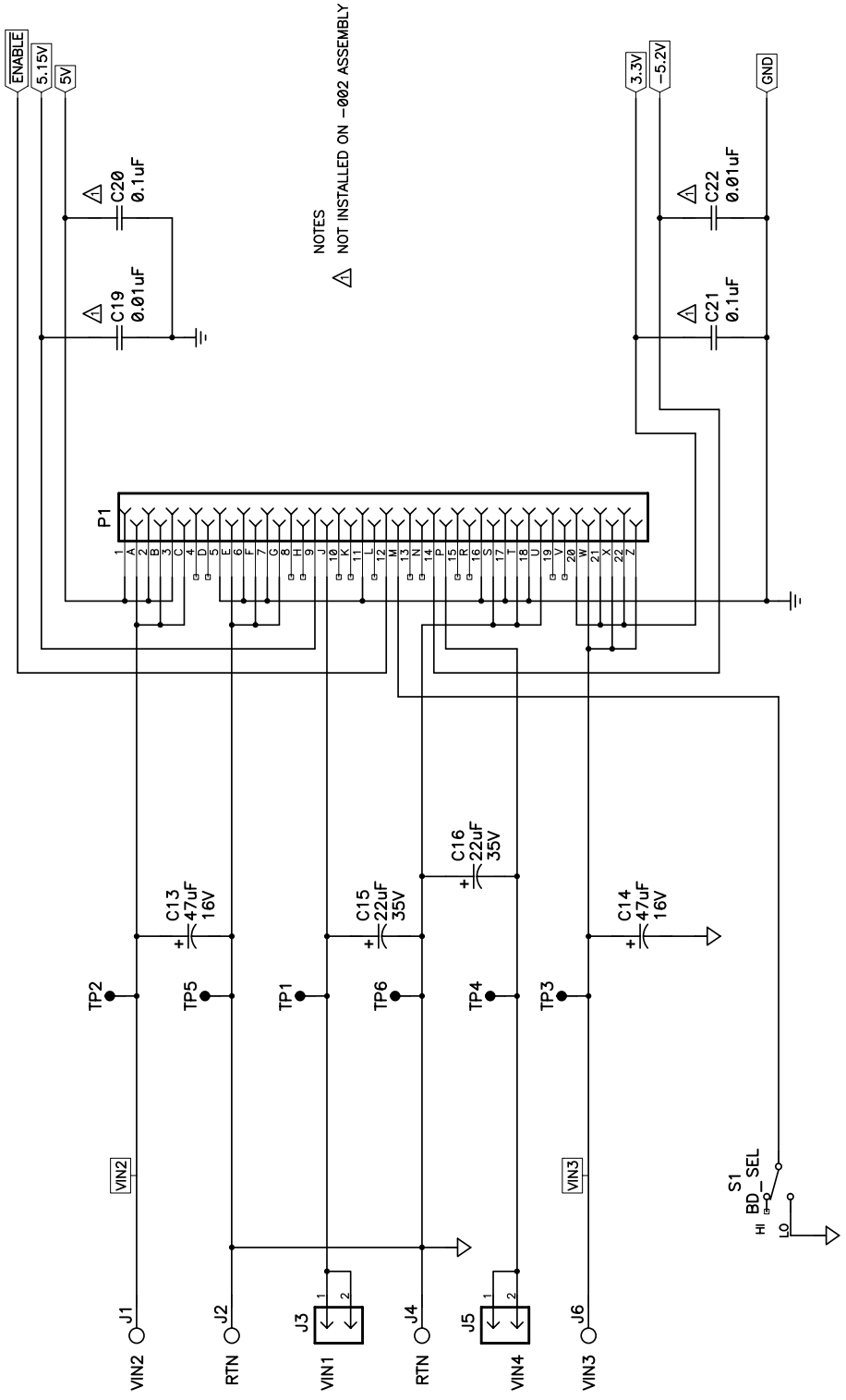

Figure 3. Optical Network Hot Swap Power Manager Reference Design Schematic (Sheet 2)

Table 1. Optical Network Hot Swap Reference Design List of Materials

REF DES	QTY	DESCRIPTION	MFGR	PART NUMBER
C10	1	Capacitor, aluminum electrolytic, 47 μF, 35 V, 20%	Panasonic	EEU–FC1V470
C15, C16, C18	3	Capacitor, aluminum electrolytic, 22 μF, 35 V, 20%	Panasonic	EEU–FC1V220
C6, C8	2	Capacitor, aluminum electrolytic, 470 μF, 16 V, 20%	Panasonic	ECA–1CM471
C5, C7, C11	3	Capacitor, aluminum electrolytic, 220 μF, 16 V, 20%	Panasonic	ECA–1CM221
C17	1	Capacitor, aluminum electrolytic, 100 μF, 16 V, 20%	Panasonic	ECA–1CM101
C13, C14	2	Capacitor, aluminum electrolytic, 47 μF, 16 V, 20%	Panasonic	EEU–FC1C470
C12	1	Capacitor, ceramic, 0.1 μF, 50 V, 20%, Z5U	Vitramon	VJ1206U104MXAA
C23		Capacitor, ceramic, 0805	Standard	Standard
C9	1	Capacitor, ceramic, 270 pF, 50 V, 10%, C0G	Vitramon	VJ0805A271KXAA
C4	1	Capacitor, ceramic, 0.1 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U104MXXA
C20, C21		Capacitor, ceramic, 0.1 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U104MXXA
C19, C22		Capacitor, ceramic, 0.01 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U103MXXA
C24–C27	4	Capacitor, ceramic, 0.01 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U103MXXA
C3	1	Capacitor, ceramic, 0.47 μF, 16 V, 10%, X7R	Panasonic	ECJ–2FB1C474K
C2	1	Capacitor, ceramic, 0.1 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y104KXJA
C1	1	Capacitor, ceramic, 0.01 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y103KXJA
P1	1	Connector, 44-pin, PCB vert., .100 cntrs	Tyco	530843–4
D1, D2		Diode, zener, SC–59		
D3	1	Diode, LED, green, GW type	Panasonic	LN1361C
J3, J5, J9, J11, JP1 – JP12	16	Header, 2-pin, Sgl Row, .100 cntr., .025 sq., .230 head	Sullins	PTC36SAxN
N/A	10	Jumper, 2-pin, 0.100 cntr	Sullins	STC02SYAN
Q2, Q3	2	MOSFET, XSTR, , N–Chan, V(BR) > 30 V	Vishay – Siliconix	SUD50N03–10P
Q1, Q4	2	MOSFET, XSTR, N-Channel, V(BR) > 30 V	Vishay – Siliconix	Si4410DY
N/A	1	Connector, keying, plug, intercontact	Tyco	650025–2
R4	1	Resistor, 0.20 Ω, 0.5 W, 1%	Vishay	WSL–2010 .200<1%
R1	1	Resistor, 0.0075 Ω, 0.5 W, 1%	Vishay	WSL–2010 .0075<1%
R2, R3, R12, R13	4	Resistor, 0.005 Ω, 0.5 W, 1%	Vishay	WSL–2010 .005<1%
R7, R10	2	Resistor, 10 Ω, 0.125 W, 5%	Venkel	CR1206–8W100J
R9		Resistor, 0.1 W, 5%, 0805	Standard	Standard
R6	1	Resistor, 10 kΩ, 0.1 W, 5%	Venkel	CR0805–10W103J
R5	1	Resistor, 1.2 kΩ, 0.1 W, 5%	Venkel	CR0805–10W122J
R11	1	Resistor, 270 Ω, 0.1 W, 5%	Venkel	CR0805–10W271J
R8	1	Resistor, 2.55 kΩ, 0.1 W, 1%	Venkel	CR0805–10W2551F

REF DES	QTY	DESCRIPTION	MFGR	PART NUMBER
N/A	4	Screw, nylon, round head, #6–32, 0.25 in.	Eagle	010632R025
N/A	4	Spacer, nylon, Hex, #6–32, 0.625 in.	Eagle	14HTSP020
S1, S3, S6	3	Switch, slide, SPDT, Rt. angle, 200 mA	E–Switch	EG1213
S2	1	Switch, dip, 3 Pos., SPST	CTS	219–03MS
S4, S5	2	Switch, momentary, NO, 1.6N	Panasonic	EVQ–PAE0xy
TP5, TP6, TP21, TP25, TP26	5	Test Point, jack, black	Farnell	240–333
TP1–TP4, TP7–TP20, TP27, TP22–TP24	22	Test Point, jack, red	Farnell	240–345
J1, J2, J4, J6, J7, J8, J10, J12	8	Test Point, banana, non-insulated, PCmnt.	Pomona	3267
U1	1	Optical network hot swap power manager	Texas Instruments	TPS2346PW
N/A	1	PCB, FR–4, 2 layer, SM0BC, 5.6”x3.9”, 0.062”thick	Texas Instruments	SLUP156
N/A	1	PCB, FR–4, 2 layer, SM0BC, 2.33”x2.3”	Texas Instruments	SLUP159

2.2 The Optical Network Reference design Jumper Card

2.2.1 Description

The reference design jumper card is used to apply the four supply voltages, present at the input banana jacks, to the four supply inputs of the main board’s plug-in side. Inserting and removing the jumper card into and out of the main board P1 connector simulates hot swap events. There are no components mounted on the jumper card; it simply makes the point-to-point connections to apply input power to the plug-in electronics. This mechanism allows the kit’s main board, which may have several scope probes and meter leads connected to it during use, to remain stationary on the user’s bench.

A pictorial of the jumper card top layer is shown in Figure 4.

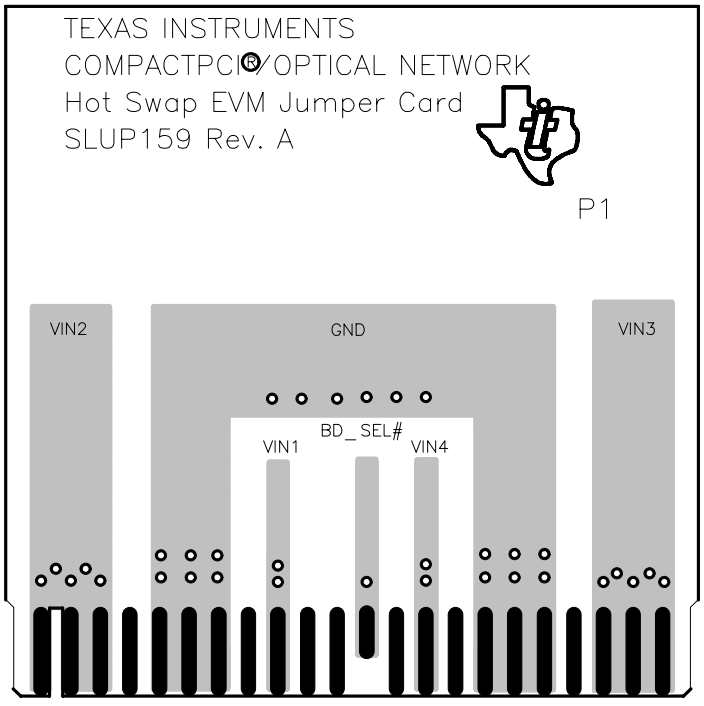

Figure 4. Jumper Card Top Assembly

2.2.2 Jumper Card Schematic Diagram and List of Materials

The reference design jumper card schematic diagram is shown in Figure 5.

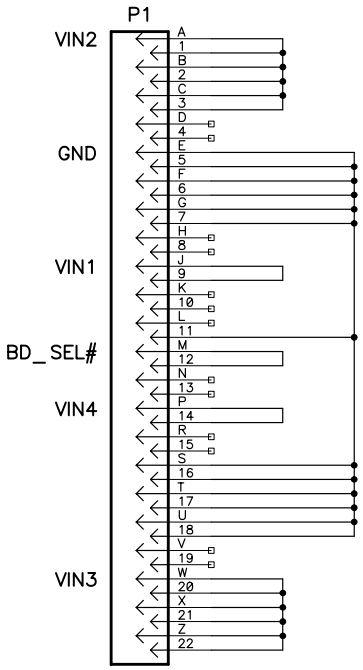

Figure 5. Jumper Card Schematic

There are no components installed on the jumper card, and consequently no list of materials required.

2.3 Optical Network Hot Swap Reference design Operating Specifications

The optical network hot swap reference design and jumper card were designed for some degree of user reconfiguration, as described later in Section 4, Using the reference design to evaluate the TPS2346 HSPM device. This includes modifications for different load current requirements. However, under no circumstances should the kit be operated beyond the input supply and load currents specified in Table 2.

Table 2. Reference Design Absolute Maximum Ratings[1,2]

PARAMETER	MIN	MAX	UNITS
Channel 1 supply voltage range, VIN1	–0.3	15	V
Channel 2 supply voltage range, VIN2	–0.3	15	V
Channel 3 supply voltage range, VIN3	–0.3	15	V
Channel 4 supply voltage range, VIN4	–15	0.3	V
Load current, VLOAD1		–3	A
Load current, VLOAD2		–9	A
Load current, VLOAD3		–9	A
Load current, VLOAD4		1.9	A
Load return current, J8, J10		12	A
Supply return current, J2, J4		–12	A
Ambient Operating Temperature Range	–40	85	°C

NOTES: 1. All voltages are with respect to PCB RTN node, J2 or J4.
2. Currents are positive into and negative out of the specified terminal.

Component selection for the design was done to configure the circuit for a typical application. As such, the target operating conditions, for the factory-installed component values, are as shown in Table 3.

Table 3. Optical Network Reference Design Recommended Operating Conditions[1,2]

PARAMETER	MIN	NOM	MAX	UNITS
Nominal supply voltage, VIN1		5.15		V
Nominal supply voltage, VIN2		5.0		V
Nominal supply voltage, VIN3		3.3		V
Nominal supply voltage, VIN4		–5.2		V
Load current, VLOAD1			–2.0	A
Load current, VLOAD2			–6.0	A
Load current, VLOAD3			–6.0	A
Load current, VLOAD4			0.3	A

NOTES: 1. All voltages are with respect to PCB RTN node, J2 or J4.
2. Currents are positive into and negative out of the specified terminal.

3 Getting Started

3.1 Equipment Requirements

The following test equipment is required to use the ONET hot swap design kit.

- Power supply, 10 VDC at 4 amps minimum, quantity of 2
- Power supply, 6 VDC at 10 amps minimum, quantity of 2
- Oscilloscope, 4 channel preferred
- Digital voltmeter (DVM)

The availability of any additional DVMs will simplify using the kit.

3.2 Verifying the Kit Operation

The following procedure steps may be used to verify functional operation of the reference design kit after receipt.

3.2.1 Equipment Setup

CAUTION:
Under no circumstances should the shorting jumpers be installed across both headers JP9 and JP10, or both JP11 and JP12 at the same time. Doing so may cause damage to the PCB assembly or test equipment.

If installed, remove the jumper card from the main board P1 connector. Connect the supplied jumpers across headers JP1 through JP8, inclusive.

Connect the main board and test equipment as shown in Figure 6. Turn on and adjust the power supplies to the nominal voltages shown in Table 4. On each supply, verify the current limit control is set to allow sourcing of the minimum current indicated in the table.

During a power down event, the TPS2346 HSPM device sequences the loads off in a prescribed order. For each load disable, the back-end plane voltage is monitored for decay below 1 V prior to advancing to and turning off the next load (except for the negative voltage channel). Because of the large amount of capacitance on the circuit's back-end planes, this sequence can take a long time if no discharge load other than the device sense pins is provided. Consequently, the user may wish to connect discharge resistors at each voltage plane, shown as R_{LOAD} in Figure 6. Even light loads will work for this function; for example, 510Ω, 1-W resistors will suffice.

Table 4. Power Supply Setup

POWER SUPPLY	NOMINAL OUTPUT	MINIMUM CURRENT
1	5.15 V	4 A
2	5.0 V	10 A
3	3.3 V	10 A
4	–5.2 V	2 A

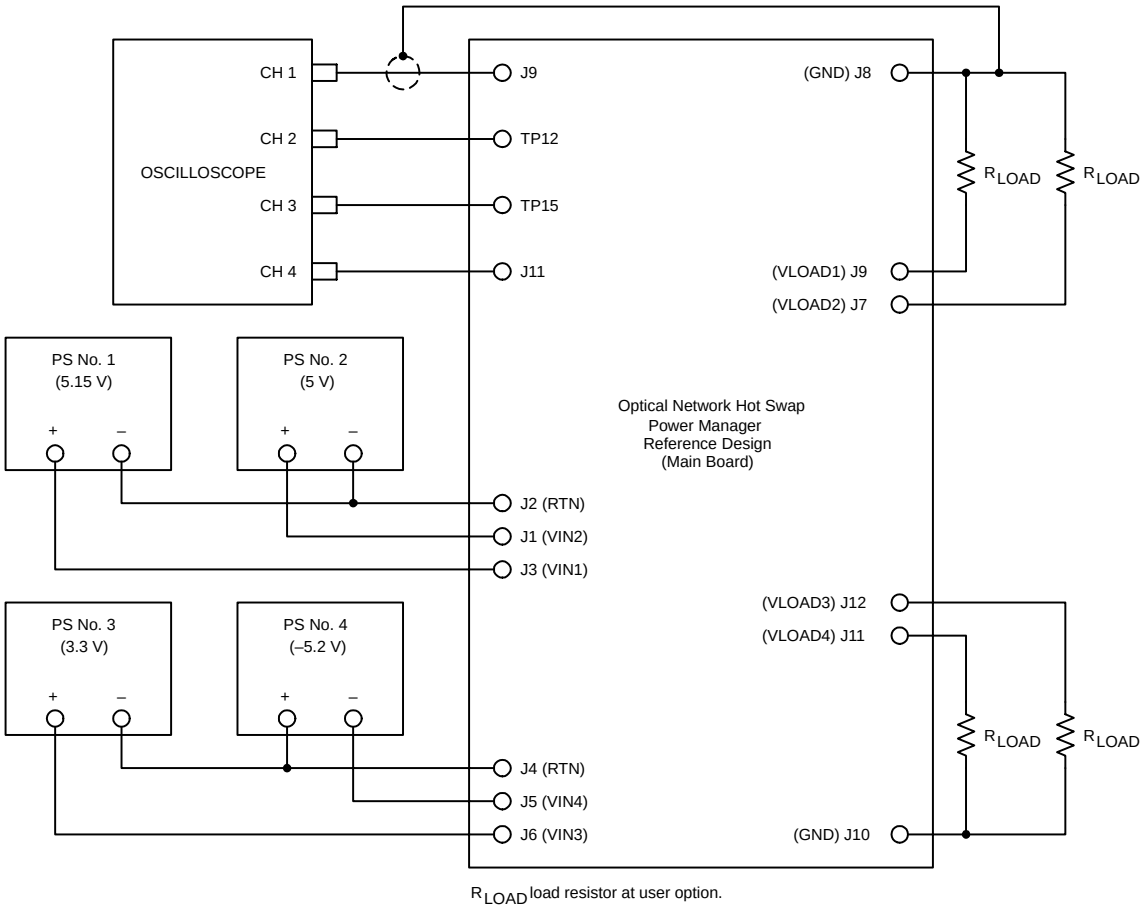

Figure 6. Optical Network Hot Swap Reference design Setup

On the main board, set the switches to the initial positions indicated in Table 5.

Table 5. Main Board Switch Initial Positions

SWITCH	REF DESIGNATOR	POSITION
BD_SEL	S1	HI
C–RAMP	S2–1	ON
	S2–2	OFF
	S2–3	OFF
PRESET_V	S3	GND
PRESET_V	S6	GND

3.2.2 Functional Test

Insert the jumper card into the P1 connector, observing the proper insertion keying. On the main board, verify the HEALTHY LED is OFF. Verify the voltage readings indicated in Table 6 are obtained at the corresponding test points. All voltages are referenced to the PCB ground at TP25 or TP26.

Table 6. Test Point Voltages –– Outputs OFF

TEST POINT	VOLTAGE READING
TP9	0 ± 10 mVDC
TP12	0 ± 10 mVDC
TP15	0 ± 10 mVDC
TP18	0 ± 10 mVDC
TP20	4.8 VDC minimum
TP24	1.0 ± 0.1 VDC

On the oscilloscope, set the channel amplifiers to the following scales:

- CH1: 2 V/div
- CH2: 2 V/div
- CH3: 2 V/div
- CH4: 2 V/div

Set the scope time base to 5 ms/div. Set the scope to trigger on the rising edge of channel 1, at about a 2-V level. Set the trigger mode to NORMAL.

On the main board, set the BD_SEL switch to the LO position. Verify that the green HEALTHY LED is illuminated. On the oscilloscope, a sweep should have been obtained similar to that shown in Figure 7. The total ramp-up time of all four back-end voltages, t_{START} in Figure 7, should be about 26 ms. To verify that all four back-end planes are powered up, a DVM can be used to verify the Table 7 voltages are present at the test points indicated. All voltages are referenced to the PCB ground at TP25 or TP26.

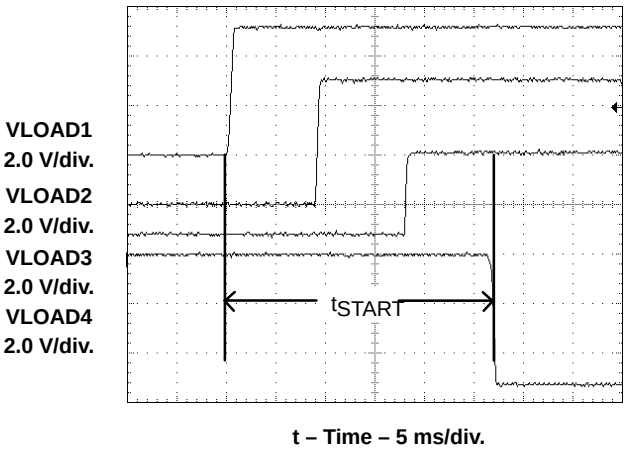

Figure 7. Load Power-Up Sequence

Table 7. Test Point Voltages –– Outputs ON

TEST POINT	VOLTAGE READING
TP9	5.15 VDC
TP12	5.0 VDC
TP15	3.3 VDC
TP18	–5.2 VDC
TP24	1.0 ± 0.1 VDC

Place the BD_SEL switch in the HI position.

Reconnect the channel 1 scope probe to test point TP19. Set the channel 1 vertical amp to 500 mV/div. Set the scope time base to 100 ms/div. Set the scope to trigger on the rising edge of channel 1 at about 500 mV, single sequence.

Verify all four back-end planes have decayed to about 0 volts. On the main board, set switches S2–2 and S2–3 to the ON position.

Place the BD_SEL switch in the LO position. After a slight delay, the HEALTHY LED should be illuminated. A scope sweep similar to the one shown in Figure 8 should be obtained.

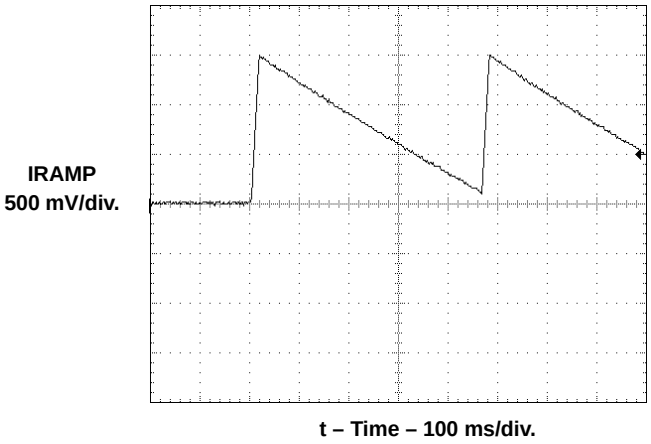

Figure 8. IRAMP Waveform Pulse

4 Using the Reference design Kit to Evaluate the TPS2346 HSPM Device

Procedures similar to the steps of Section 3.2.2 for functional test of the design kit can also be used to continue evaluation of the TPS2346 controller. Additional details about the design features are provided in this section.

4.1 Test Points

The ONET hot swap reference design contains numerous test points located throughout the circuit for waveform monitoring. A list of the test points and their associated signals is given in Table 8.

Table 8. Optical Network Hot Swap Reference design Test Points

TEST POINT	SIGNAL NAME	DESCRIPTION
TP1	VIN1	Channel 1 (5.15 V) supply input.
TP2	VIN2	Channel 2 (5 V) supply input.
TP3	VIN3	Channel 3 (3.3 V) supply input.
TP4	VIN4	Channel 4 (–5.2 V) supply input.
TP5	RTN	Supply return.
TP6	RTN	Supply return.
TP7	VIN1	Channel 1 (5.15 V) power, plug-in side.
TP8	GATE1	Gate drive for channel 1 pass FET
TP9	VLOAD1	Channel 1 load (back-end plane) voltage.
TP10	VIN2	Channel 2 (5 V) power, plug-in side.
TP11	GATE2	Gate drive for channel 2 pass FET
TP12	VLOAD2	Channel 2 load (back-end plane) voltage.
TP13	VIN3	Channel 3 (3.3 V) power, plug-in side.
TP14	GATE3	Gate drive for channel 3 pass FET
TP15	VLOAD3	Channel 3 load (back-end plane) voltage.
TP16	VIN4	Channel 4 (–5.2 V) power, plug-in side.
TP17	GATE4	Gate drive for channel 4 pass FET
TP18	VLOAD4	Channel 4 load (back-end plane) voltage.
TP19	IRAMP	TPS2346 IRAMP pin.
TP20	$\overline{\text{ENABLE}}$	Active-low enable signal.
TP21	GND	Circuit common (ground) node.
TP22	CPUMP	TPS2346 charge pump output.
TP23	$\overline{\text{PG}}$	Load power good indication.
TP24	V(P)	Test network, precharge circuit.
TP25	GND	Load common.
TP26	GND	Load common.
TP27	V(P)	Test network, precharge circuit.

4.2 Load Capacitors

Capacitors are available on-board for connection into the four switched load-side planes. These capacitors can be used to model the bulk capacitance that the target hot swap plug-in will present to the supply planes. Table 9 lists the load capacitors installed for each back-end node. The jumpers shown for each plane can be used for quick connect into or disconnect from the circuit.

Table 9. Optical Network Hot Swap Reference design Load Capacitors

BACK-END NODE	JUMPER NAME	VALUE	MIN VOLTAGE RATING
5.15 V (VLOAD1)	JP3	100 μF	16 V
	JP4	220 μF	16 V
5 V (VLOAD2)	JP1	220 μF	10 V
	JP2	470 μF	10 V
3.3 V (VLOAD3)	JP5	220 μF	10 V
	JP6	470 μF	10 V
–5.2 V (VLOAD4)	JP7	22 μF	16 V
	JP8	47 μF	16 V

To closer approximate the user's application, these capacitors can be removed from the PCB and replaced.

CAUTION:
When replacing any of the large aluminum electrolytic load caps, care should be taken to select capacitors with an appropriate voltage rating, and to observe the polarity marking on the PCB silkscreen.

4.3 Device Enable Signal

The TPS2346 $\overline{\text{ENABLE}}$ pin provides a TTL– and CMOS–compatible logic input for enabling and disabling power to the load planes. This can be used for platform control of the hardware connection process. On the main board, this signal is controlled with the BD_SEL switch, located towards the left end of the main board. One consideration in system design is the use of connector pin length staging to further control the connection process and enhance hot swap performance. The jumper card has only two levels of contact staging; however, $\overline{\text{ENABLE}}$ is on shorter contacts such that it mates only after all power and ground pins connect.

4.4 Changing the Current Limit Thresholds

During power-up of a plug-in card, the TPS2346 limits the peak current sourced to each back-end plane for charging of bulk capacitance. The LCA in each of the device's four channels (one per controlled supply) senses load current as the drop across an external sense resistor. Current is regulated by slewing the gate of the pass FET to maintain the voltage drop at a preset level. Therefore, peak current can be established by selecting the appropriate sense resistor value. As supplied from the factory, this reference design has the following sense resistor values installed, with the corresponding nominal current limits shown.

Table 10. Default Current Limit Thresholds

DEVICE CHANNEL	SUPPLY CONTROLLED	SENSE RESISTOR		CURRENT LIMIT (A)	
		REF. DESIGNATOR	VALUE (mΩ)	MIN	NOM
1	5.15 V	R1	7.5	2.1	2.7
2	5 V	R2, R12	2.5 [1]	6.4	8.0
3	3.3 V	R3, R13	2.5 [1]	6.4	8.0
4	–5.2 V	R4	200	0.375	0.75

NOTES: 1. The parallel combination of the two resistors.

To modify the current limit for any of the TPS2346 channels, the appropriate resistor can be determined from Equation 1.

$$R_{SNSx} = \frac{VMAXx}{IMAXx} \quad (1)$$

where:

- R_{SNSx} is the sense resistor value for channel x,
- VMAXx is the sense voltage limit, and
- IMAXx is the desired current limit threshold.

Using the device minimum values for VMAXx along with the required minimum current limit will ensure that minimum amount of current can always be supplied to the load. For information on the sense voltage specifications, please refer to the TPS2346 data sheet.

4.5 Changing the Inrush Slew Rate

During a turn-on sequence, the TPS2346 power manager device also controls the slew rate at which charging current is ramped to the back-end power planes. The slew rate is user-programmable as a function of sense resistor and a single capacitor connected between the IRAMP and GND pins. The design kit provides three preset capacitor values, selectable via the individual DIP switches of S2. These default values and the resultant nominal slew rates are given in Table 11.

Table 11. Optical Network Reference design Default Slew Rates

S2 DIP CLOSED	SUPPLY NAME	SLEW RATE (A/S)
1	5.15 V	11.5 k
	5 V	34.4 k
	3.3 V	34.4 k
2	5.15 V	1150
	5 V	3440
	3.3 V	3440
3	5.15 V	244
	5 V	730
	3.3 V	730

The slew rate of the three positive supplies can be changed by replacing any capacitor C1, C2 or C3 on the main board. The PCB component patterns are sized for standard 0805 ceramic chip capacitors. To configure the board for a different slew rate, the recommended procedure is to select the supply with the most stringent (slowest) requirement, and calculate a new capacitor value from Equation 2. Then, verify that the new value satisfies the requirements of the remaining supplies using Equation 3.

$$C_{RAMPx} = \frac{58}{67,500 \times R_{SNSx} \times (di/dt)_x} \quad (2)$$

where:

- C_{RAMPx} is the capacitor value (in microfarads) indicated by the channel x slew rate requirement,
- R_{SNSx} is the channel x sense resistor value, in ohms, and
- $(di/dt)_x$ is the slew rate in A/ms

Once a value, C_{RAMP}, has been selected, the slew rates of the other channels (in A/ms) can be determined by rewriting Equation 2 as Equation 3, and plugging in the appropriate numbers.

$$(di/dt)_x = \frac{58}{67,500 \times R_{SNSx} \times C_{RAMP}} \quad (3)$$

where:

- C_{RAMP} is given in microfarads.

4.6 Using the Precharge Circuitry

The ONET hot swap reference design contains two test points, TP24 and TP27, either of which can be used to observe the operation of the PRECHG output of the TPS2346. The internal precharge regulator provides a 1-V bias supply at the PRECHG pin whenever 5-V power (VIN2 input) is applied.

Test point TP24 can be used to monitor the voltage that might be seen at any of the plug-in module's I/O pins during an insertion. TP24 connects to the output (pin side) of an RC network driven by the PRECHG output. The network is intended to represent the equivalent load on PRECHG of multiple I/O lines pulled simultaneously in the same direction. The default characteristic of this load is 270 pF driven through a 2.55-kΩ resistor. The network at TP24 is charged to either V(I/O) or ground potential whenever momentary switch S4 (I/O PRESET) is depressed and held. Place switch S3 (PRESET_V) in either the VX(I/O) or GND position for a V(I/O) or ground bias value, respectively. The TPS2346 precharge circuit brings the network back to the nominal 1.0-V precharge voltage when S4 is released. This can help the user simulate bus precharge at power application, or during I/O pin contact bounce. The VX(I/O) potential can be set to either 5 V by installing a jumper across header JP9, or 3.3 V by installing jumper JP10.

CAUTION:

Do NOT install jumpers across both headers JP9 and JP10 at the same time. Doing so will short the 5-V and 3.3-V input supplies together, possibly damaging either the supplies or the PCB assembly. It is recommended to use a single jumper for both JP9 and JP10, such that it must always be removed from one header to be installed across the other.

As an alternative, test point TP27 is provided, with a separate set of component patterns, for monitoring the precharge function with the user's selection of RC network. Use 0805 resistor R9 and 0805 chip capacitor C23 for this. TP27 connects to the output (pin side) of this network. The network at TP27 is charged to either V(I/O) or ground potential whenever momentary switch S5 (I/O PRESET) is depressed and held. Place switch S6 (PRESET_V) in either the V1(I/O) or GND position for a V(I/O) or ground bias value, respectively. The TPS2346 precharge circuit brings the network back to the nominal 1.0-V precharge voltage when S5 is released. The V1(I/O) potential can be set to either 5 V by installing a jumper across header JP11, or 3.3 V by installing jumper JP12.

CAUTION:

Do NOT install jumpers across both headers JP11 and JP12 at the same time. Doing so will short the 5-V and 3.3-V input supplies together, possibly damaging either the supplies or the PCB assembly. It is recommended to use a single jumper for both JP11and JP12, such that it must always be removed from one header to be installed across the other.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265