User's Guide
SLUU183 − March 2004

10-V to 55-V Input, 3.3-V Output, 4-A, Wide Input Range Synchronous Buck Converter Using the TPS40060

System Power

Contents

1 Introduction

The TPS40060EVM evaluation module (EVM) is a high efficiency, wide input range synchronous buck converter providing a fixed 3.3-V output at 4 A from a 10-V to 55-V input. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40060 wide input range synchronous buck controller driving a P-channel high-side MOSFET.

2 Description

TPS40060EVM is a wide input range synchronous buck converter using the full input range of the TPS40060 to produce a regulated 3.3 V output at up to 4 A of load current. Using lossless $R_{DS(on)}$ current sense for short circuit protection and a high-side P-channel MOSFET simplifies the circuit design without sacrificing performance.

The evaluation module provides test points for input voltage, output voltage, key waveforms and a 50 Ω connection point in the feedback loop for non-invasive measurements of the feedback loop along with an oscilloscope jack for easy measurements of output ripple.

With the wide input range and voltage feed-forward capabilities of the TPS40060, many different sources are possible from a single converter, including 16 V, 24 V, 36 V and 42 V.

2.1 Applications

The TPS40060 has a non-isolated wide-input range from 10 V to 55 V for input systems requiring light current and low output voltage, including:

- DSP and logic Power
- General computing
- Point-of-load DC/DC conversion from unregulated or variable bus voltage

2.2 Features

- Up to 93% peak and 91% full load efficiency at 10 V input
- 10 V to 55 V input range
- 3.3 V fixed output, adjustable with single resistor
- 4 Adc output current
- 250 kHz operation
- Single main switch MOSFET and single synchronous rectifier MOSFET
- Compact size, surface mount design (2.0” x 2.2”)
- Voltage mode control
- Up to 20 kHz feedback loop bandwidth for fast transient response and high stability operation
- Double sided PCB with power stage and devices all on top side
- Convenient test points for probing critical waveforms and non-invasive loop response testing

3 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS		V_{IN}	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input voltage range				10		55	V
Maximum input current	10 V ≤ V_{IN} ≤ 55 V,	I_{OUT} = 4 A			1.5	1.8	A
No−load input current	10 V ≤ V_{IN} ≤ 55 V,	I_{OUT} = 0 A				15	mA
OUTPUT CHARACTERISTICS							
Output voltage set	10 V ≤ V_{IN} ≤ 55 V,	0A ≤ I_{OUT} ≤ 4 A		3.25	3.30	3.35	
Output voltage regulation	Line regulation, 10 V ≤ V_{IN} ≤ 55 V	I_{OUT} = 0 A,	All			1%	
	Load regulation,	V_{IN} = 32				1%	
Output voltage ripple	V_{IN} = 55,	I_{OUT} = 4 A			30		mVpp
Output load current			All				A
CONTROL LOOP CHARACTERISTICS							
Switching frequency			All	225	250	275	kHz
Control loop bandwidth				15		30	
Phase margin				60		90	°
EFFICIENCY							
Peak efficiency	V_{OUT} = 3.3 V,	2A ≤ I_{OUT} ≤ 3 A	10 V		93%		
			16 V		91%		
			24 V		89%		
			36 V		85%		
			42 V		84%		
			55 V		80%		
Full load efficiency	V_{OUT} = 3.3 V,	I_{OUT} = 4 A	10 V		91%		
			16 V		90%		
			24 V		88%		
			36 V		85%		
			42 V		84%		
			55 V		80%		

4 Schematic

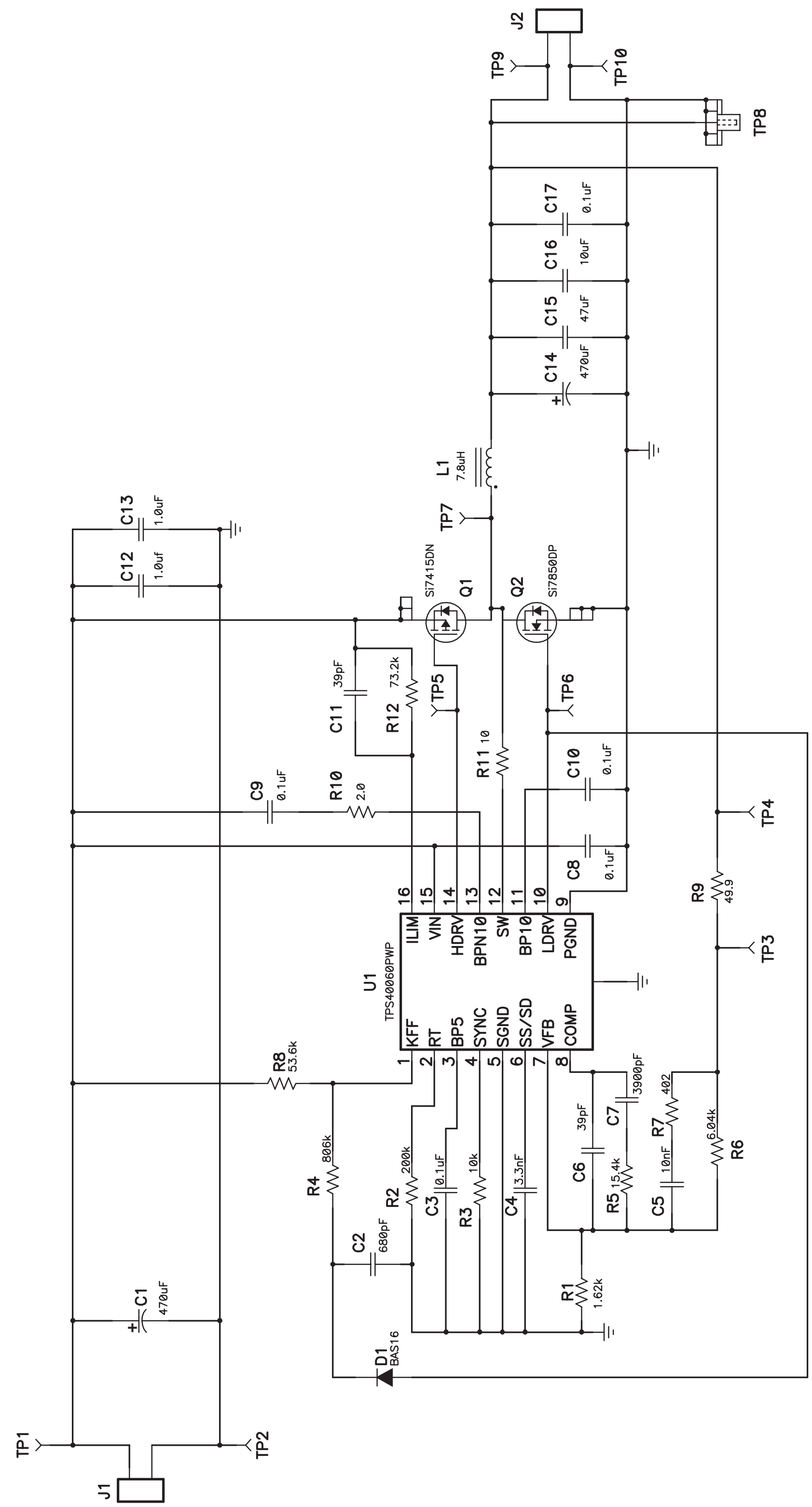

Figure 1. TPS40060EVM Schematic

5 Resistor Divider and Output Voltage

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R1). The output voltage is given by V_{REF} = 0.7 V, R6 = 6.04 kΩ and R1 by the formula in equation (1).

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R6}{R1}\right) \tag{1}$$

Table 2 contains several values for R1 to generate several different popular output voltages. TPS40060EVM is stable through these output voltages and while the efficiency is very poor at high line and full load, the module is capable of delivering a regulated output voltage at full load for each of these output voltage.

Table 1. Adjusting V_{OUT} Using R1

V_{OUT} (V)	R1 (kΩ)
3.3	1.62
2.5	2.32
2.2	2.74
2.0	3.24
1.8	3.83
1.5	5.23
1.2	8.45
0.9	21.0

6 Test Set-Up

Shown in Figure 2 is the basic test set up recommended to evaluate the TPS40060EVM. Please note that although the return for J1 is the same as the J2 return, the V_{IN} and LOAD1 connections should remain separate as shown below.

6.1 EVM Setup

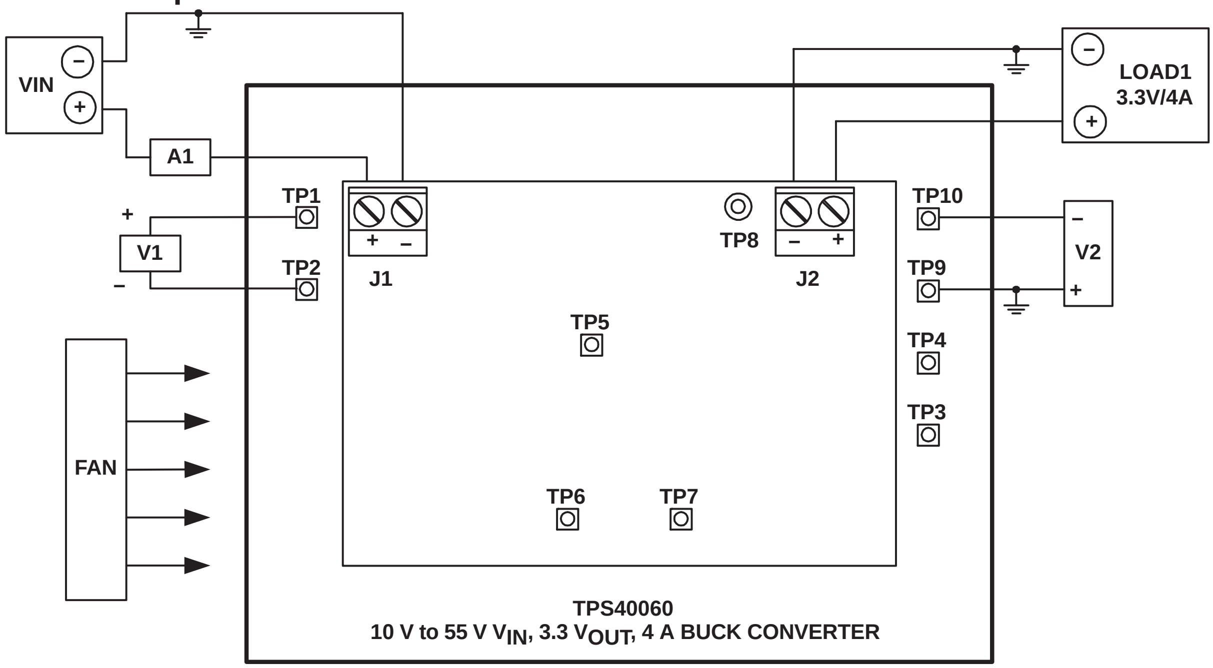

Figure 2. EVM Test Set-Up

6.2 Output Load (LOAD1)

For the output load to V_{OUT}, use a programmable electronic load set to constant current mode and capable of sinking between 0 Adc and 4Adc. Using a DC voltmeter, V2, it is also advised to make all output voltage measurements directly at TP10 and TP9 terminals. Measuring V_{OUT} at LOAD1 or J2 may result in some voltage measurement error, due to finite voltage drops across J2 and the wires between J2 and the electronic load.

6.3 DC Input Source (VIN)

The input voltage source shall be a variable DC source capable of supplying between 0 Vdc and 55 Vdc at no less than 2 Adc, and connected to J1 as shown in Figure 2. For fault protection to the EVM, good common practice is to limit the source current to no more than 2 Adc for a 10 V to 55 V input. A DC ammeter, A1 should also be inserted between VIN and J1 as shown in Figure 2 for input current measurements. A DC voltmeter, V1 should be connected to TP1 and TP2 for V_{IN} measurements.

6.4 Network Analyzer

A network analyzer can be connected directly to TP3 and TP4 shown in Figure 2. The TPS40060EVM provides a 50 Ω resistor (R9) between the output and the voltage feedback to allow easy non−invasive measurement of the control to output loop response.

6.5 Recommended Wire Gauge

For the connection between the source voltage, VIN and J5 of the EVM the minimum recommended wire size is AWG #18 with the total length of wire less than 8 feet (4 feet input, 4 feet return). For the connection between J7 of the EVM and LOAD1 the minimum recommended wire size is AWG #12, with the total length of wire less than 8 feet (4 feet output, 4 feet return). Due to the low output voltage, and the limitations of an electronic load, larger wire with shorter total length may be required.

6.6 Test Points and Oscilloscope Test Jack

TP5, TP6, TP7 and TP8 are available to allow for convenient, non-invasive probing and measuring of high speed noise sensitive signals such as gate drive voltage, switch-node voltage and output voltage ripple without modification of the EVM design board

6.7 Fan

Most power converters include components that can get hot to the touch approaching temperatures of 60°C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of between 200 and 400 LFM is recommended to reduce component temperatures during operation.

7 Power Up/Down Test Procedure

The following test procedure is recommended primarily for power up and shutting down the EVM. Whenever the EVM is running the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 2-A maximum. Connect the ammeter A1 (0 Ato 2 A range) between V_{IN} and J1 as shown in Figure 2. Make sure V_{IN} is initially set to 0 V.
3. Connect LOAD1 to J2 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 Adc before V_{IN} is applied.
4. Connect the voltmeter, V2 to TP9 and TP10 as shown in Figure 2.
5. Increase V_{IN} from 0 V to 10 Vdc, while monitoring the output voltage on V2. V_{OUT} should be in regulation when V_{IN} > 10 V.
6. Turn on fan blowing air directly on the EVM
7. Vary LOAD1 anywhere between 0 A to 4 Adc.
8. Vary the input voltage between 10 V and 55 V.
9. Set LOAD1 to 0 A.
10. Set V_{IN} to 0 Vdc.
11. Shut down the electronic load.
12. Shut down V_{IN}.

8 Performance Data and Characteristic Curves

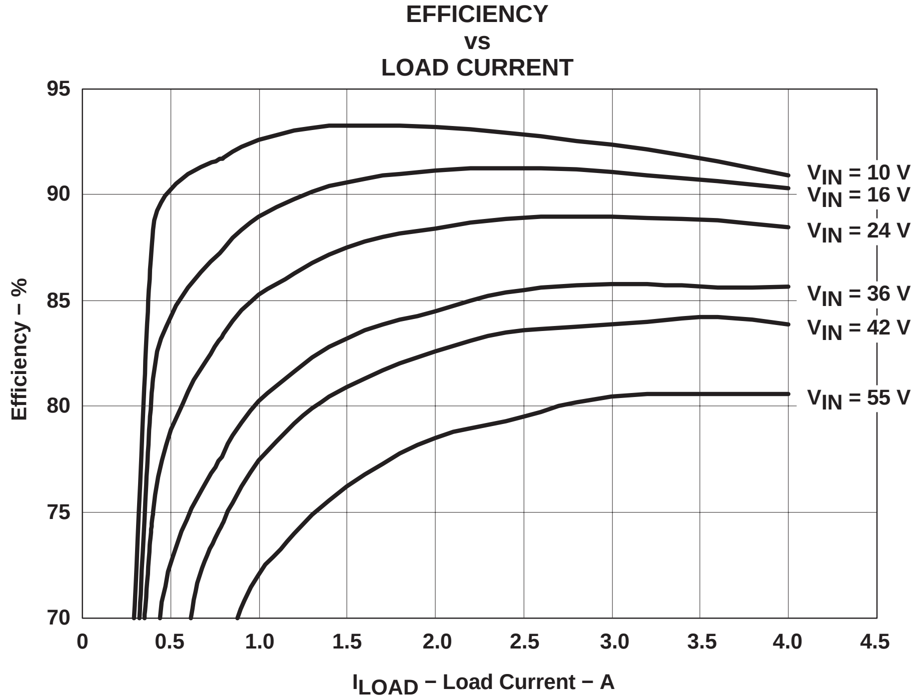

Figure 3.

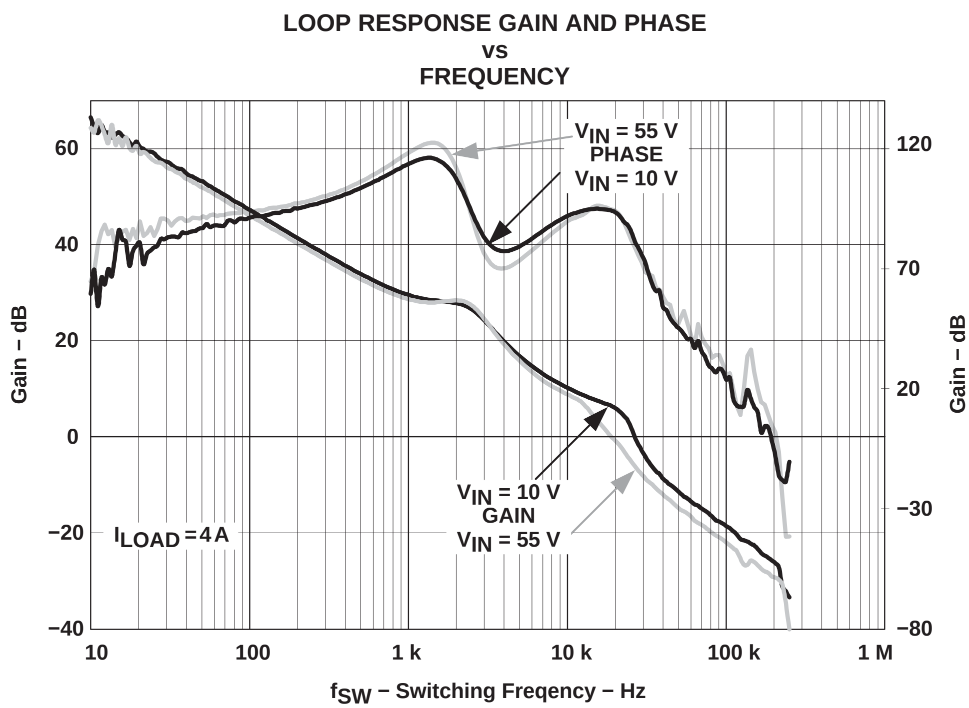

Figure 4.

9 EVM Assembly Drawing and PCB Layout

Figure 5 through 8 show the design of the TPS40060EVM printed circuit board. The EVM has been designed using an inexpensive two-sided, copper-clad circuit board 3.0” x 3.5” with all components and routing confined to a 2.0” x 2.2” area to allow the circuit design to be incorporated into almost any PCB design without needing to add additional internal layers, or as an external module.

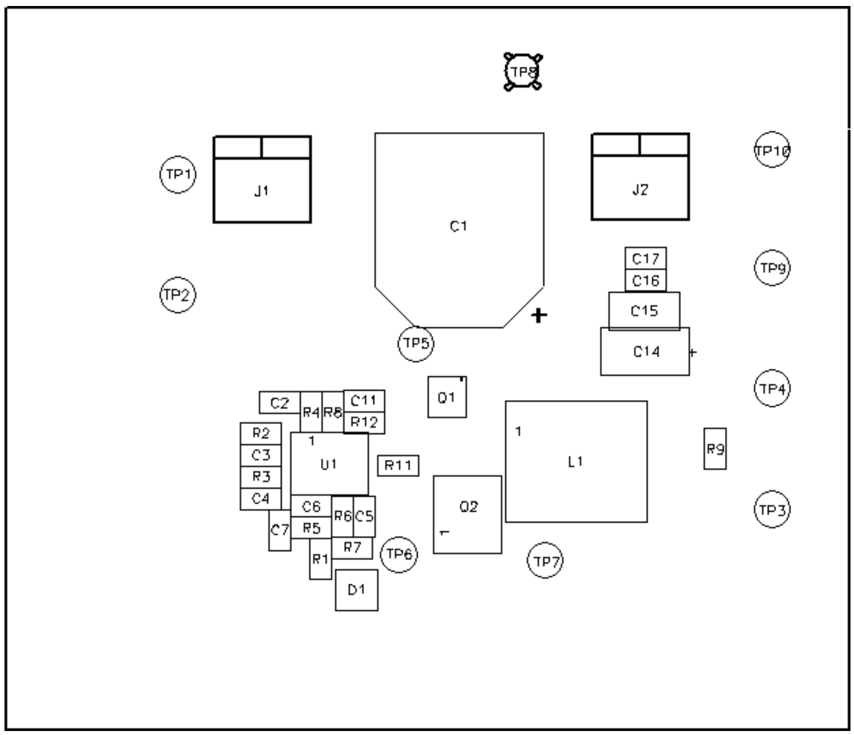

Figure 5. Top Side Component Assembly

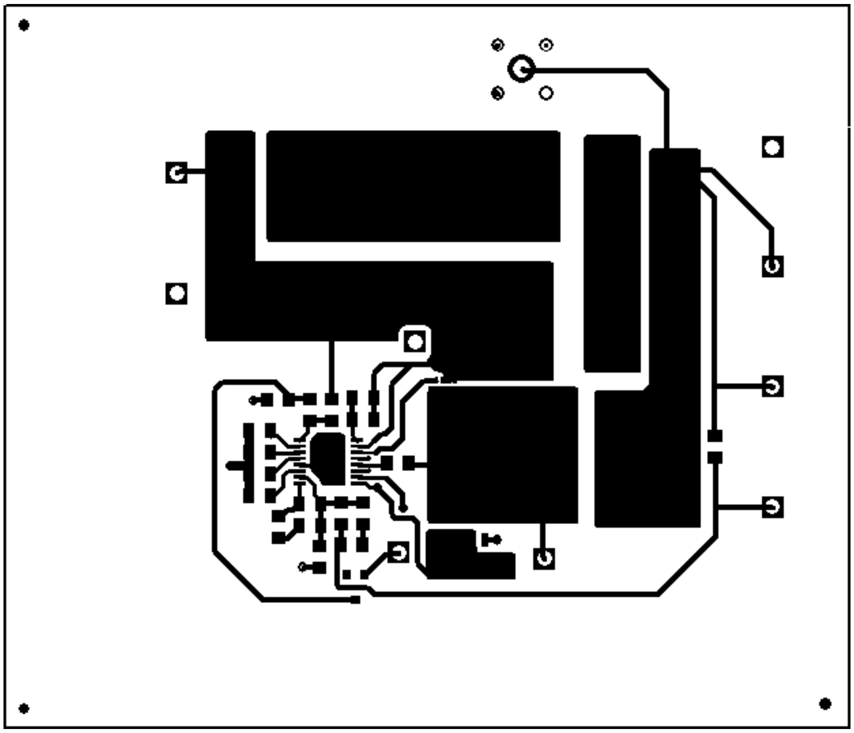

Figure 6. Top Side Copper Trace

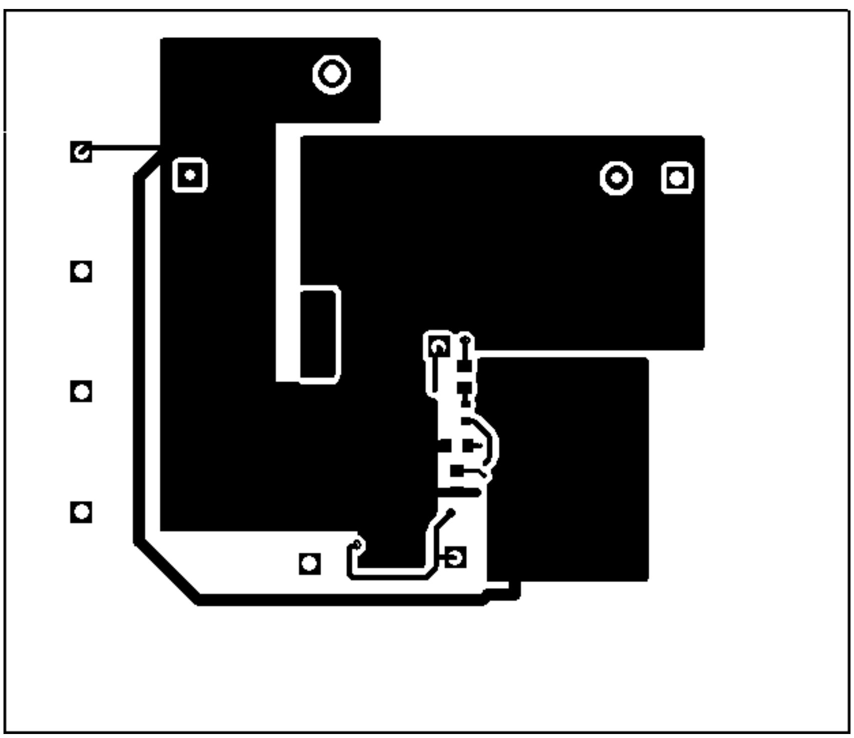

Figure 7. Bottom Side Copper Trace

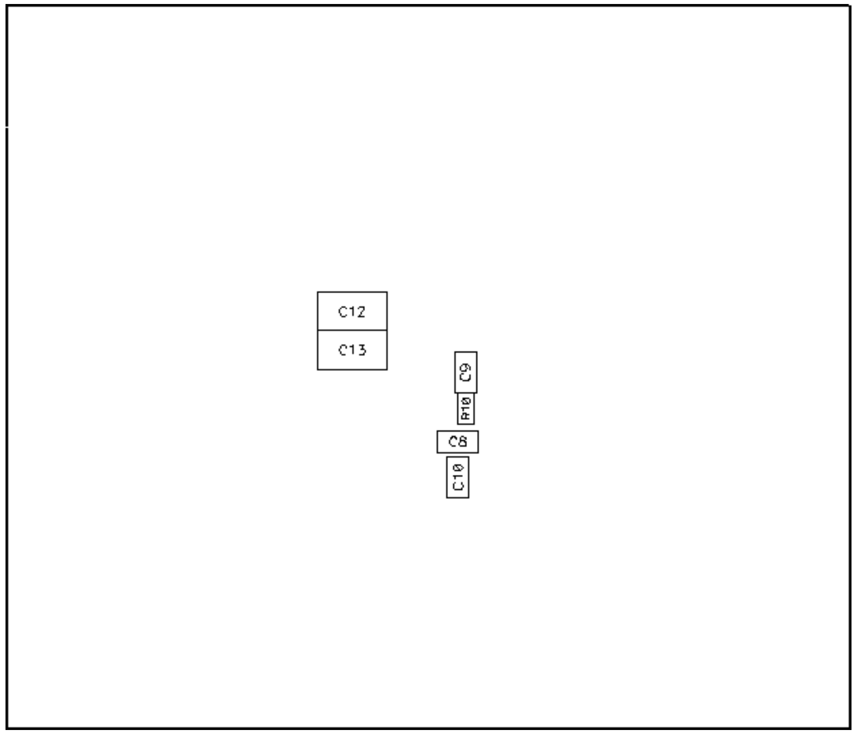

Figure 8. Bottom Side Component Assembly

10 List of Materials

Table 2 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 2. TPS40060EVM (HPA057A) List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
C1	1	Capacitor, aluminum, SM 470 µF, 63 V	0.67 x 0.75	Panasonic	EEVFK1J471M
C2	1	Capacitor, ceramic, 680 pF, 50 V, X7R, 20%	805	std	std
C3, C10, C17	3	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 20%	805	std	std
C4	1	Capacitor, ceramic, 3.3 nF, 50 V, X7R, 20%	805	std	std
C5	1	Capacitor, ceramic, 10 nF, 50 V, X7R, 20%	805	std	std
C6,C11	2	Capacitor, ceramic, 39 pF, 50 V, X7R, 20%	805	std	std
C7	1	Capacitor, ceramic, 3900 pF, 50 V, X7R, 20%	805	std	std
C8, C9	2	Capacitor, ceramic, 0.1 µF, 100 V, X7R, 20%	805	std	std
C12, C13	2	Capacitor, ceramic, 1.0 µF, 100 V, X7R, 20%	1812	TDK	C4532X7R2A105M
C14	1	Capacitor, POSCAP, 470 µF, 6.3 V, 35 mΩ, 20%	D4	Sanyo	6TPB470M
C15	1	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 20%	1812	TDK	C4532X5R0J476M
C16	1	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%	805	TDK	C2012X5R0J106M
D1	1	Diode, switching, 10 mA, 85 V, 350 mW	SOT23	Vishay−Liteon	BAS16
J1, J2	2	Terminal block, 2-pin, 15 A, 5.1 mm	0.40 x 0.35	OST	ED1609
L1	1	Inductor, SMT, 7.8 µH, 8.2 A, 10.2 mΩ	0.325 x 0.318	TDK	RLF12560−7R8N8R2
Q1	1	MOSFET, P−channel, −60 V, 5.7 A, 0.065 mΩ	1212−8 single		Si7415DN
Q2	1	MOSFET, N−channel, 60 V, 10.3 A, 0.022 mΩ	PWRPAK SO−8		Si7850DP
R1	1	Resistor, chip, 1.62 kΩ, 1/10−W, 1%	805	Std	Std
R2	1	Resistor, chip, 200 kΩ, 1/10−W, 1%	805	Std	Std
R3	1	Resistor, chip, 10 kΩ, 1/10−W, 1%	805	Std	Std
R4	1	Resistor, chip, 806 kΩ, 1/10−W, 1%	805	Std	Std
R5	1	Resistor, chip, 15.4 kΩ, 1/10−W, 1%	805	Std	Std
R6	1	Resistor, chip, 6.04 kΩ, 1/10−W, 1%	805	Std	Std
R7	1	Resistor, chip, 402 Ω, 1/10−W, 1%	805	Std	Std
R8	1	Resistor, chip, 53.6 kΩ, 1/10−W, 1%	805	Std	Std
R9	1	Resistor, chip, 49.9 Ω, 1/10−W, 1%	805	Std	Std
R10	1	Resistor, chip, 2.0 Ω, 1/16−W, 5%	603	Std	Std
R11	1	Resistor, chip, 10 Ω, 1/10−W, 1%	805	Std	Std
R12	1	Resistor, chip, 73.2 kΩ, 1/10−W, 1%	805	Std	Std
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP9, TP10	5	Test point, 0.050 hole,	0.050”	MILL−MAX	3103−1−00−15−00−00−0X−0
TP8	4	Adaptor, 3.5 mm probe clip (or 131−5031−00)	0.2	Tektronix	131−4244−00
U1	1	Wide input synchronous buck controller	PWP16	TI	TPS40060PWP
−−	1	PCB, 4-Layer FR4, 2.4” x 2.1” x 0.062”	2.4” x 2.1”	Any	HPA057A
−−	1	Bumpon, transparent	0.44” x 0.2”	3M	SJ5303

(1) Should not be substituted.

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