User's Guide
SLUU412–March 2010

CSD163CEVM-591

The CSD163CEVM-591 evaluation module (EVM) is a synchronous buck converter providing a fixed 1.2V output at up to 25A from a 12-V input bus. The EVM is designed to start-up from a single supply; so, no additional bias voltage is required for start-up. The module uses the TPS40304 high performance, mid-input voltage synchronous buck controller and TI's DualCool™ NexFET™ high performance MOSFETs

TI's DualCool™ NexFET™ family of power MOSFETs delivers an industry standard footprint, while enabling thermally efficient cooling through the top and bottom of the package. This package allows power system designers to effectively direct heat away from the PCB in high-current DC/DC applications, resulting in improved power density, higher current capability and improved system reliability.

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1 Description

CSD163CEVM-591 is designed to use a regulated 12V (8V – 14V) bus voltage to provide a regulated 1.2-V output at up to 25A of load current. CSD163CEVM-591 is designed to demonstrate the TPS40304 controller and TI DualCool™ NexFETs™ in a typical 12-V bus to low-voltage application while providing a number of non-invasive test points to evaluate the performance of the system.

In addition, a heatsink and thermal interface pad are provided to take advantage of the topside cooling capability of the DualCool packaging. By installing the provided heatsink and adding 100-200lfm airflow, the system is capable of delivering 25A continuous. Without this heatsink, evaluation module is only capable of 20A. See the performance curves in Section 6 of this document

Note, the topside thermal tab of the DualCool™ devices are electrically live and connected to the MOSFET source pin. As such, a thermal interface pad with electrical isolation must be used before mounting a metal heatsink. See Section 5.1.6 for further details on thermal interface pad requirements.

1.1 Applications

- High-current, low-voltage FPGA or microcontroller core supplies
- High-current point of load modules
- Telecommunications equipment
- Computer peripherals

1.2 Features

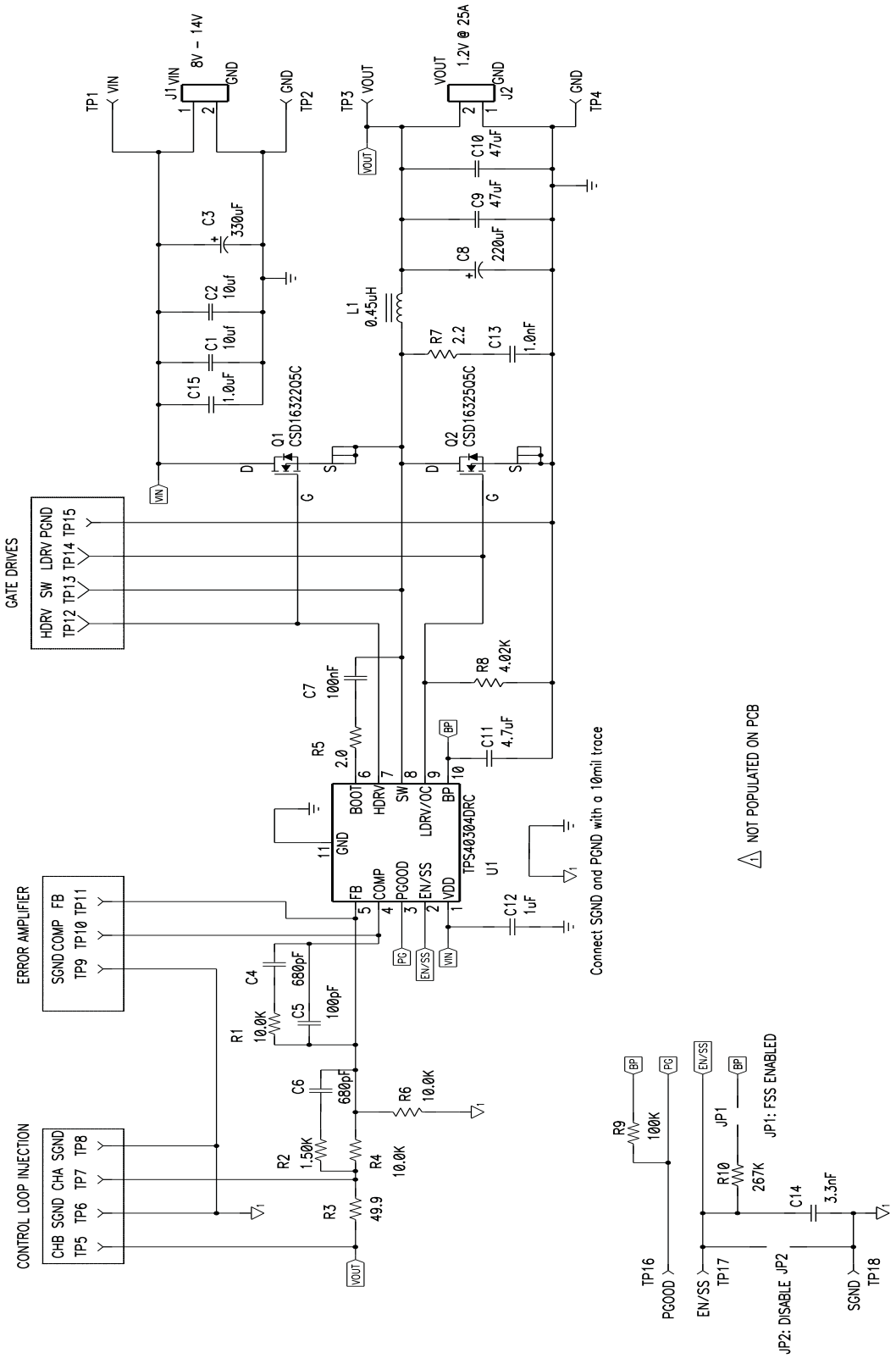
- 8-V to 14-V input voltage rating
- 1.2-V ± 2% output voltage rating
- 25-A steady state load current
- 600-kHz switching frequency
- Simple access to IC features including Power Good, Enable, Soft-Start and Error Amplifier
- Convenient test points for simple, non-invasive measurements of converter performance

2 CSD163CEVM-591 Electrical Performance Specifications

Table 1. CSD163CEVM-591 Electrical and Performance Specifications

Parameter		Notes and Conditions	Min	Typ	Max	Unit
Inputs Characteristics						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = Nom, I_{OUT} = Max	–	3	3.3	A
	No load input current	V_{IN} = Nom, I_{OUT} = 0A	–	40	50	mA
V_{IN_UVLO}	Input UVLO	I_{OUT} = 10A		3		V
Outputs Characteristics						
V_{OUT1}	Output voltage 1	V_{IN} = 12V, I_{OUT} = 20A	1.17	1.2	1.23	V
	Line regulation	V_{IN} = 8V to 14V	–	–	0.5%	
	Load regulation	I_{OUT} = 0A to 20A	–	–	0.5%	
V_{OUT_ripple}	Output voltage ripple	V_{IN} = 12V, I_{OUT} = 20A	–	–	24	mVpp
I_{OUT1}	Output current 1	V_{IN} = 8V to 14V	0		25	A
Systems Characteristics						
F_{SW}	Switching frequency		540	600	660	kHz
ηpk	Peak efficiency	V_{IN} = 12V, Heatsink installed	–	88%	–	
η	Full load efficiency	V_{IN} = 12V, I_{OUT} = 25A, Heatsink installed	–	85%	–	

3 CSD163CEVM-591 Schematic



For reference only, See Section 8 for specific values

Figure 1. CSD163CEVM-591 Schematic

4 Connector and Test Point Descriptions

4.1 Enable Jumper (JP2)

CSD163CEVM-591 is designed with a Disable Jumper (JP2) using a 0.1" spacing header and shunt. Installing a shunt in the JP2 position connects the EN/SS pin to GND, discharge the soft-start capacitor and disable the TPS40304 controller. This forces the output into a high-impedance stage (Approximately 20kΩ to GND)

4.2 Frequency Spread Spectrum – FSS Jumper (JP1)

CSD163CEVM-591 is designed with a FSS Enable Jumper (JP1) using a 0.1" spacing header and shunt. Installing a shunt in the JP1 position connects the EN/SS pin to BP via a 267kΩ resistor (R10) to enable Frequency Spread Spectrum

Frequency Spread Spectrum modulates the switching frequency to ±10% of the nominal value at 30kHz to reduce EMI at the switching frequency and its harmonics; however, there may be a 30kHz component to the output ripple (See Figure 10)

CSD163CEVM-591 does not dynamically monitor the JP1 status for programming FSS. CSD163CEVM-591 must be disabled via JP2 or powered down by reducing VIN to less than 3.0V to remove or install JP1.

4.3 Test Point Descriptions

Table 2. Test Point Description

Test Point	Label	Use	Section
TP1	VIN	Measurement test point for input voltage	Section 4.3.1
TP2	GND	Ground test point for input voltage	Section 4.3.1
TP3	VOUT	Measurement test point for output voltage	Section 4.3.1
TP4	GND	Ground test point for output voltage	Section 4.3.2
TP5	CHB	Measurement test point for channel B of loop response	Section 4.3.3
TP6	SGND	Ground test point for channel B of loop response	Section 4.3.3
TP7	CHA	Measurement test point for channel A of loop response	Section 4.3.3
TP8	SGND	Ground test point for channel A of loop response	Section 4.3.3
TP9	SGND	Ground test point for error amplifier measurements	Section 4.3.4
TP10	COMP	Measurement test point for error amplifier output voltage	Section 4.3.4
TP11	FB	Measurement test point for error amplifier input voltage	Section 4.3.4
TP12	HDRV	Measurement test point for high-side gate driver voltage	Section 4.3.5
TP13	SW	Measurement test point for switch node voltage	Section 4.3.5
TP14	LDRV	Measurement test point for low-side gate driver voltage	Section 4.3.5
TP15	PGND	Ground test point for switch node and gate drive voltages	Section 4.3.5
TP16	PGOOD	Measurement test point for power good	Section 4.3.6
TP17	EN/SS	Measurement test point for enable / soft-start	Section 4.3.7
TP18	SGND	Ground test point for power good and enable / soft-start	Section 4.3.6 and Section 4.3.7

4.3.1 Input Voltage Monitoring (TP1 and TP2)

CSD163CEVM-591 provides two test points for measuring the input voltage applied to the module. This allows the user to measure the actual input module voltage without losses from input cables and connectors. All input voltage measurements should be made between TP1 and TP2. To use TP1 and TP2, connect a voltmeter positive input to TP1 and input terminal to TP2.

4.3.2 Output Voltage Monitoring (TP3 and TP4)

CSD163CEVM-591 provides two test points for measuring the output voltage generated by the module. This allows the user to measure the actual module output voltage without losses from input cables and connectors. All input voltage measurements should be made between TP3 and TP4. To use TP3 and TP4, connect a voltmeter positive input to TP3 and negative input to TP4.

4.3.3 Loop Response Testing (TP5, TP6, TP7, TP8, and R3)

CSD163CEVM-591 provides four test points (2 Signal and 2 Ground) for measuring the control loop frequency response. This allows the user to measure the actual module loop response without modifying the evaluation board. A transformer isolated signal upto 30mV can be injected between TP5 and TP7. The injected signal amplitude can be measured by the AC coupled amplitude at CHA (TP7) and the resulting output voltage deviation can be measured at CHB (TP5). See Figure 4 for additional detail.

4.3.4 Error Amplifier Voltage Monitoring (TP9, TP10, and TP11)

CSD163CEVM-591 provides three test points for measuring the error amplifier input and output voltages. This allows the user to directly measure the feedback and control voltages of the TPS40304 controller. The control voltage (TP10) can also be used to measure the Control to Output or Power Stage frequency response or Output to Control or Error Amplifier frequency response. See Section 5.5 for additional details.

4.3.5 Switching Waveform Monitoring (TP12, TP13, TP14, and TP15)

CSD163CEVM-591 provides three test points and a local power ground for measuring the switching waveforms of the module's power stage. This allows the user to monitor actual switching waveforms during operation. TP13 is a 0.040" square pad of exposed PCB copper to minimize EMI radiation from the high transient voltages on the switch node. Switching waveform measurements should be made using Power Ground (TP15) as the ground reference for more accurate measurements.

4.3.6 Power Good Voltage Monitoring (TP16 and TP18)

CSD163CEVM-591 provides a test point and local ground for measuring the power good output voltage. A 100kΩ resistor pull-up to BP (R9) is included to allow the Power Good signal to be monitored without requiring an external pull-up. For true open-drain operation with no pull-up, remove R9. With R9 removed TP16 can be connected to TP17 of another CSD163CEVM-591 to provide sequential start-up of the two CSD163CEVM-591 converters.

4.3.7 Enable and Soft-Start Voltage Monitoring (TP17 and TP18)

CSD163CEVM-591 provides a test point and local ground for measuring the Enable and Soft-Start voltage. TP17 and TP18 or JP2 can be used to provide an external enable signal. Due to the nature of the Soft-Start function, the external signal must be open-collector or open-drain without pull-up.

5 Test Set Up

5.1 Equipment

5.1.1 Voltage Source

V_{IN} — The input voltage source (V_{IN}) shall be a 0V – 15V variable dc source capable of supplying 5Adc

5.1.2 Meters

A1: — Input current meter. 0Adc – 5Adc ammeter

V1: — Input voltage meter. 0V – 15V voltmeter

V2: — Output voltage meter. 0V – 2V voltmeter

5.1.3 Loads

LOAD1: — Output load. Electronic load set for constant current or constant resistance capable of 0Adc – 25Adc at 1.2Vdc

5.1.4 Oscilloscope

For Output Voltage Ripple: — Oscilloscope shall be an analog or digital oscilloscope set for ac coupled measurement with 20-MHz bandwidth limiting. Use 20mV / division vertical resolution, 1µs/division horizontal resolution.

For Switching Waveforms: — Oscilloscope shall be an analog or digital oscilloscope set for dc coupled measurement with 20-MHz bandwidth limiting. Use 2V/division or 5V/division vertical resolution and 1µs/division horizontal resolution.

5.1.5 Recommended Wire Gauge

VIN to J1: — The connection between the source voltage (VIN) and J1 of CSD163CEVM-591 can carry as much as 3.5Adc of current. The minimum recommended wire size is AWG #16 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

J2 to LOAD1: — The connection between the source voltage (VIN) and J1 of CSD163CEVM-591 can carry as much as 25Adc of current. The minimum recommended wire size is AWG #12 with the total length of wire less than 2 feet (1 foot input, 1 foot return).

5.1.6 Thermal

FAN
The CSD163CEVM-591 Evaluation Module includes components that can get hot to the touch when operating. Because this evaluation module is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400lfm is recommended to reduce component temperatures when operating.

Heatsink
A pinfin heatsink from CoolInnovations (#3-050505U) is supplied with this EVM. It has a Thermal Resistance of 11.23ºC/W when 200LFM of air is supplied and reduces to 8.3ºC/W when the airflow is increased to 400LFM.

Thermal Interface Pad
A thermally conductive interface pad from Bergquist (Gap Pad® 1500) is supplied with this EVM. The Gap Pad material provides thermal coupling between the exposed tops of the DualCool™ devices and the provided heatsink. Also, the Gap Pad material provides electrical isolation of up to 6000V and has a thermal conductivity of 1.5 W/m-K

Temperature Measurements
Temperature measurements are best measured with an infrared camera. Alternatively, a thermometer with a J or K type thermal couple may be used. Special care must be taken on the selection of the thermal couple wire size. Use 32AWG or smaller to minimize the error caused the heatsinking effects of the thermal couple bead.

NOTE: To normalize the emmistive of the PCB prior to taking thermal images, it is important to coat the PCB in a thin film of material offering a uniform emmisivity, such as black spray paint, then calibrate the camera by comparing the camera's thermograph to a known reference temperature. This can be accomplished by placing a thermal couple on the heat-sink, then using the thermograph of the heatsink to compare to the thermal couple measurement.

5.2 Equipment Setup

Shown in Figure 2 is the basic test set up recommended to evaluate the CSD163CEVM-591. Note that although the return for J1 and JP2 are the same system ground, the connections should remain separate as shown in Figure 2.

5.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 4A maximum. Make sure V_{IN} is initially set to 0V and connected as shown in Figure 2.
3. Connect VIN to J1 as shown in Figure 2.
4. Connect ammeter A1 between VIN and J1 as shown in Figure 2.
5. Connect voltmeter V1 to TP1 and TP2 as shown in Figure 2.
6. Connect voltmeter V2 to TP3 and TP4 as shown in Figure 2.
7. Connect oscilloscope probes to desired test points per Table 2.
8. Place fan as shown in Figure 2 and turn on making sure to blow air directly across the evaluation module.

5.2.2 Diagram

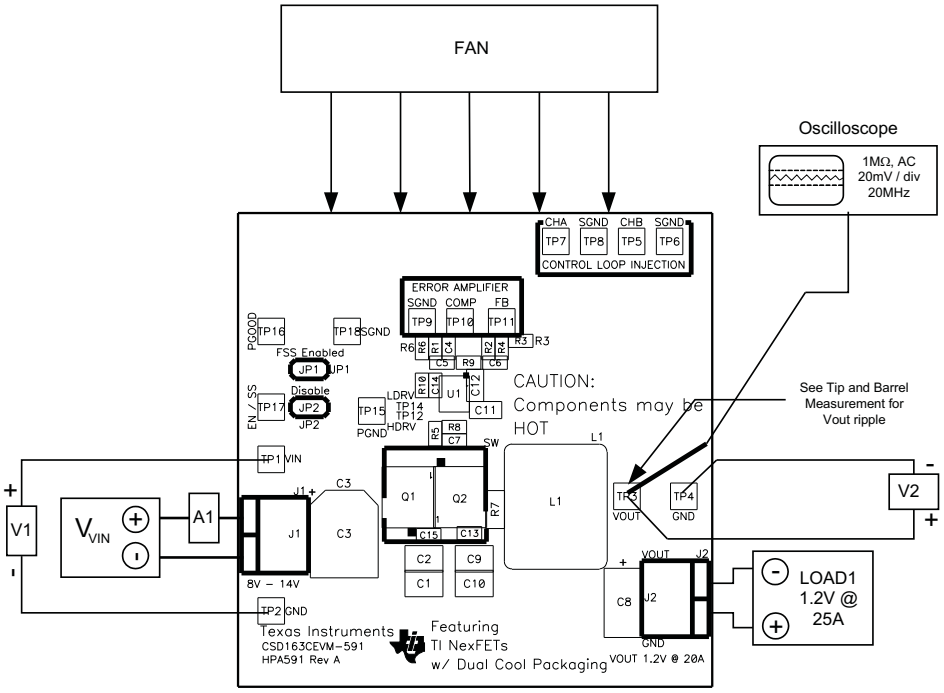


Figure 2. CSD163CEVM-591 Recommended Test Set-Up

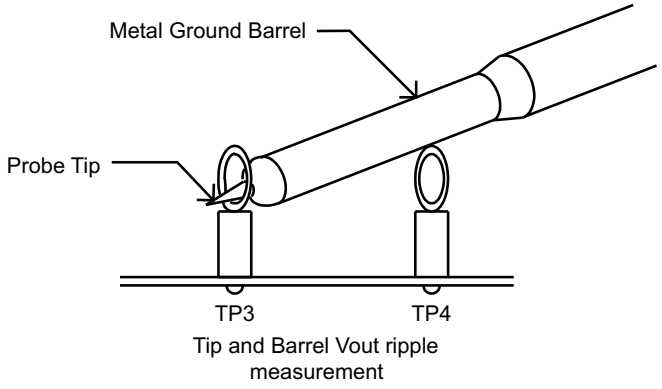


Figure 3. Output Ripple Measurement – Tip and Barrel using TP3 and TP4

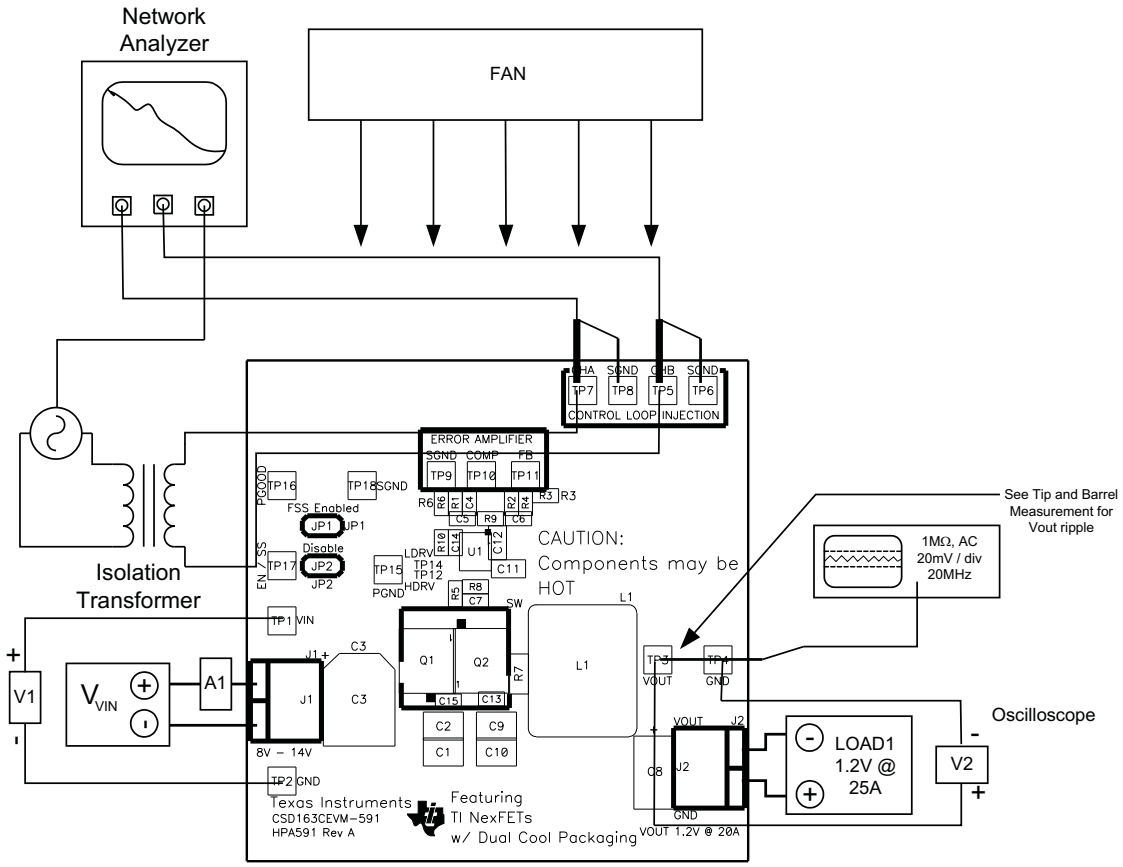


Figure 4. Control Loop Measurement Setup

5.3 Heatsink Installation

Clean the underside of the heatsink to ensure it is free from debris for this will degrade the thermal performance of the heatsink. Remove one of the backing tapes from the included Gap Pad and attach to the heatsink. Firmly press down to make sure there is uniform contact to the surface of the heatsink. Remove the second backing tape of the Gap Pad material and attach the heatsink to the topside of the DualCool devices in the area marked around Q1 and Q2. Firmly press down while aligning the heatsink over the designated area on the PCB. Make sure to keep the heatsink edge clear of the ceramic capacitors (C2 and C9).

5.4 Start Up/Shut Down Procedure

1. Verify shunt position for JP1 for desired FSS status per Section 4.2
2. Remove shunt from JP2 location if present
3. Increase VIN from 0Vdc to 12Vdc
4. Vary LOAD1 from 0Adc to 25Adc
5. Vary VIN from 8V to 14V
6. Decrease VIN to 0V
7. Decrease LOAD1 to 0A

5.5 Output Ripple Voltage Measurement Procedure

1. Follow Section 5.4 Start-Up / Shut-Down Procedure steps 1 – 5 to set VIN and LOAD1 to the desired operating condition
2. Connect oscilloscope probe with exposed metal barrel to TP3 and TP4 per Figure 3
3. Set oscilloscope per oscilloscope for output voltage ripple measurement in Section 5.1.4
4. Follow Section 5.4 Start-Up / Shut-Down Procedure steps 6 and 7 to power down

5.6 Control Loop Gain and Phase Measurement Procedure

1. Follow Section 5.4 Start-Up / Shut-Down Procedure steps 1 – 5 to set VIN and LOAD1 to desired operating condition
   (a) If JP1 is installed (FSS enabled), loop response data about the modulation frequency (30kHz) may be affected
2. Connect a 1-kHz – 1-MHz isolation transformer to TP5 and TP7 as shown in Figure 4
3. Connect input signal amplitude measurement probe (channel A) to TP7 as shown in Figure 4
4. Connect output signal amplitude measurement probe (channel B) to TP5 as shown in Figure 4
5. Connect ground lead of channel A and channel B to TP6 and TP8 as shown in Figure 4
6. Inject 30mV or less signal across R3 through isolation transformer
7. Sweep frequency from 1kHz to 1MHz with 10Hz or lower post filter
8. Control loop gain can be measured by: $20 \times \mathrm{LOG}\left(\frac{\text{Channel B}}{\text{Channel A}}\right)$
9. Control loop phase can be measured by the phase difference between channel A and channel B
10. Control to output response (power stage transfer function) can be measured by connecting channel A probe to TP10 (COMP) and channel B probe to TP5 (CHB)
11. Output to control response (compensated error amplifier transfer function) can be measured by connecting channel A probe to TP7 (CHA) and channel B probe to TP10 (COMP)
12. Follow Section 5.4 Start-Up / Shut-Down Procedure steps 6 and 7 to power down

5.7 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down LOAD1
3. Shut down VIN
4. Shut down fan

6 CSD163CEVM-591 Test Data

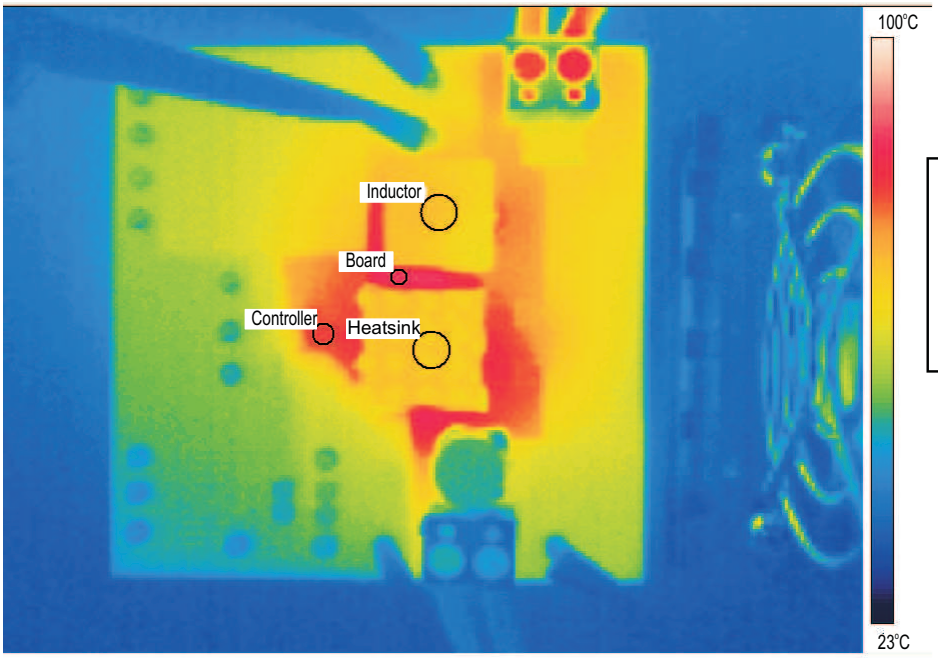
Figure 5 through Figure 13 present typical performance curves for the CSD163CEVM-591. Since actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and may differ from actual field measurements.

6.1 Efficiency

With and without a heatsink at V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 0A – 25A

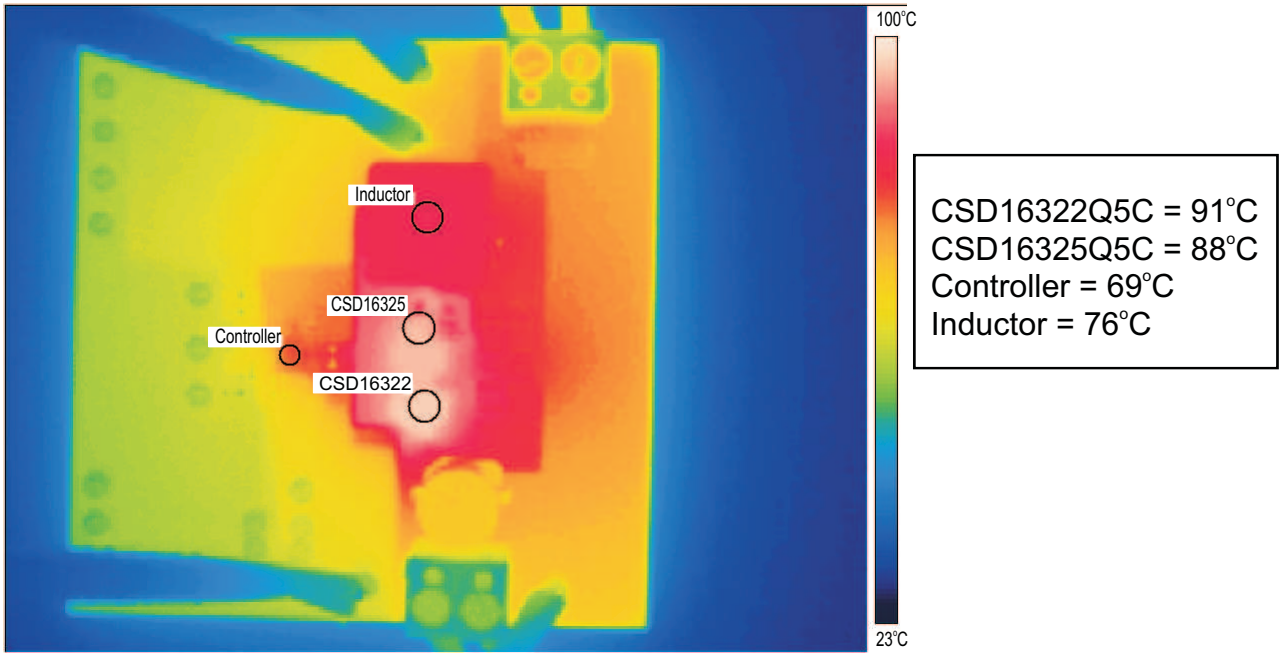
Figure 5. CSD163CEVM-591 Efficiency vs Load Current

6.2 Thermal Image (Emissivity Balanced See Section 5.1.6)



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A

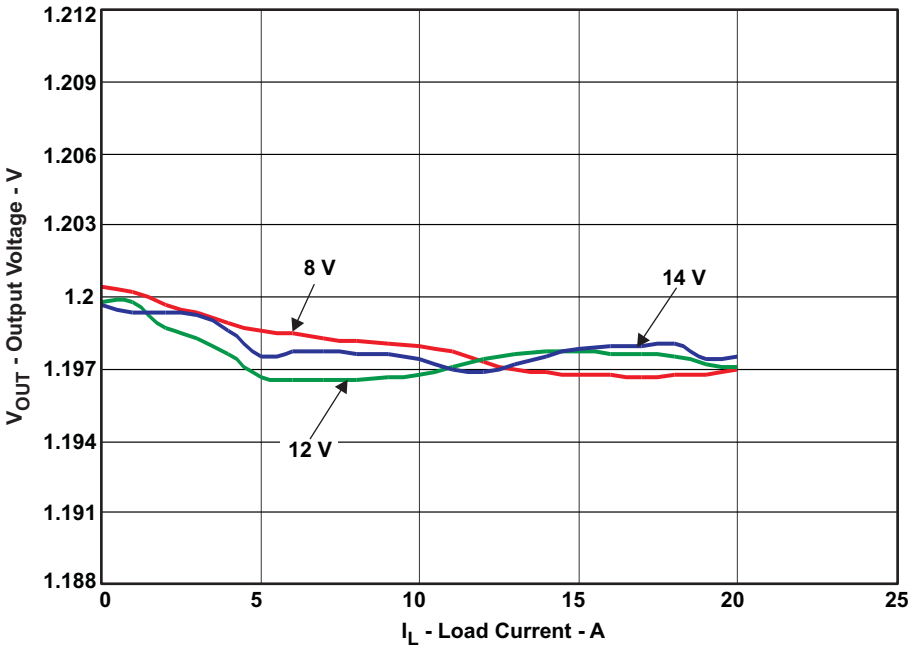
Figure 6. CSD163CEVM-591 Thermal Graph with Heatsink + 200LFM



V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 20A

Figure 7. CSD163CEVM-591 Thermal Graph without Heatsink or Airflow

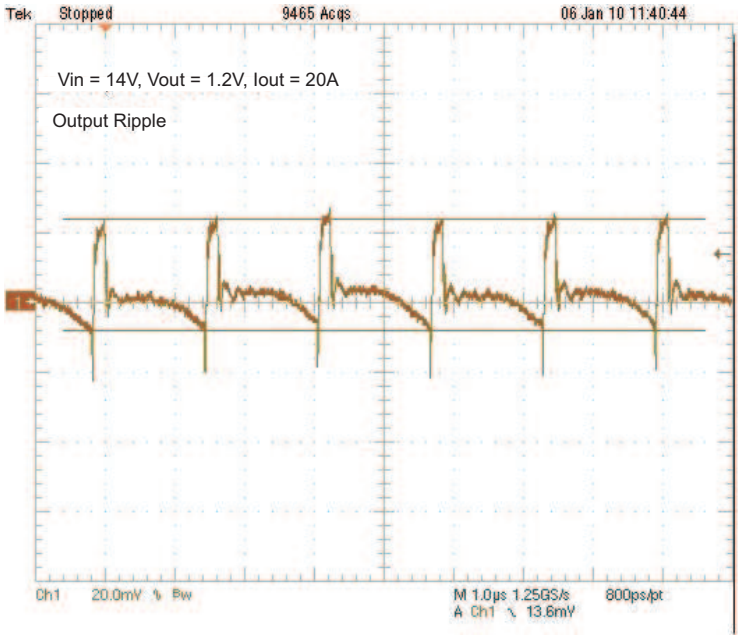
6.3 Line and Load Regulation



V_{IN} = 8V – 14V, V_{OUT} = 1.2V, I_{OUT} = 0A – 20A

Figure 8. CSD163CEVM-591 Output Voltage vs Load Current

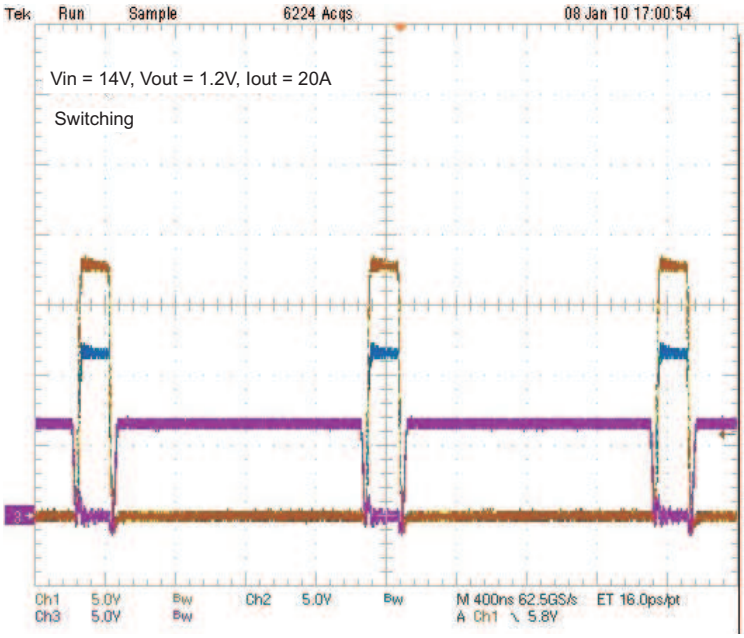
6.4 Output Voltage Ripple



V_{IN} = 14V, V_{OUT} = 1.2V, I_{OUT} = 20A

Figure 9. CSD163CEVM-591 Output Voltage Ripple

6.5 Switch Node

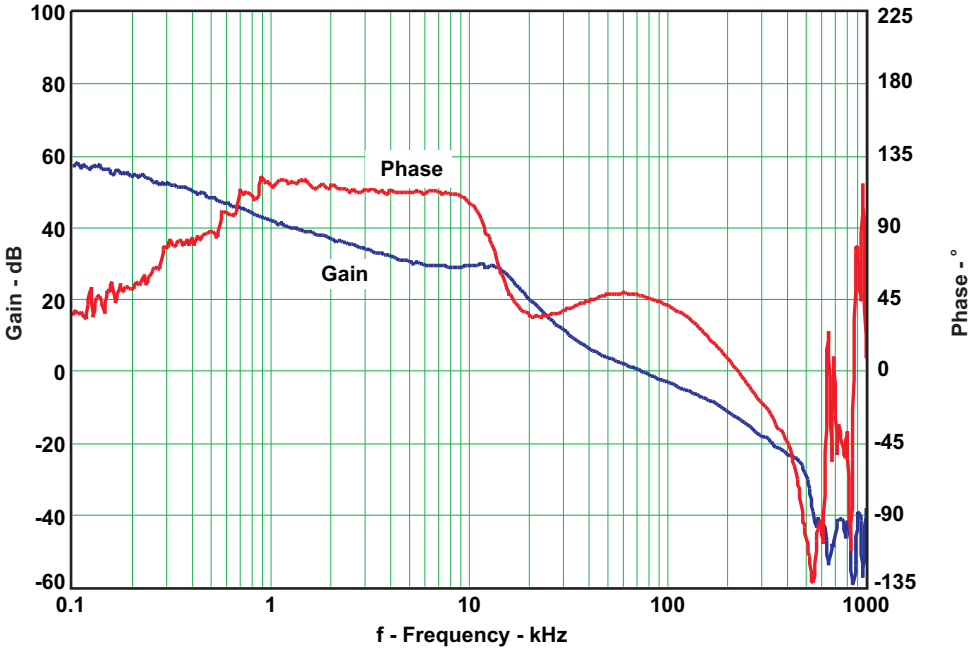


V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 20A

Ch1: TP12 (HDRV), Ch2:13 TP (SW), Ch3: TP14 (LDRV)

Figure 10. CSD163CEVM-591 Switching Waveforms

6.6 Control Loop Bode Diagram



V_{IN} = 14V, V_{OUT} = 1.2V, I_{OUT} = 20A, Bandwidth: 73kHz, Phase Margin: 47°

Figure 11. CSD163CEVM-591 Gain and Phase vs. Frequency

6.7 Additional Waveforms

6.7.1 Output Ripple with Frequency Spread Spectrum (FSS) Enabled

Frequency Spread Spectrum varies the output switching frequency. This change in switching frequency can produce a small change in the output voltage at the modulation frequency. Figure 12 shows the approximately 10mV modulation of the output voltage generated when Frequency Spread Spectrum is enabled.

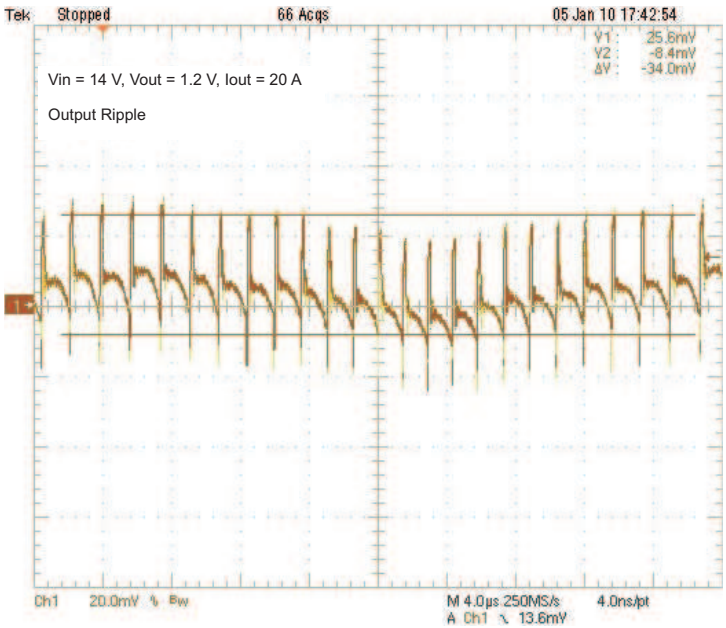


Figure 12. CSD163CEVM-591 Output Ripple with FSS Enabled

7 CSD163CEVM-591 Assembly Drawings and Layout

The following figures (Figure 13 through Figure 18) show the design of the CSD163CEVM-591 printed circuit board. The EVM has been designed using a 4-layer, 2oz. copper-clad circuit board 3" × 3" with all populated components on the top to allow the user to view, probe and evaluate the TI DualCool™ NexFETs in a practical 4-layer application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

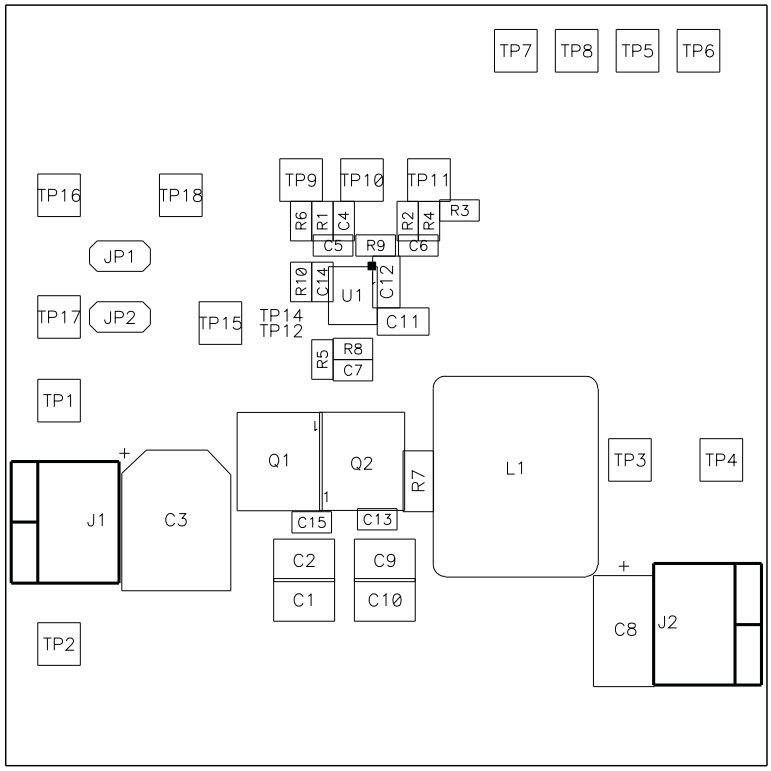


Figure 13. CSD163CEVM-591 Top Component Placement (Top View)

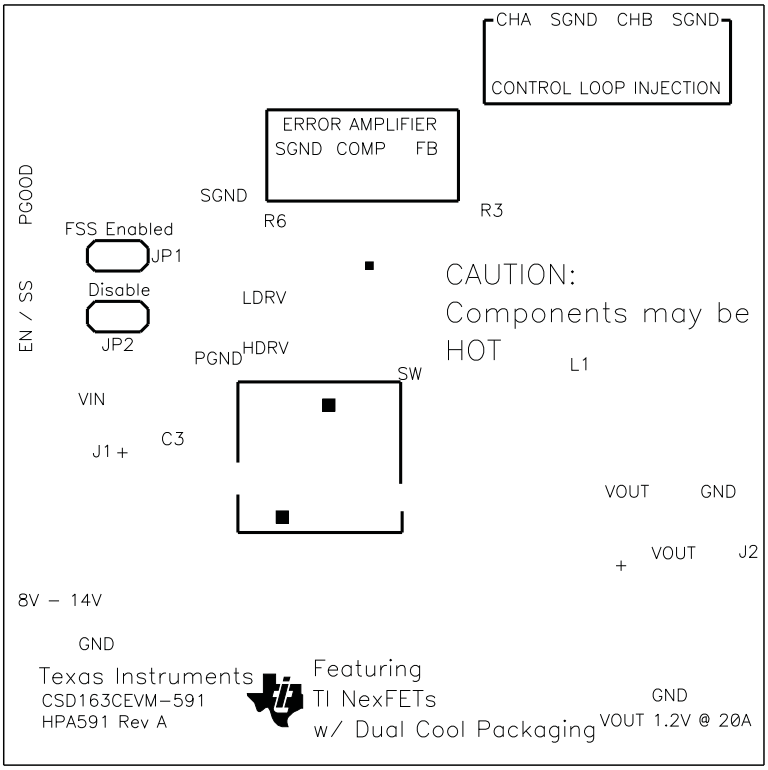


Figure 14. CSD163CEVM-591 Silk Screen (Top View)

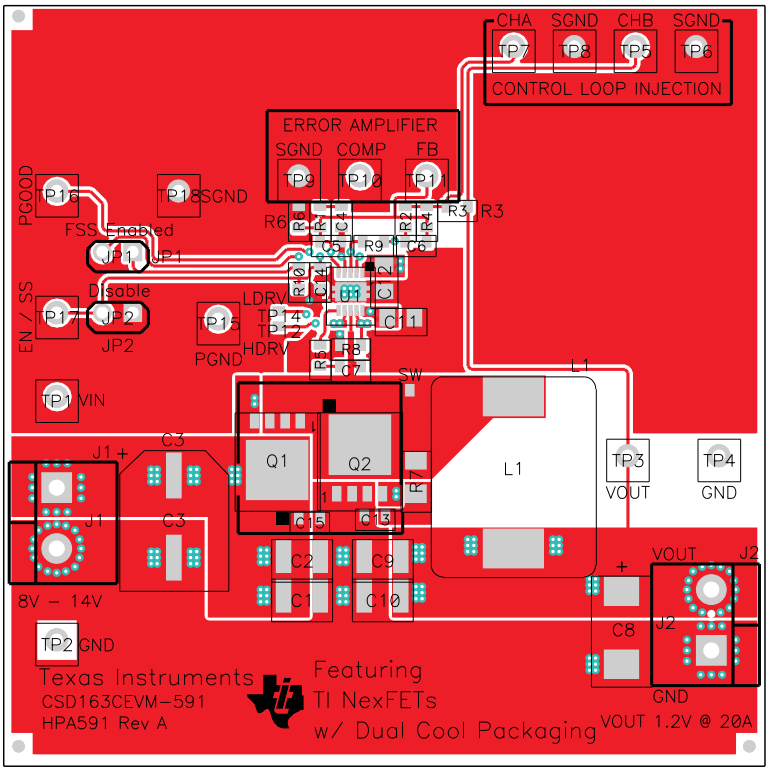


Figure 15. CSD163CEVM-591 Top Copper (Top View)

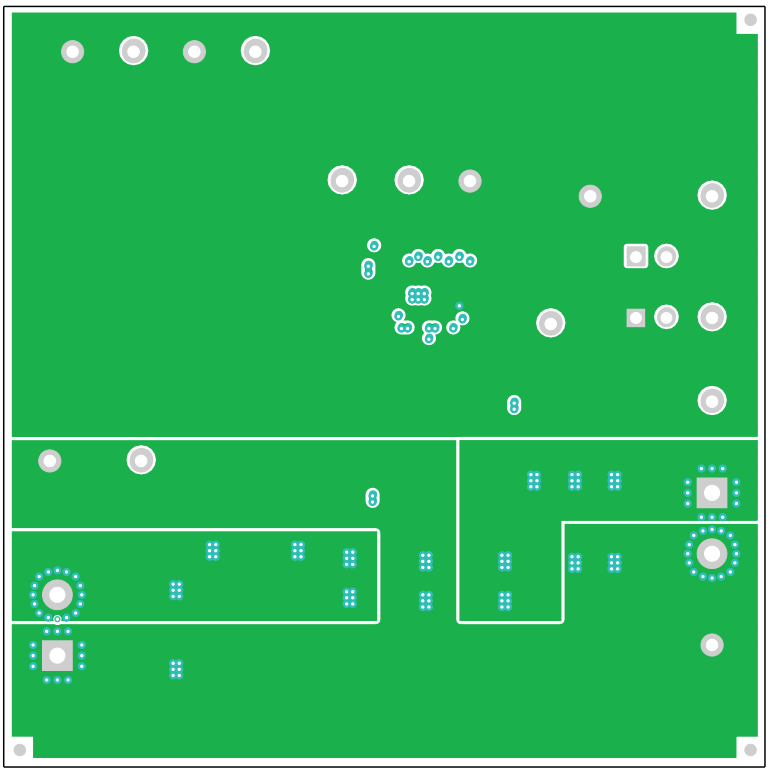


Figure 16. CSD163CEVM-591 Bottom Copper (Top View)

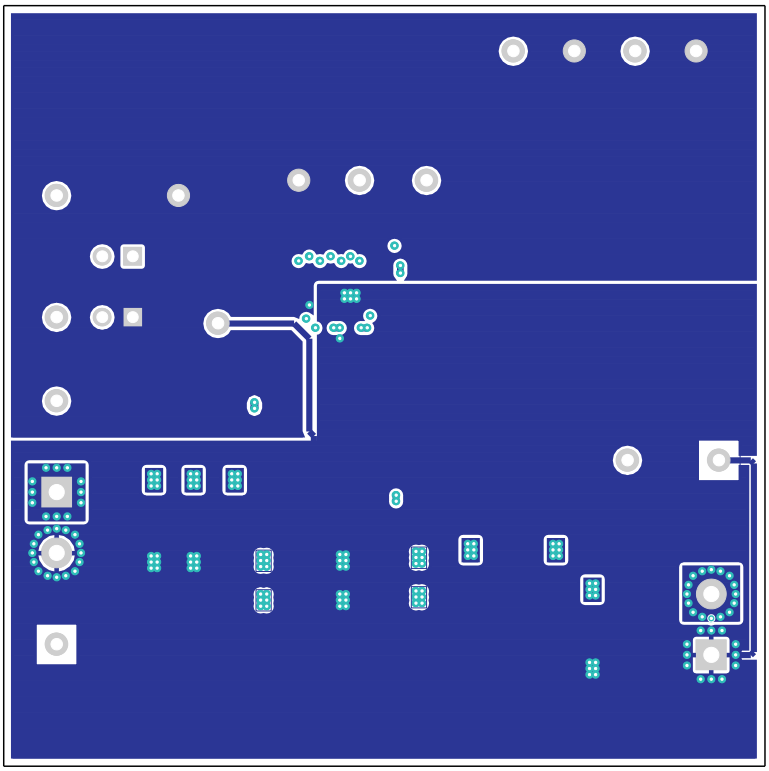


Figure 17. CSD163CEVM-591 Internal 1 (X-Ray Top View)

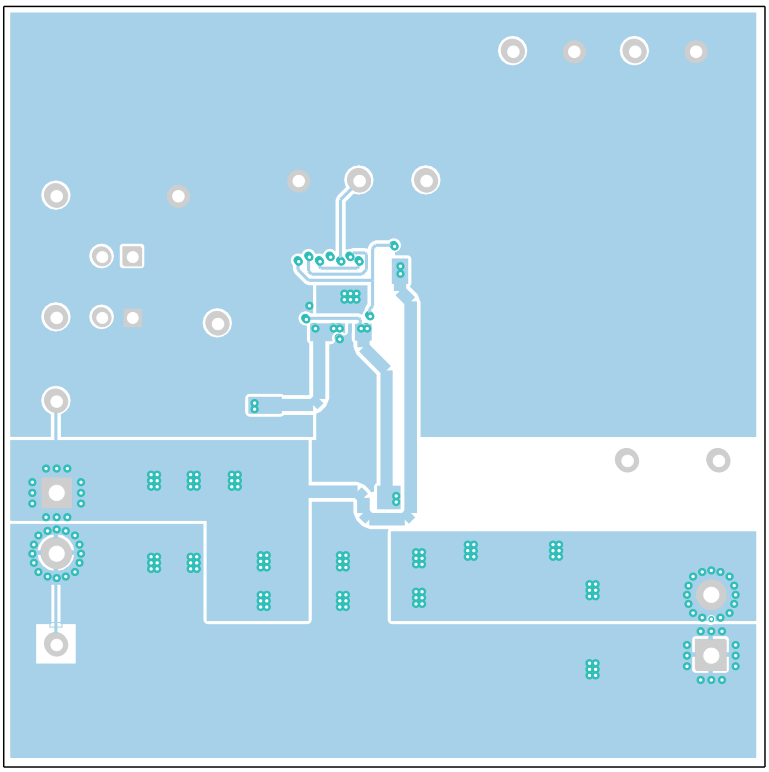


Figure 18. CSD163CEVM-591 Internal 2 (X-Ray Top View)

8 CSD163CEVM-591 Bill of Materials

Table 3. CSD163CEVM-591 Bill of Materials[1][2][3]

QTY	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2	10uf	Capacitor, Ceramic, 25-V, X7R, 10%	1210	Std	Std
1	C11	4.7uF	Capacitor, Ceramic, 10-V, X7R, 20%	0805	Std	Std
1	C12	1uF	Capacitor, Ceramic, 25-V, X7R, 20%	0805	Std	Std
1	C13	1.0nF	Capacitor, Ceramic, 25V, X5R, 20%	0603	Std	Std
1	C14	3.3nF	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
1	C15	1.0uF	Capacitor, Ceramic, 25V, X7R, 20%	0603	Std	Std
1	C3	330uF	Capacitor, Aluminum, 25V, ±20%, 160mohms	0.328 x 0.390 inch	EEEFK1E331P	Panasonic
2	C4, C6	680pF	Capacitor, Ceramic, 25V, COG, 10%	0603	Std	Std
1	C5	100pF	Capacitor, Ceramic, 25V, COG, 10%	0603	Std	Std
1	C7	100nF	Capacitor, Ceramic, 16V, X7R, 20%	0603	Std	Std
1	C8	220uF	Capacitor, POSCAP, 6.3-V, 25milliohm, 105C, 20%	7343(D)	6TPE220M	Sanyo
2	C9, C10	47uF	Capacitor, Ceramic, 6.3-V, X5R, 20%	1210	Std	Std
2	J1, J2	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
2	JP1, JP2	PEC02SAAN	Header, 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	0.45uH	Inductor, SMT, 25A	0.512 x 0.571 inch	MLC1565-451MLB	Coil Craft
1	Q1[4][5]	CSD16322Q5C	MOSFET, N-Chan, 25V, 21 A, 4.6 milli-ohm, Dual Cool	QFN-8 POWER	CSD16322Q5C	TI
1	Q2[4][5]	CSD16325Q5C	MOSFET, N-Chan, 25V, 33 A, 1.7 milli-ohm, Dual Cool	QFN-8 POWER	CSD16325Q5C	TI
3	R1, R4, R6	10.0K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R10	267K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	1.50K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	2	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	2.2	Resistor, Chip, 1/8W, 5%	1206	Std	Std
1	R8	4.02K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	100K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	TP1, TP3	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
0	TP12, TP13, TP14	N/A	Test Point, SM, 2x3mm	0.118 x 0.079 inch		
6	TP2, TP4, TP6, TP8, TP15, TP18	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
7	TP5, TP7, TP9, TP10, TP11, TP16, TP17	5002	Test Point, White, Thru Hole Color Keyed	0.100 x 0.100 inch	5002	Keystone
1	U1[4][5]	TPS40304DRC	IC, 3V-20V sync. Buck controller/Enable Light Load/Fq Spread Spectrum	DRC10	TPS40304DRC	TI
2	--		Shunt, 100-mil, Black	0.1	929950-00	3M
1	HS1[6]		HeatSink, 0.54"x0.54"x0.3", Aluminum, Pinned	13.7mm x 13.7mm	3-050505U	CoolInovations
1	GP1 [7]		Thermal Gap Pad, Insulated, 0.020" thk, Natural Tack, Cut to 0.5" x 0.5"	0.5" x 0.5"	GP1500-02-0404	Bergquist
	--		PCB, 2.5 In x 2.5 In x 0.062 In		HPA591	Any

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterisk ('*') cannot be substituted. All other components can be substituted with equivalent MFG's components.
(5) Ref designators marked with a carrot ('^') are included in ESD shipping bag but not populated on PCB
(6) Wrap and tape HS1 with Anti-Static Foam prior to inserting into ESD shielded bag with the PCB assembly
(7) Place GP1 in ESD bag with PCB assembly

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 1.2 V ± 2% .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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