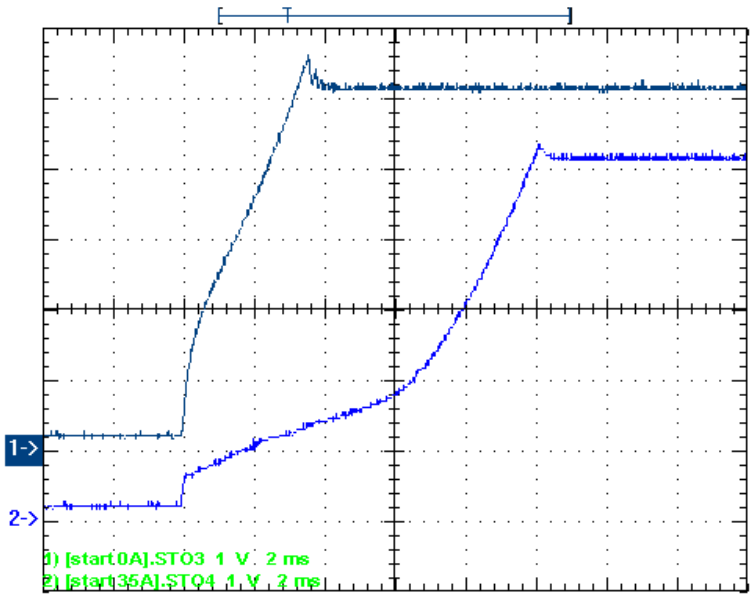
PMP5711RevC Test Results

1 Startup

The startup waveform is shown in Figure 1. The input voltage was set to 48V, with 0A and 35A load current at the output. Startup at full load 35Amps needs 10ms.



Ch1=> output voltage @ 0A Iout

1V/div

Ch2=> output voltage @ 35A Iout

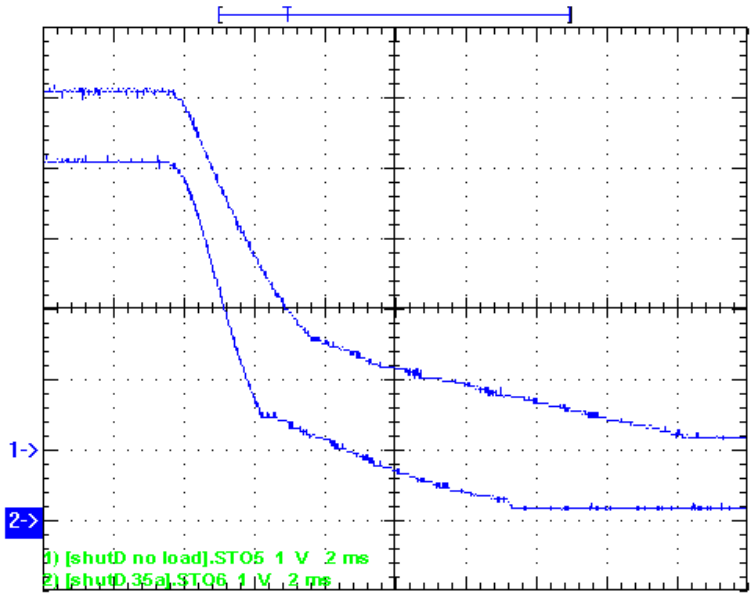
1V/div

2ms/div

Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage was set at 48V, with 0A, and 35A load on the output.



Ch1=> output voltage @ 0A Iout

1V/div

Ch2=> output voltage @ 35A Iout

1V/div

2ms/div

Figure 2

3 Efficiency

The efficiency is shown in Figure 3 below, evaluated at Vmin 36V, Vnom 48V and Vmax 72V; Both voltages are measured directly at input/output capacitors:

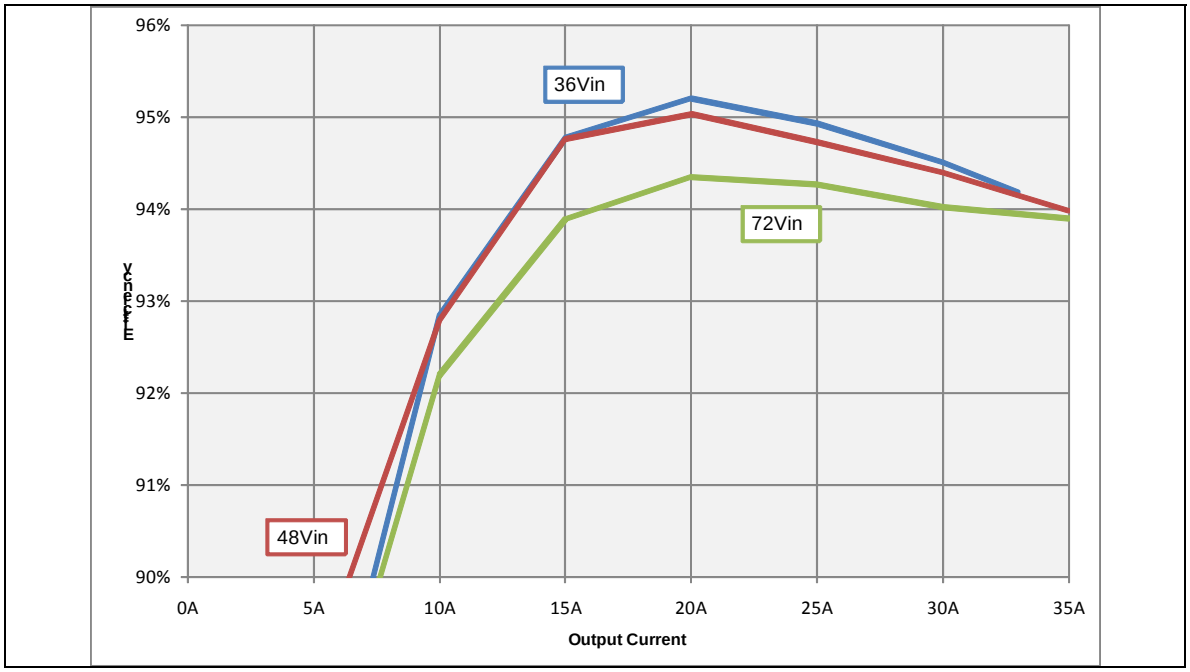


Figure 3

Table 1, Vmin 36V:

VOUT	IOUT	VIN	IIN	POUT	PIN	Eff
5.00	5.04	36.25	0.80	25.2	28.8	87.5%
5.01	10.01	36.24	1.49	50.1	54.0	92.8%
5.01	15.02	36.22	2.19	75.2	79.4	**94.8%**
5.01	20.03	36.21	2.91	100.4	105.4	**95.2%**
5.01	25.00	36.19	3.65	125.3	131.9	**94.9%**
5.01	30.01	36.18	4.40	150.4	159.2	**94.5%**
5.01	32.99	36.17	4.86	165.4	175.6	**94.2%**

Table 2, Vnom 48V:

VOUT	IOUT	VIN	IIN	POUT	PIN	Eff
5.00	5.04	48.48	0.59	25.2	28.4	88.9%
5.01	10.01	48.47	1.11	50.1	54.0	92.8%
5.01	15.02	48.46	1.64	75.2	79.4	**94.8%**
5.01	20.03	48.45	2.18	100.4	105.6	**95.0%**
5.01	25.00	48.44	2.73	125.3	132.2	**94.7%**
5.01	30.01	48.43	3.29	150.4	159.4	**94.4%**
5.02	35.02	48.42	3.86	175.7	186.9	**94.0%**

Table 3, Vmax 72V:

VOUT	IOUT	VIN	IIN	POUT	PIN	Eff
5.00	5.04	71.80	0.40	25.2	28.8	87.6%
5.01	10.01	71.79	0.76	50.1	54.3	92.2%
5.01	15.02	71.78	1.12	75.2	80.1	**93.9%**
5.01	20.03	71.77	1.48	100.4	106.4	**94.3%**
5.01	25.00	71.77	1.85	125.2	132.8	**94.3%**
5.01	30.01	71.76	2.23	150.4	160.0	**94.0%**
5.01	35.00	71.57	2.61	175.5	186.9	**93.9%**

4 Load Regulation

The load regulation of the output is shown in the **Figure 4** below, precision is +14mV, so 0.28%.

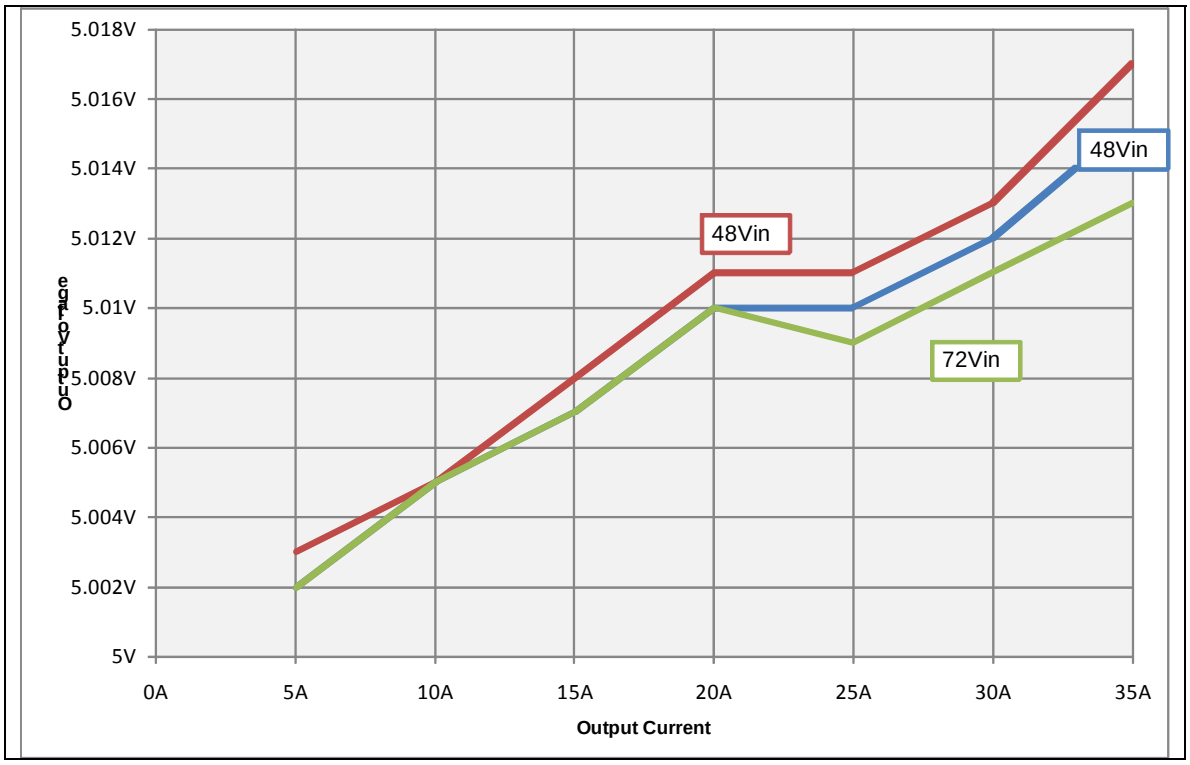


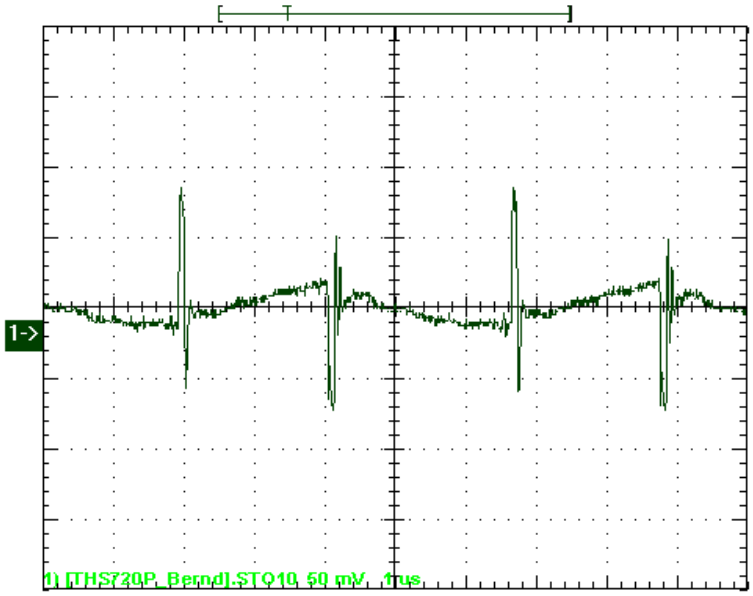
Figure 4

5 Line Regulation

No influence of the output voltage to the input voltage (36V to 72V). The current was set to 20A, voltage stayed constant at 5.011V by covering total input voltage range.

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 5. The image was taken with a 35 A load and 48V at the input. Voltage ripple du is 40mVpp, noise is 110mVp.



Ch1 =>output voltage 50mV/Div

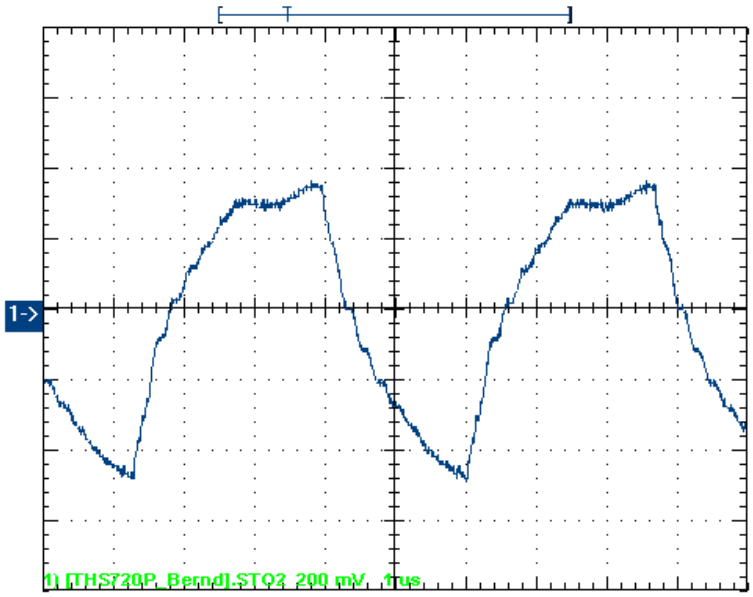
20MHz bandwidth setting

1µs/div

Figure 5

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 6 and Figure 7. The input voltage was set to 48V with 20A output current.



without bulk capacitor

Ch1 =>input voltage **200mV**/Div

20MHz bandwidth setting

1µs/div

Figure 6

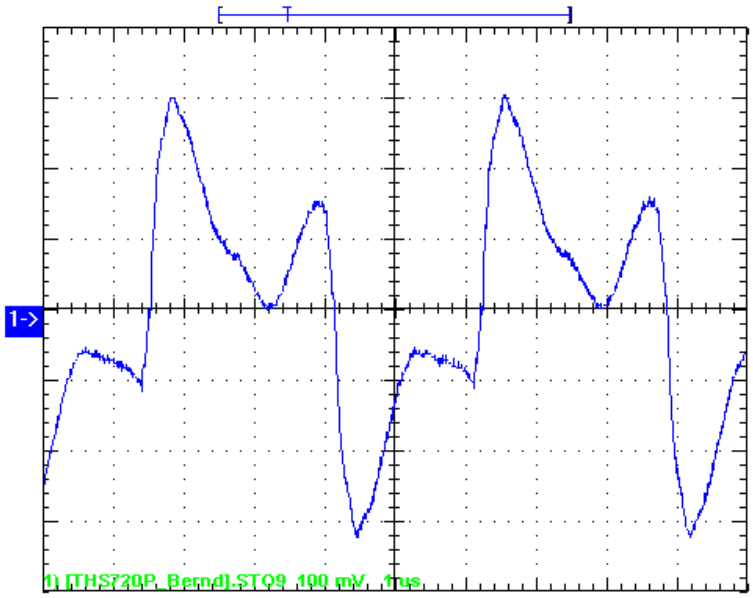


Figure 7

with bulk capacitor (680µF)

Ch1 =>input voltage **100mV**/Div

20MHz bandwidth setting

1µs/div

8 Control Loop Frequency Response

Figure 8 shows the loop @ 30A with input voltages Vmin 36V / Vnom 48V / Vmax 72V:

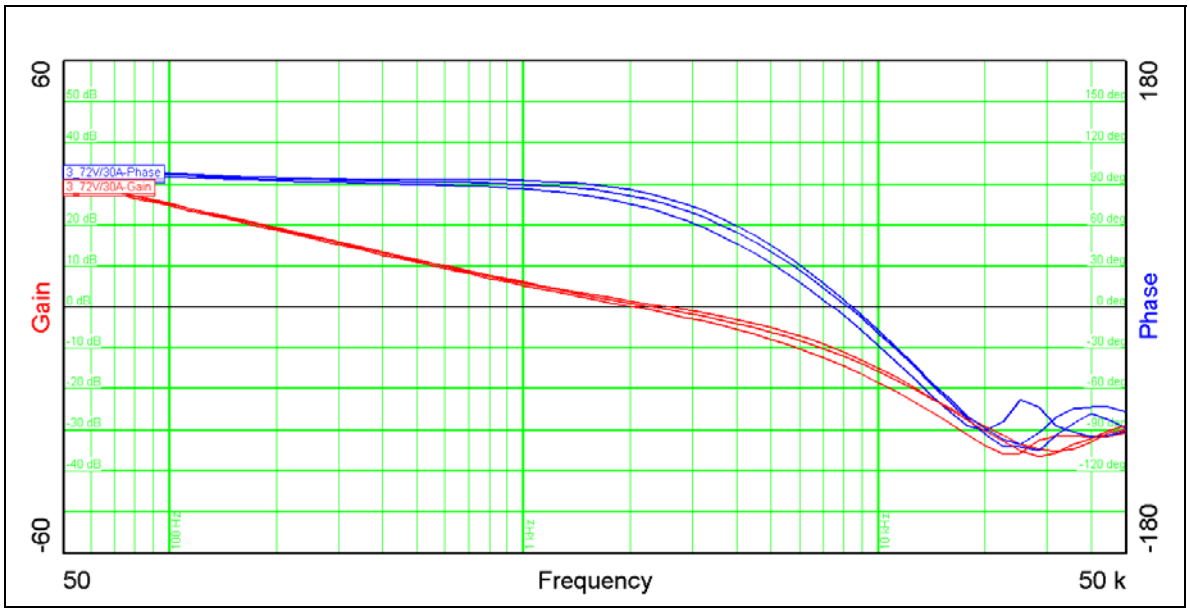


Figure 8

Table 4 summarizes the results from Figure 8

	36Vin	48Vin	72Vin
Bandwidth (kHz)	2.04	2.31	2.55
Phasemargin	75°	77.8°	79.5°
slope (20dB/decade)	-0.87	-0.80	-0.74
gain margin (dB)	-13.3	12.6	-11.9
slope (20dB/decade)	-1.79	-1.8	-1.9
freq (kHz)	7.45	8.23	8.45

Table 4

9 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 15A to 30A.with 100Hz frequency. Input voltage was set to 48V.

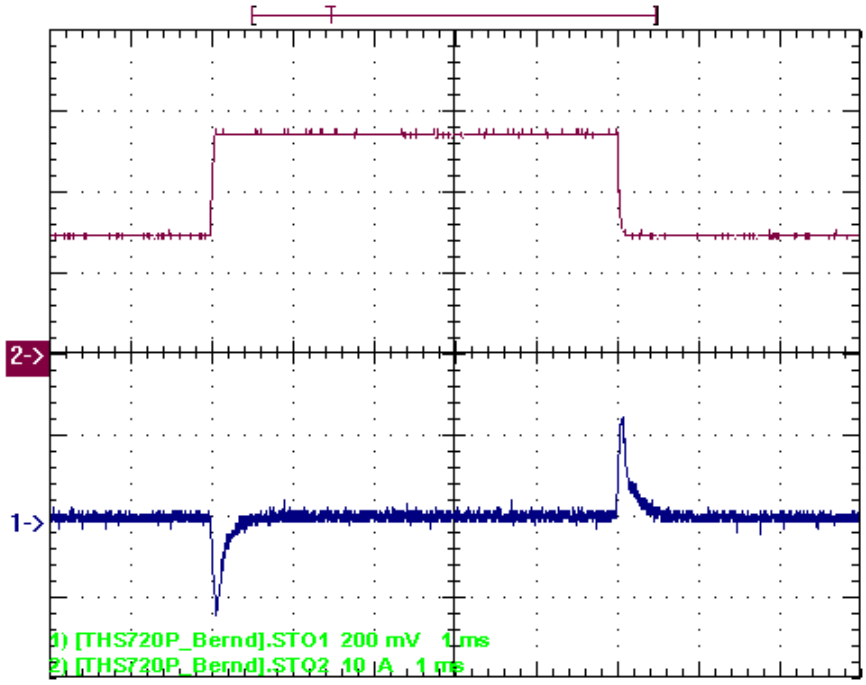


Figure 9

Ch2 => output current 10A/div

Ch1 => output voltage 200mV/div

20MHz bandwidth setting

1ms/div

10 Waveforms

10.1 Primary FET Vds

With input voltage set to 48V results in the waveform shown in Figure 10; output current was set to 20A. *Keep in mind – NMOS conducts as gate is high, figures are not in phase:*

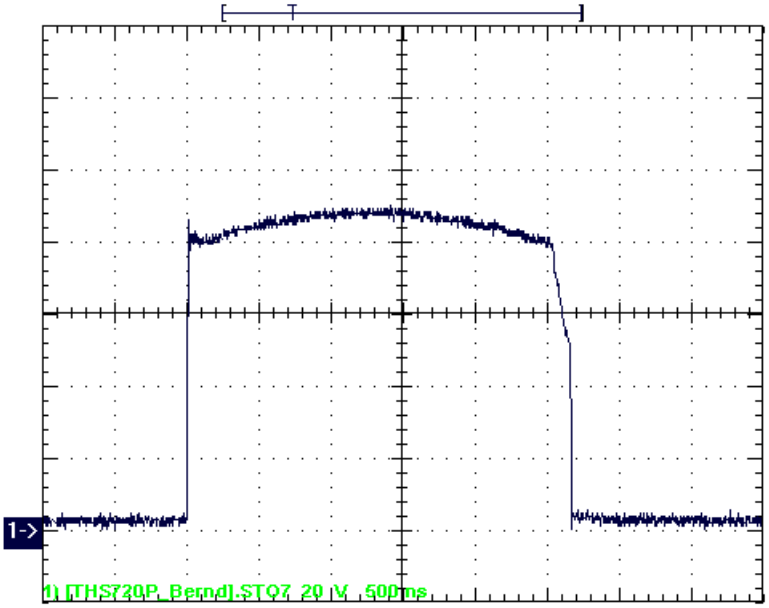


Figure 10

Ch1 =>
20V/div

500ns/div

full bandwidth

Figure 11 shows the Gate-Source voltage Vgs of the same FET

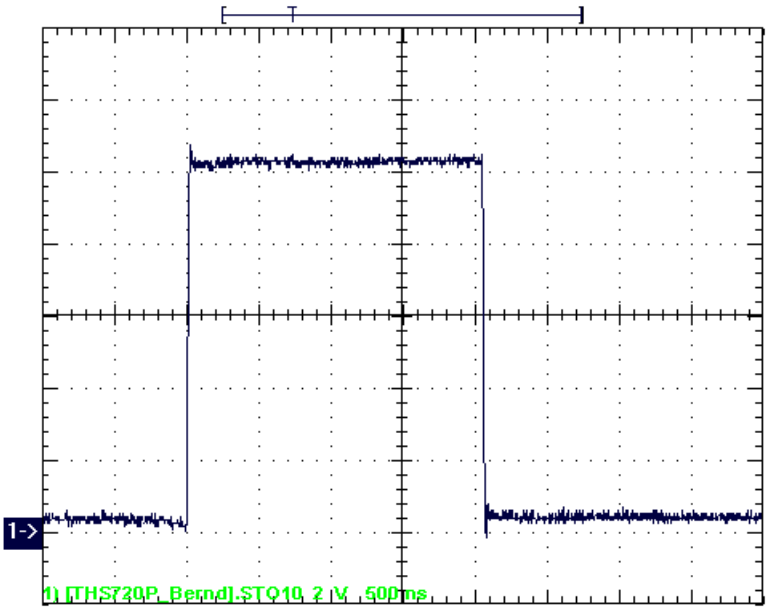


Figure 11

Ch1 =>
2V/div

500ns/div

full bandwidth

10.2 Active Clamp FET Vds

With input voltage set to 48V results in the waveform shown in Figure 12; output current was set to 20A.

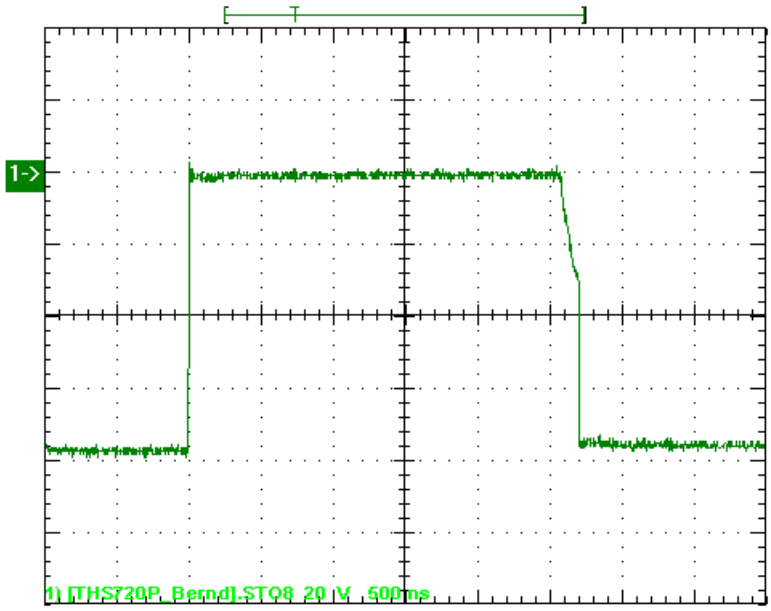


Figure 12

Ch1 =>
20V/div

500ns/div

full bandwidth

Figure 13 shows the Gate-Source voltage Vgs of the same FET

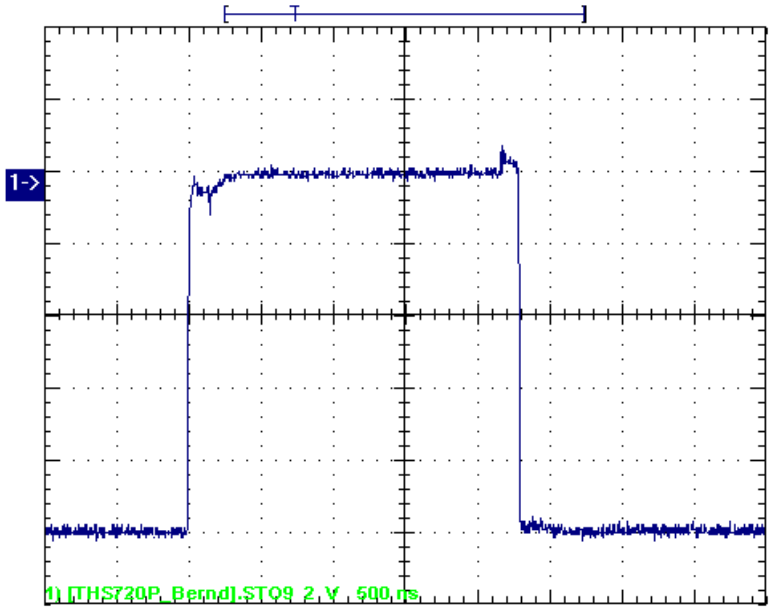


Figure 13

Ch1 =>
2V/div

500ns/div

full bandwidth

10.3 Freewheeling FET, secondary side

With input voltage set to 48V results in the waveform shown in Figure 14; output current was set to 20A.

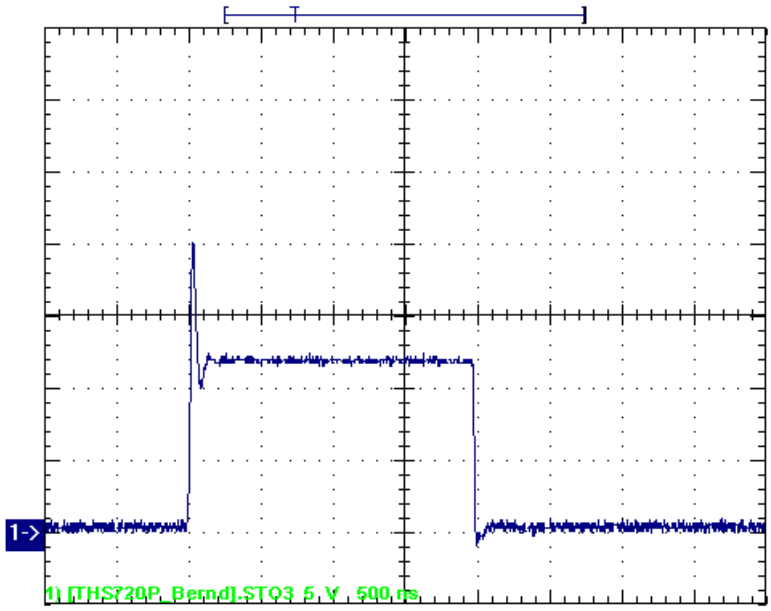


Figure 14

Ch1 =>
5V/div

500ns/div

full bandwidth

Figure 15 shows the Gate-Source voltage of the same FET

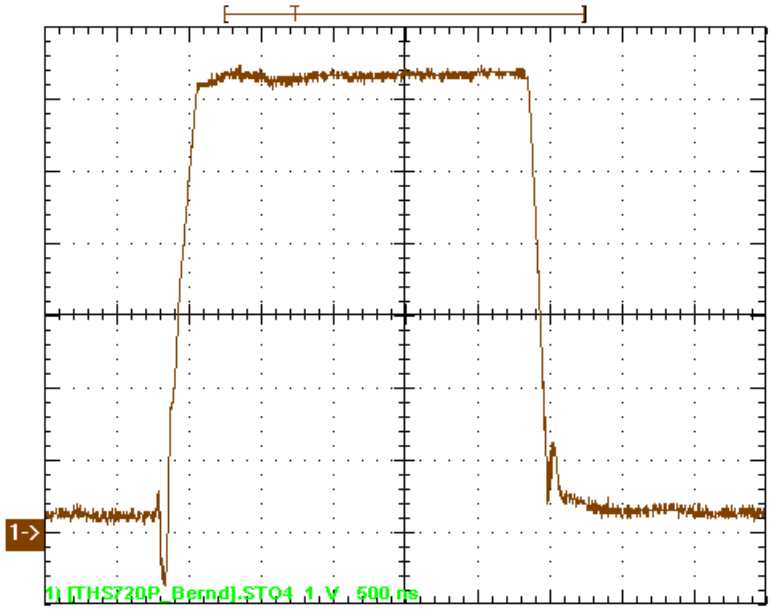


Figure 15

Ch1 =>
1V/div

500ns/div

full bandwidth

10.4 Synchronous Rectifier, secondary side

With input voltage set to 48V results in the waveform shown in Figure 16 Output current was set to 20A.

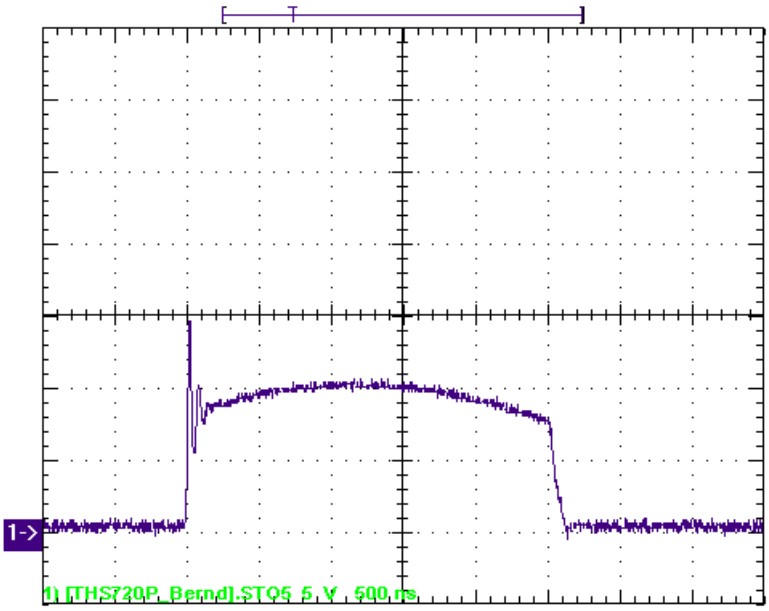


Figure 16

Ch1 =>
5V/div

500ns/div

full bandwidth

Figure 17 shows the Gate-Source voltage of the same FET

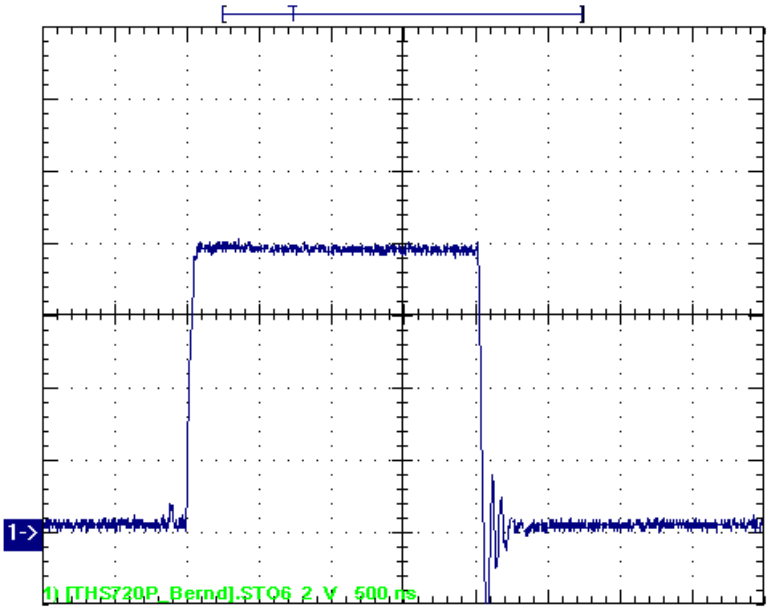


Figure 17

Ch1 =>
2V/div

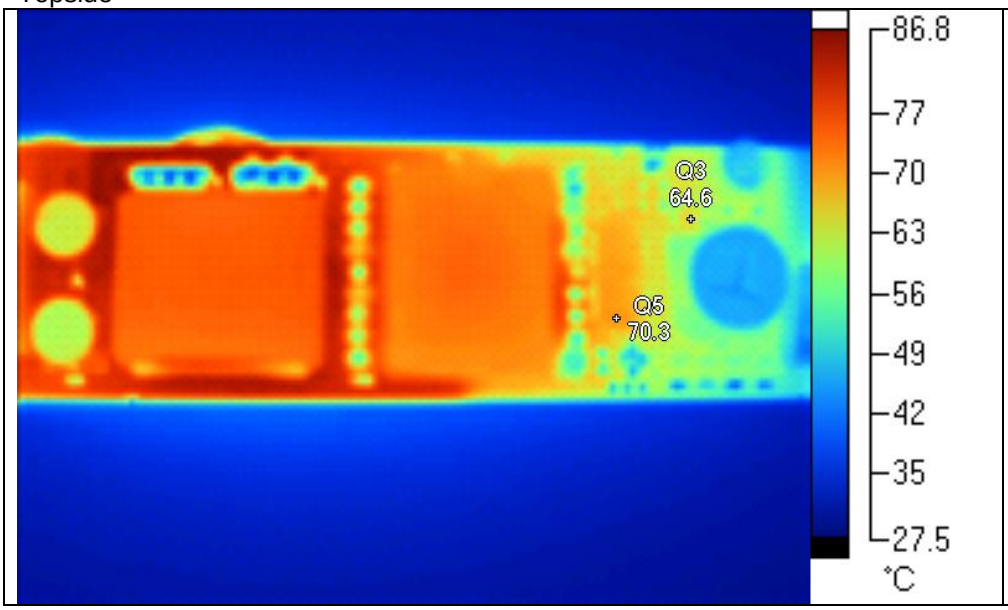
500ns/div

full bandwidth

11 Thermal Image

11.1 25A load current, no air flow, convectional cooling:

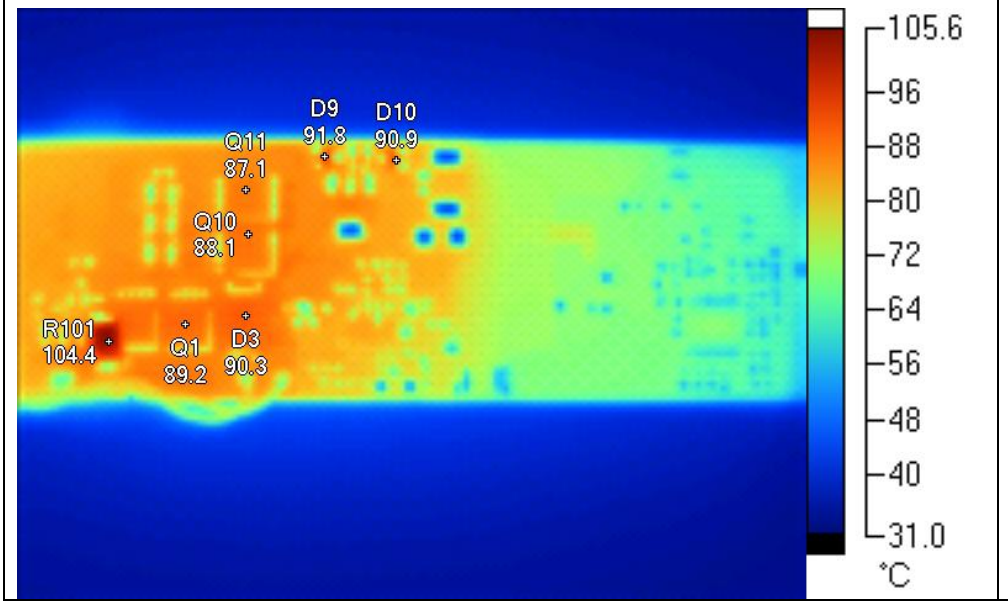
Topside



Name	Temperature
Q5	70.3°C
Q3	64.6°C

Figure 18

Bottomside

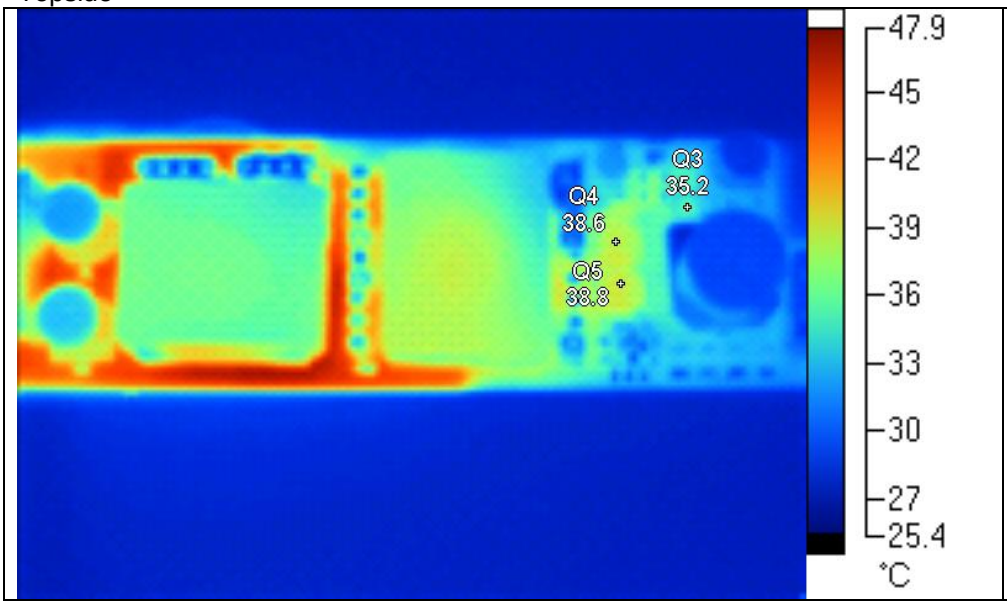


Name	Temperature
R101	104.4°C
Q1	89.2°C
D3	90.3°C
Q11	87.1°C
Q10	88.1°C
D9	91.8°C
D10	90.9°C

Figure 19

11.2 35A with forced air flow 2m/s / 400lfm:

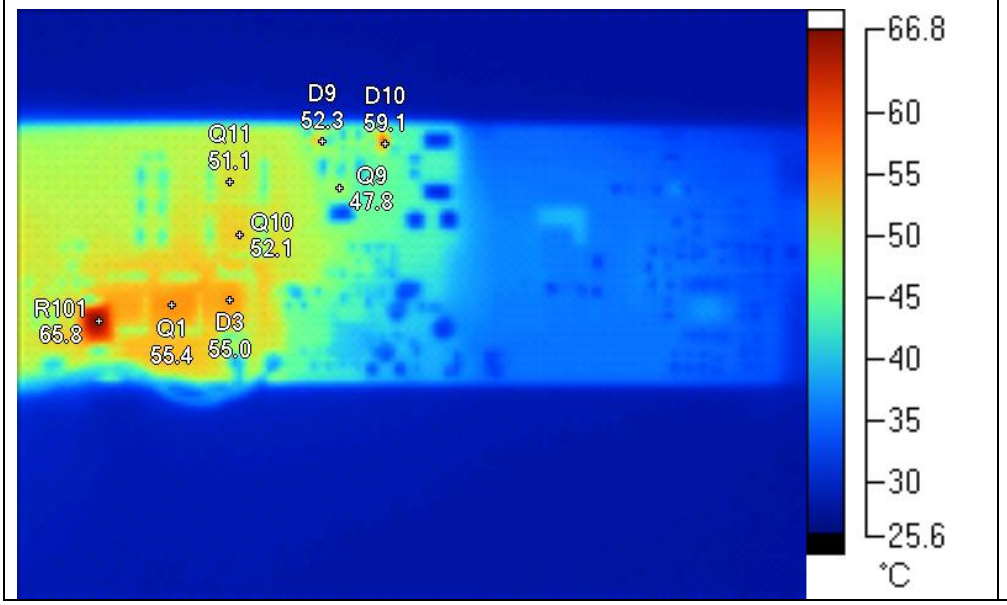
Topside



Name	Temperature
Q5	38.8°C
Q4	38.6°C
Q3	35.2°C

Figure 20

Bottomside



Name	Temperature
R101	65.8°C
D10	59.1°C
D9	52.3°C
Q1	55.4°C
D3	55.0°C
Q9	47.8°C
Q10	52.1°C
Q11	51.1°C

Figure 21

12 Miscellaneous Measurements

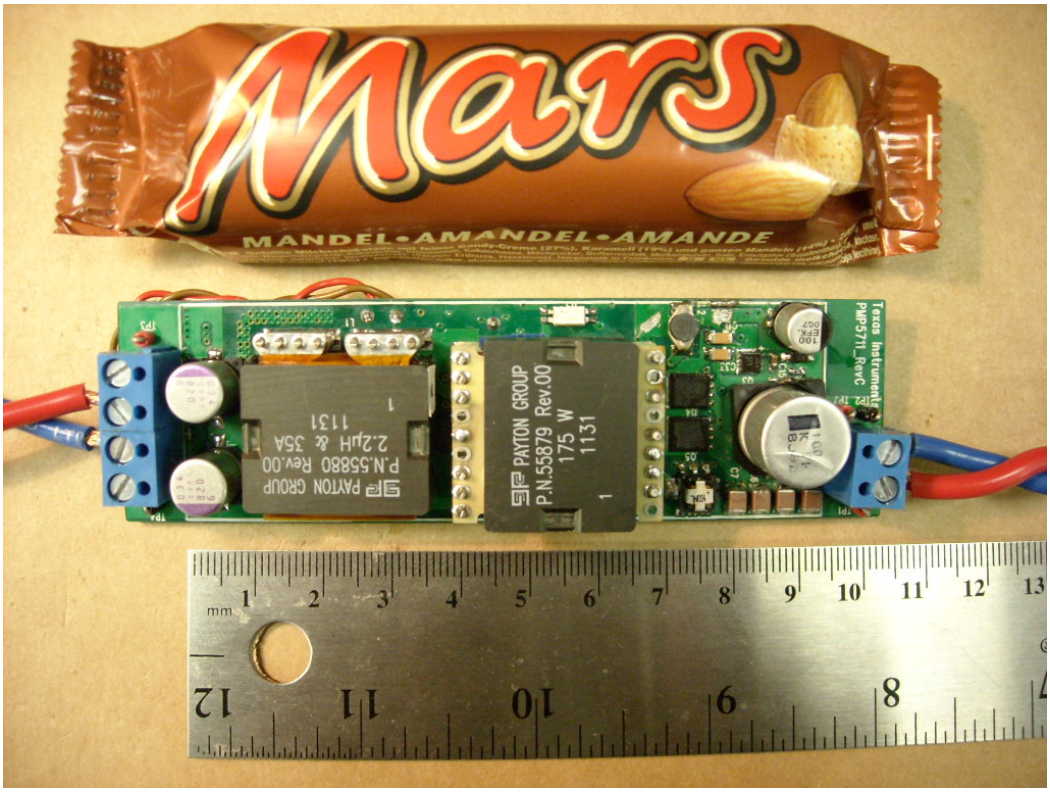
- Bias Voltage 10.36 at nominal input 48V / 20Amps output
  total variation across line and load is:
  9.15V (36Vin/0Aout) to 11.56V (72Vin/35Aout)
- UV ON 36.1V
- UV OFF 34.5V
- OV ON 71.5V
- OV OFF 72.1V
- Fsw 211kHz
- Rise of full load at 36Vin is limited to 33A due to CS limitation.

13 Summary & Pic

With an efficiency of >94% across 13Amps load to 35Amps full load and peak efficiency of 95% the results for a 5V forward converter are fine.
Due to space requirements the design is made as small as possible and is specified for forced cooling. Achieved size is L x W x H = 93mm x 31mm x 19mm.

If REMOTE SENSE isn't a must go for rugged TL431 as error amplifier. If dealing w/ TL103 select proper placement at secondary side and root shielding ground plane below this IC. So some caps could be removed and bandwidth could be doubled.

To reduce ringing on secondary side place RC snubber directly to Q1/Q2.



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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265