TPS40200 Buck Boost Evaluation Board Test Report for Alcatel-Lucent.

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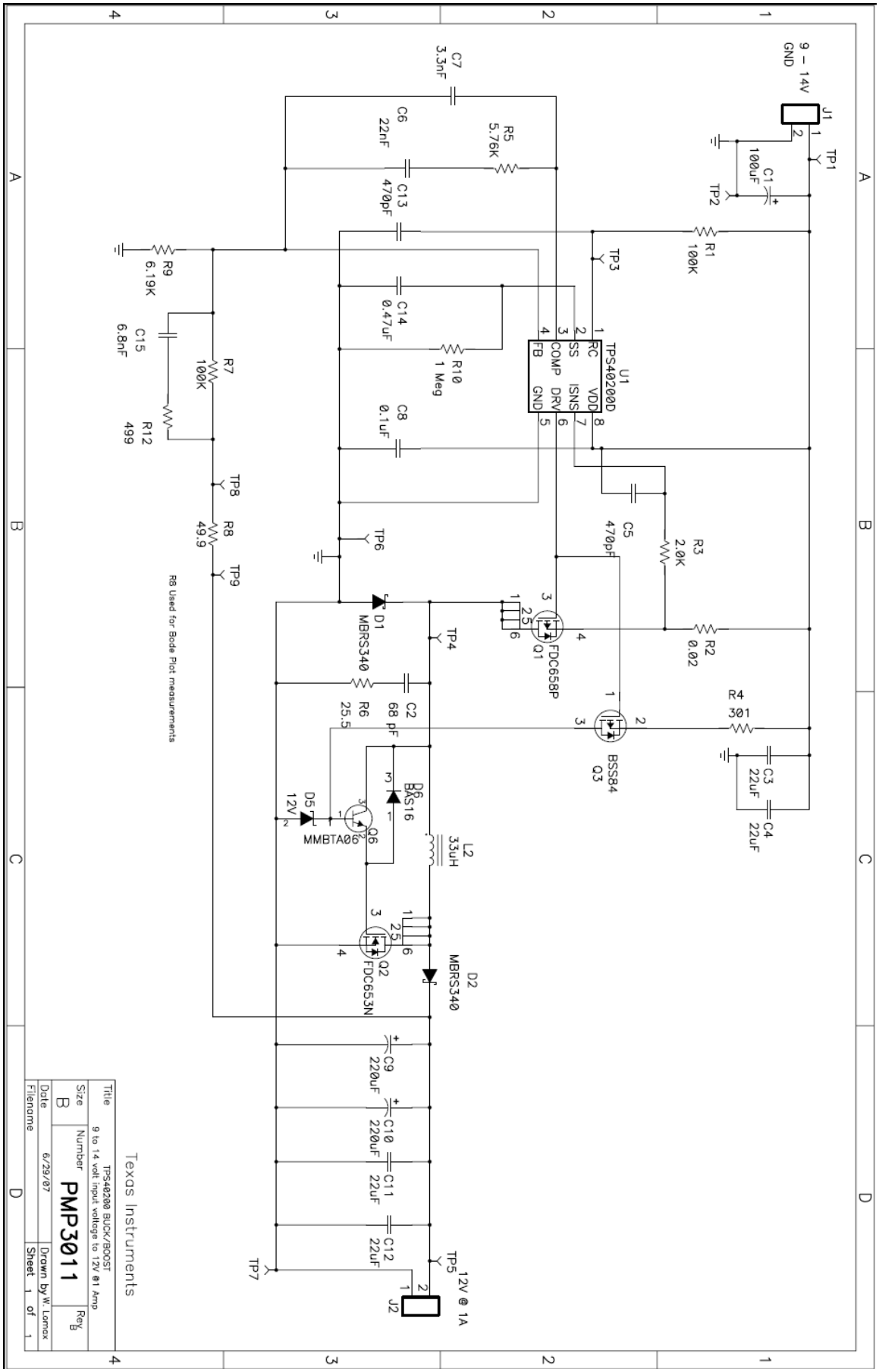
Design notes:

The PMP3011 Rev B design uses the TPS40200 buck controller to create a two switch two rectifier buck boost circuit. The high side P channel Fet Q1 and the low side N channel Fet Q2 are switched on at the same time. A current limited level shift gate drive circuit using R4, Q3, and Q6 creates the gate drive for Q2. The gate of Q2 could also be tied to the node at TP4 with a low value resistor, such as 10 ohms, as long as the peak voltage will not destroy the gate of the FET. The level shift gate drive circuit uses D5 to clamp the maximum voltage on Q2 gate to less than 12V. R4 limits the peak current suppled to the base of Q6 to turn Q2 on, and this circuit can be extended to work at voltages higher than 14V in if needed. Since the design uses diodes as rectifiers, the inductor current can be discontinuous at light loads. If the load is light enough to enter discontinuous mode and a load step transient occurs, the transient response will be worse than if it occurs when the supply is in continuous mode.

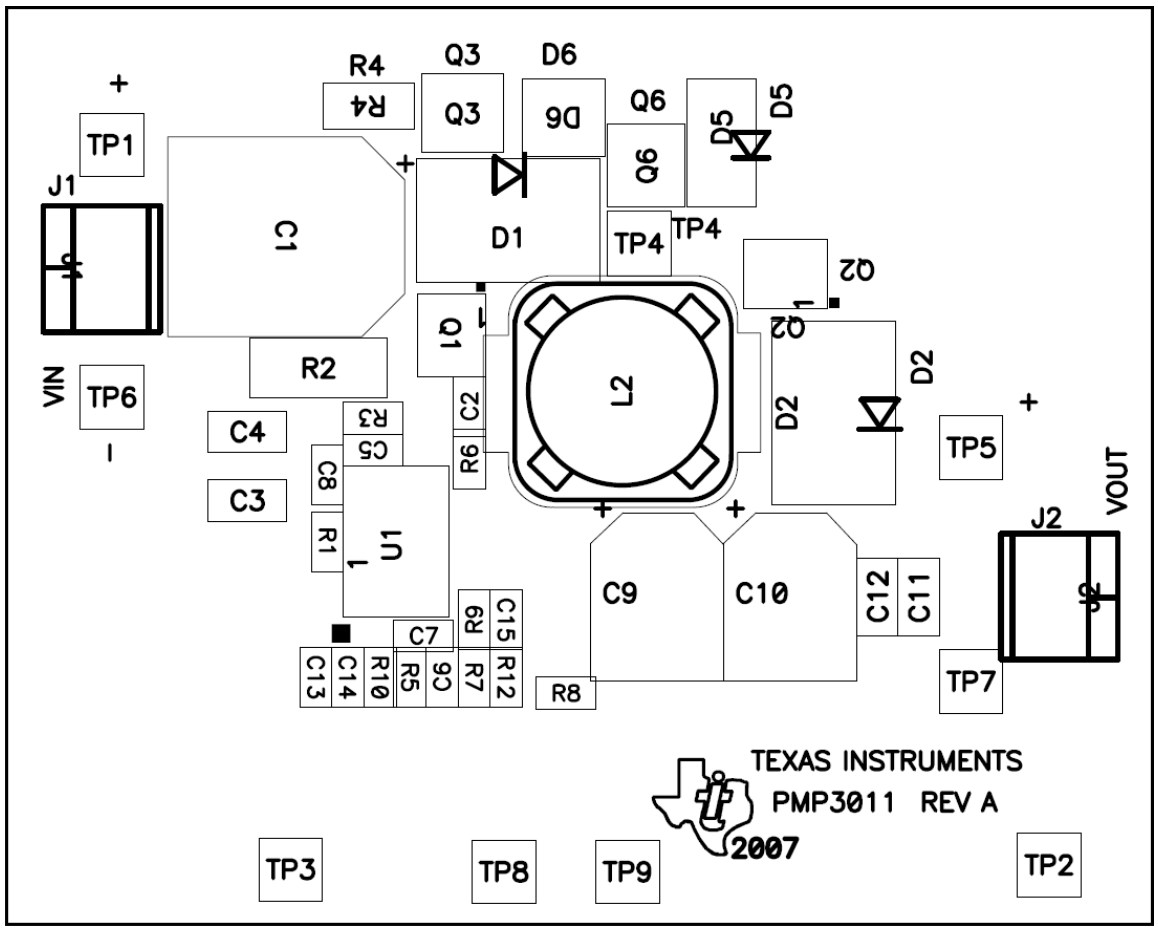
A mix of electrolytic and ceramic capacitors are used in this design. If lower input and output ripple is desired, the electrolytic capacitors could be replaced with lower ESR capacitors, or more ceramic capacitors could be added. The compensation network is a type 3, (3 poles, 2 zeros) so it is possible to compensate the loop for all ceramic output capacitors if needed.

The following tests were performed on the EVM:
Efficiency vs load at 9V, 12V, and 14V in
Output ripple at 1A load 12V in
Input ripple at 1A load 12V in
Switch node A and B waveform at 1A load
Gate drive B waveforms at 9V and 14V
Transient response from 200mA to 1A load step at 160mA/uS
Loop response at various load currents and voltages.

Schematic


9 – 14V
GND
J1
TP1
TP2
C1
100uF
C7
3.3nF
C6
22nF
R5
5.76K
C13
470pF
R1
100K
TP3
R9
6.19K
C14
0.47uF
C15
6.8nF
R7
100K
R10
1 Meg
R12
499
U1
TPS40200D
RC
SS
COMP
FB
VDD
ISNS
DRV
GND
C8
0.1uF
TP8
R8
49.9
TP9
TP6
C5
470pF
R3
2.0K
R2
0.02
D1
MBRS340
TP4
Q1
FDC658P
R4
301
Q3
BSS84
C3
22uF
C4
22uF
C2
68 pF
R6
25.5
R6 Used for Bode Plot measurements
D6
BAS16
D5
12V
Q6
MMBTA06
L2
33uH
Q2
FDC653N
D2
MBRS340
C9
220uF
C10
220uF
C11
22uF
C12
22uF
TP7
TP5
12V @ 1A
J2
Texas Instruments
Title
TPS40200 BUCK/BOOST
9 to 14 volt input voltage to 12V @1 Amp
Size
B
Number
PMP3011
Rev
B
Date
6/29/07
Drawn by W. Lomax
Filename
Sheet 1 of 1

Placement

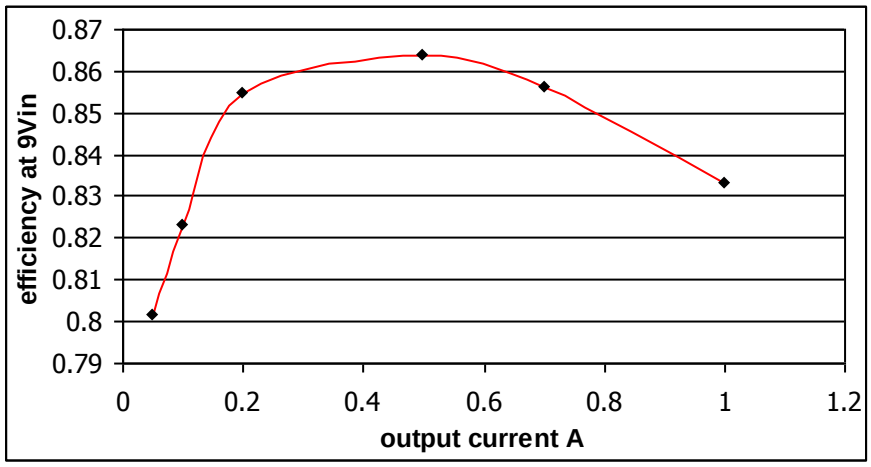

TP1
J1
C1
D1
Q3
D6
R4
Q6
D5
TP4
Q2
L2
D2
TP5
VOUT
J2
VIN
TP6
R2
C4
C3
C5
C8
R1
U1
C2
R6
Q1
C7
C9
C10
C12
C11
TP7
R8
C13
C14
R10
R5
C6
R7
R12
R9
C15
TEXAS INSTRUMENTS
PMP3011 REV A
2007
TP3
TP8
TP9
TP2

Bill of Materials:

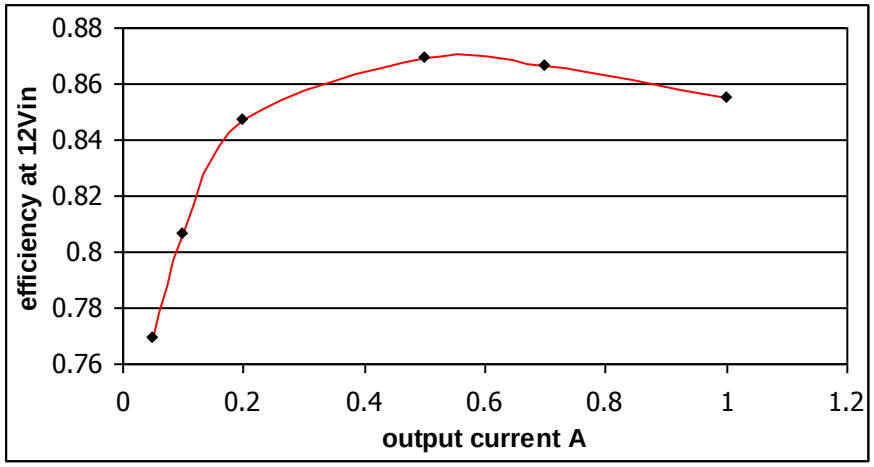
COUNT	RefDes	Value	Description	Size	Part Number	Mfr
1	C1	100uF	Capacitor, Aluminum, 63-V, 20%	0.457 x 0.406	EEVFK1J101P	Panasonic
4	C11, C12, C3, C4	22uF	Capacitor, Ceramic, 16V, X5R, 20%	1210	Std	Std
1	C14	0.47uF	Capacitor, Ceramic, 16-V, X5R, 20%	0603	Std	Std
1	C15	6.8nF	Capacitor, Ceramic, 50-V, X7R, 20%	0603	Std	Std
1	C2	68 pF	Capacitor, Ceramic, 50V, X7R, 20%	0603	Std	Std
2	C5, C13	470pF	Capacitor, Ceramic, 50-V, X7R, 20%	0603	Std	Std
1	C6	22nF	Capacitor, Ceramic, 50-V, X7R, 20%	0603	Std	Std
1	C7	3.3nF	Capacitor, Ceramic, 50-V, X7R, 20%	0603	Std	Std
1	C8	0.1uF	Capacitor, Ceramic, 50-V, X7R, 20%	0603	Std	Std
2	C9, C10	220uF	Capacitor, Aluminum, 16V, ±20%	0.260 x 0.276 inch	EEEVFK1C221XP	Panasonic
2	D1, D2	MBRS340	Diode, Schottky, 3A, 40V	SMC	MBRS340	On Semi
1	D5	12V	Diode, zener 1W, 12V	SMA	SMAZ12-13-F	Onsemi
1	D6	BAS16	Diode, Switching, 150-mA, 75-V, 350mW	SOT23	BAS16	Vishay-Liteon
2	J1, J2	ED1514	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25	ED1514	OST
1	L2	33uH	Inductor, SMT, 33-uH, 3.23-A, 0.06-ohm	0.492 sq"	DR127-330	Coiltronics
1	Q1	FDC658P	Transistor, MOSFET, Pch, -4A, -30V, 50milliohm	SuperSOT-6	FDC658P	Fairchild
1	Q2	FDC653N	Transistor, MOSFET, Nch, 5A, 30V	SuperSOT-6	FDC653N	Fairchild
1	Q3	BSS84	MOSFET, Pch, -50V, -0.13A, 10 Ohm	SOT23	BSS84	Infineon
1	Q6	MMBTA06	Bipolar, NPN, SOT23	SOT23	MMBTA06	ON Semi
2	R1, R7	100K	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R10	1 Meg	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R12	499	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R2	0.02	Resistor, Chip, 1/2-W, 5%	2010	Std	Std
1	R3	2.0K	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R4	301	Resistor, Chip, 1/8W, yy%	1206	Std	Std
1	R5	5.76K	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R6	25.5	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R8	49.9	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	R9	6.19K	Resistor, Chip, 1/16-W, 1%	0603	Std	Std
1	U1	TPS40200D	IC, Low Cost Sync Buck Controller	SO-8	TPS40200D	TI

Efficiency vs. load

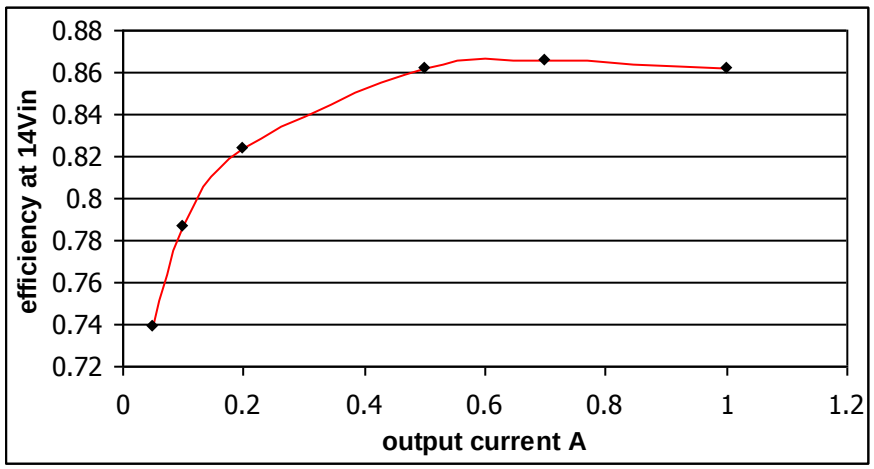
9V in efficiency plot



12V in efficiency plot

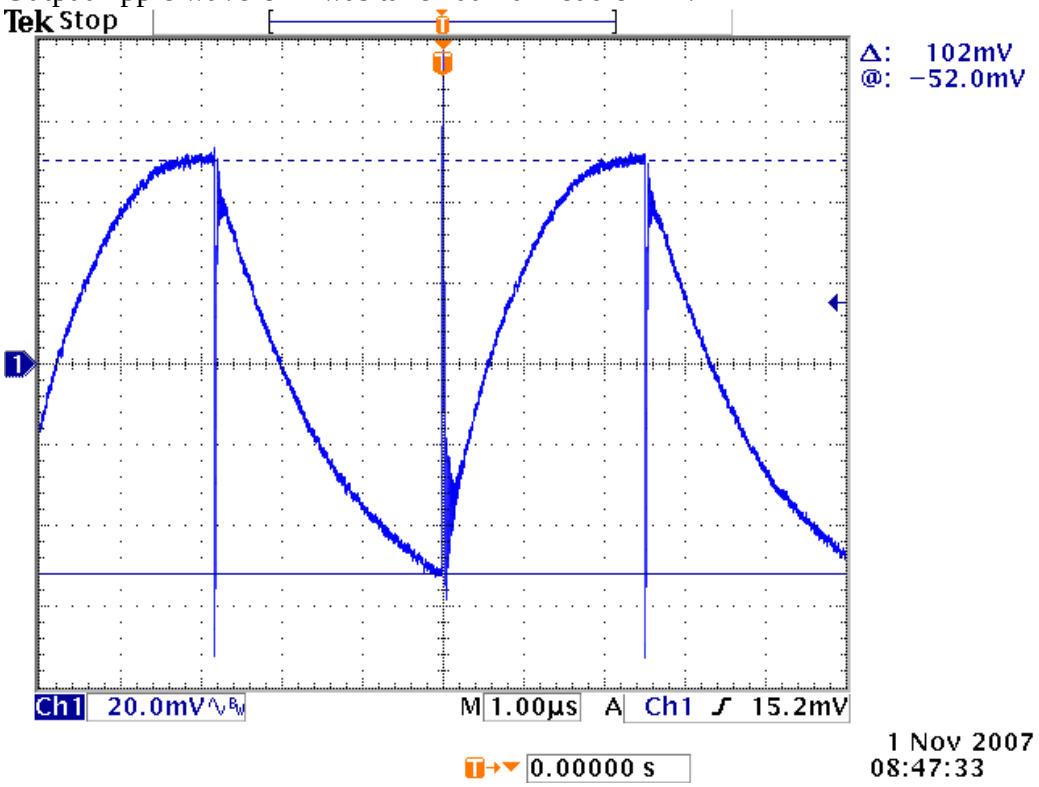


14V in efficiency plot

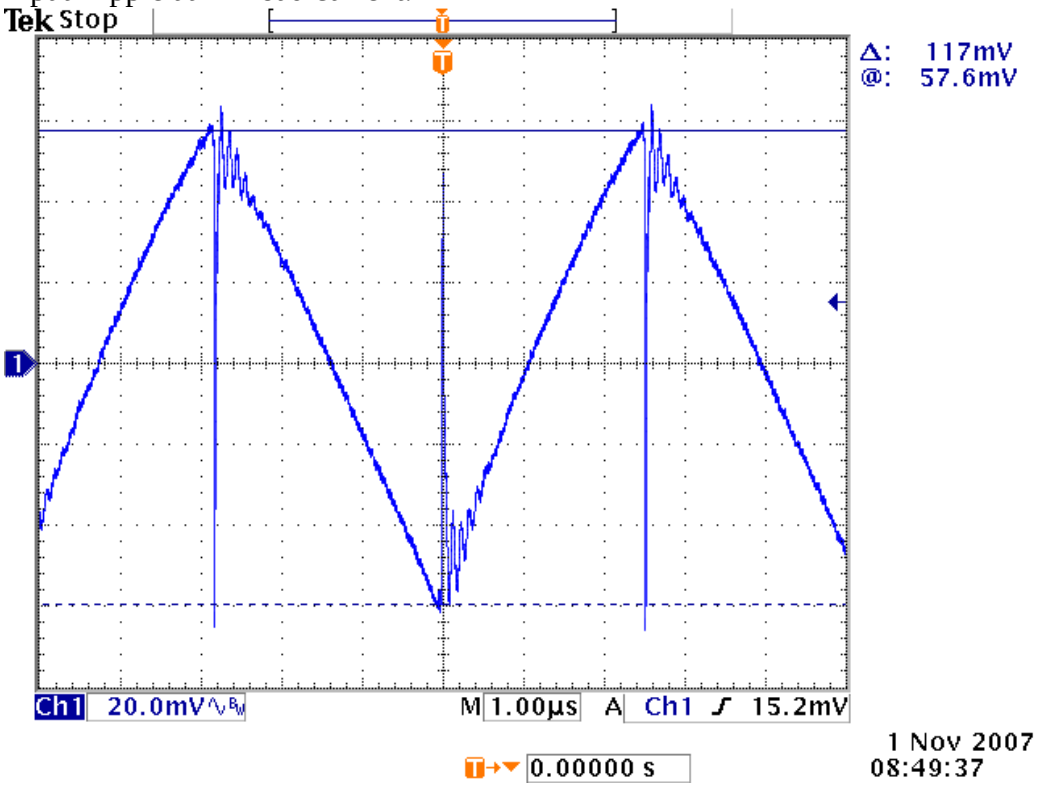


Output Ripple

Output ripple waveform was taken at max load of 1A.

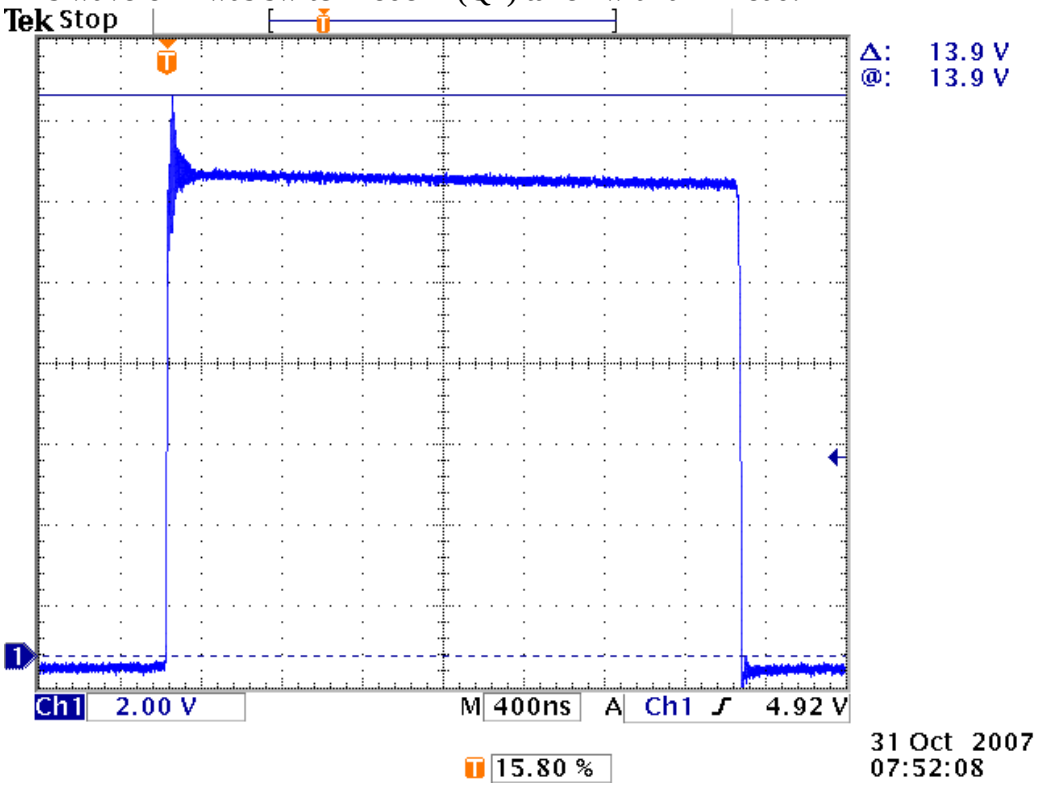


Input Ripple at 1A load current.

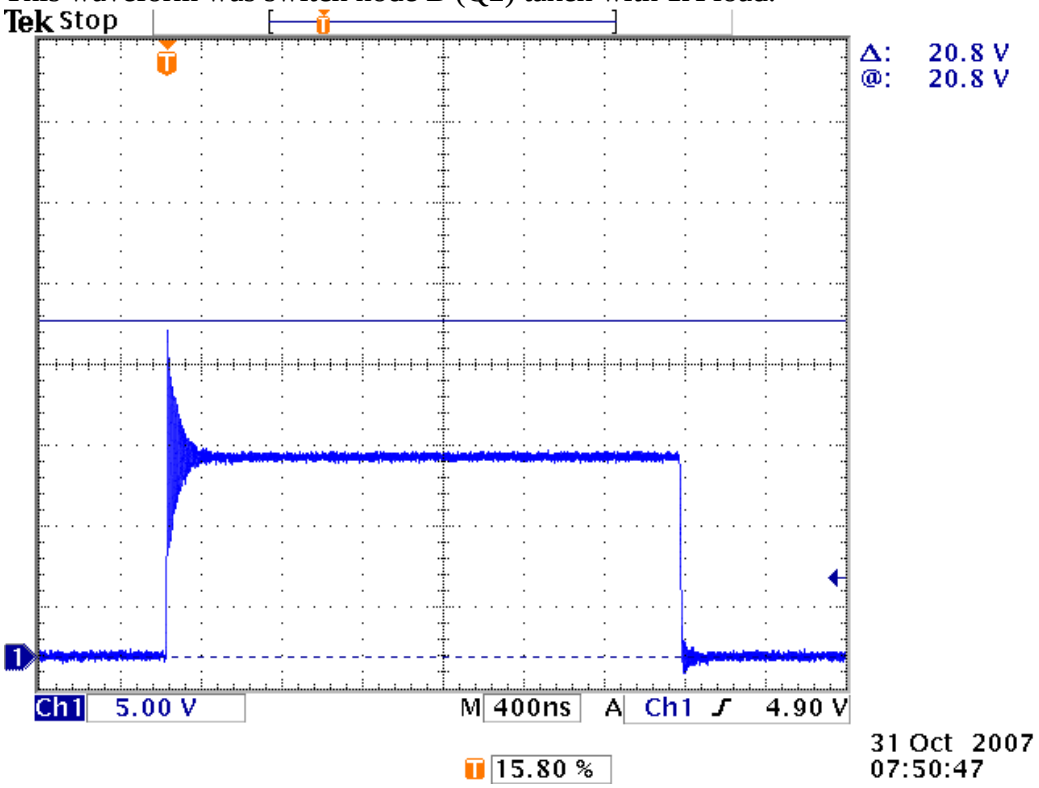


Switching waveforms

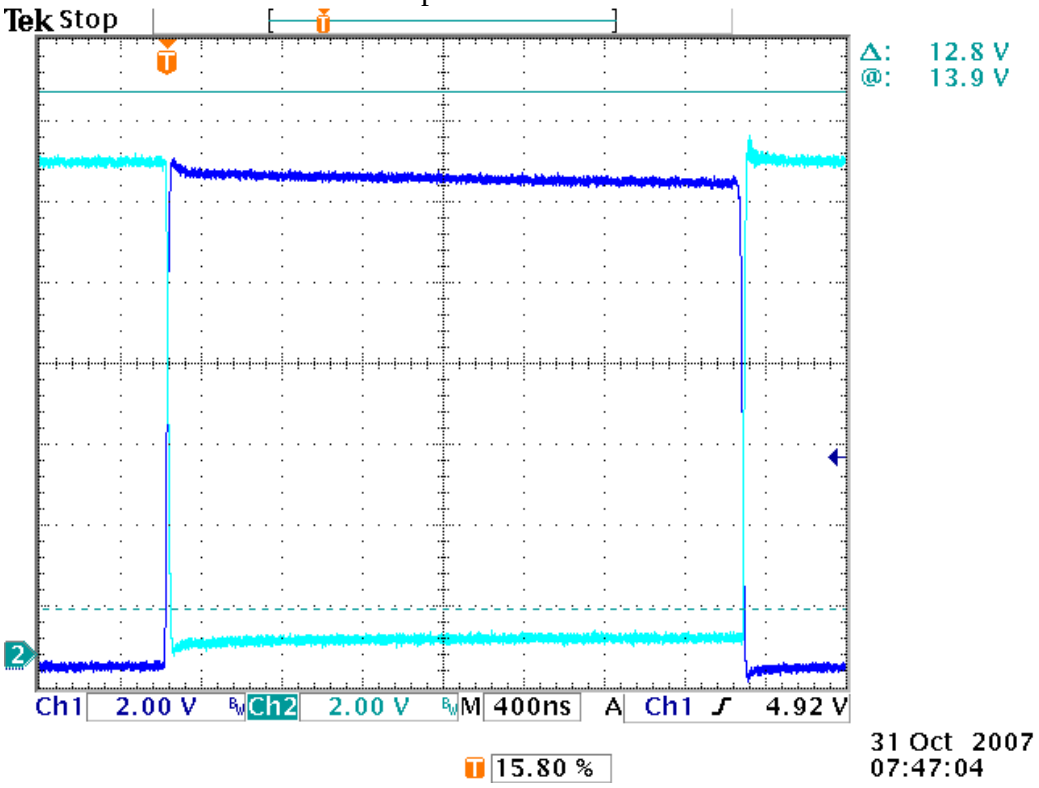
This waveform was switch node A (Q1) taken with a 1A load.



This waveform was switch node B (Q2) taken with 1A load.

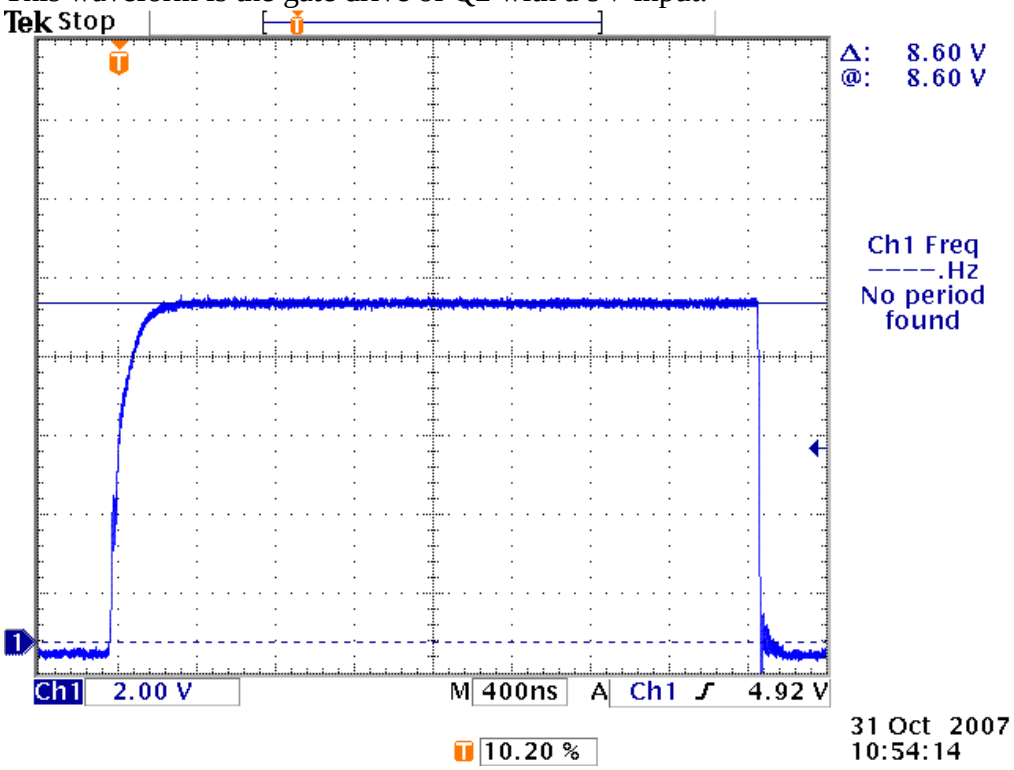


This waveform shows the overlap of both switch nodes.

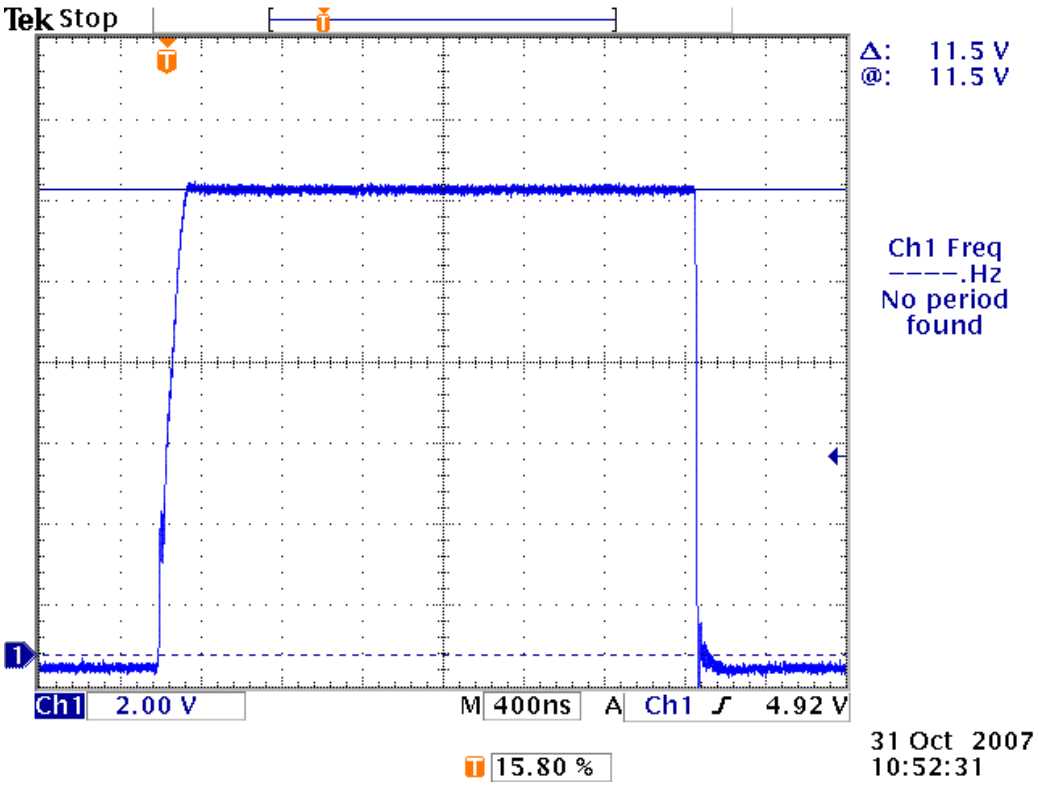


Gate drive waveforms

This waveform is the gate drive of Q2 with a 9V input.

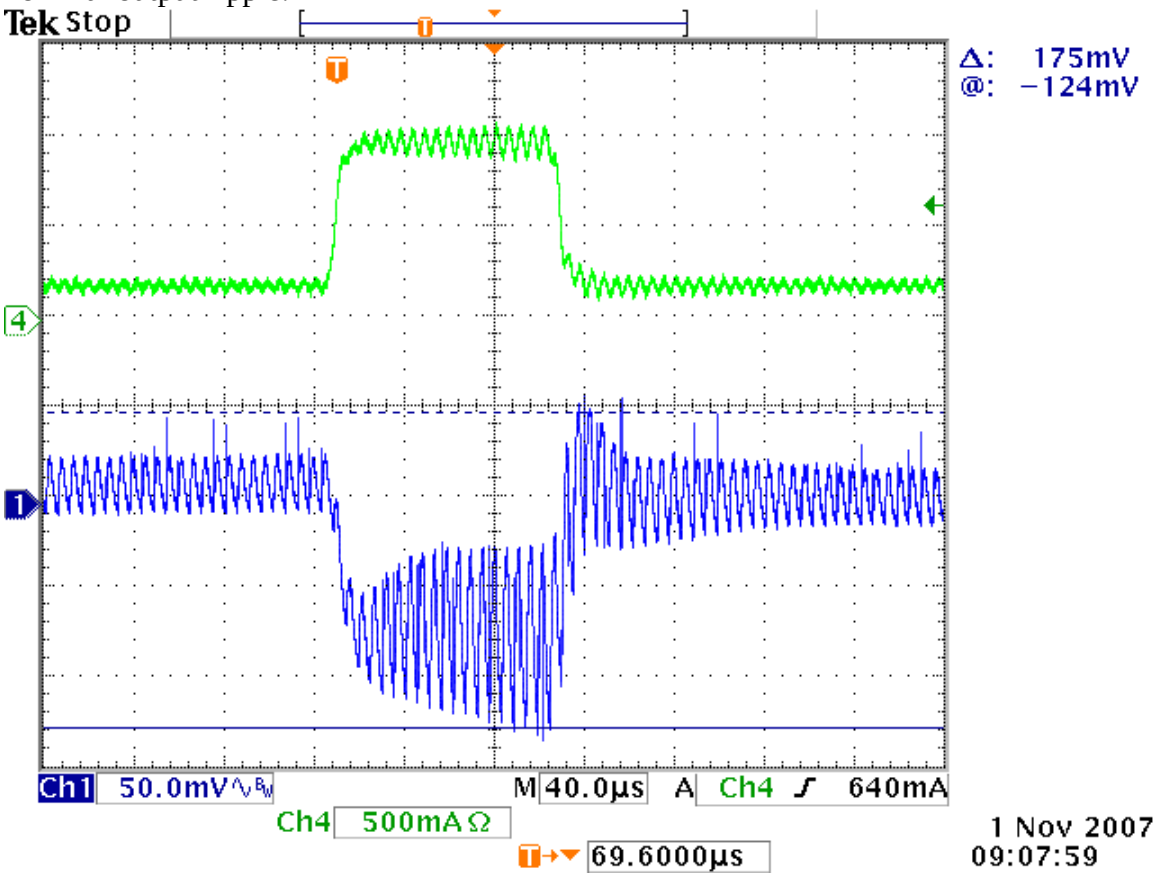


This waveform is the gate drive for Q2 with a 14V input. The gate drive is clamped at 12V max.



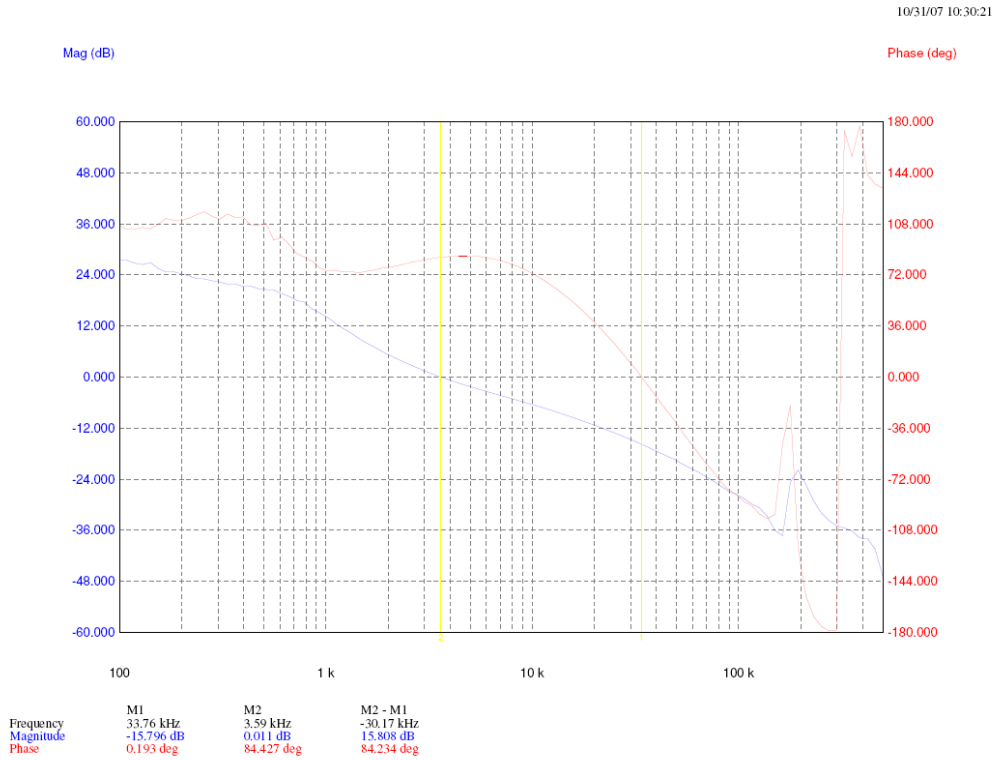
Transient response plot

The following plot was taken with a chroma electronic load stepping from 200mA to 1A at 160mA/uS rate. The output deviation caused by the transient adds very little to the nominal output ripple.

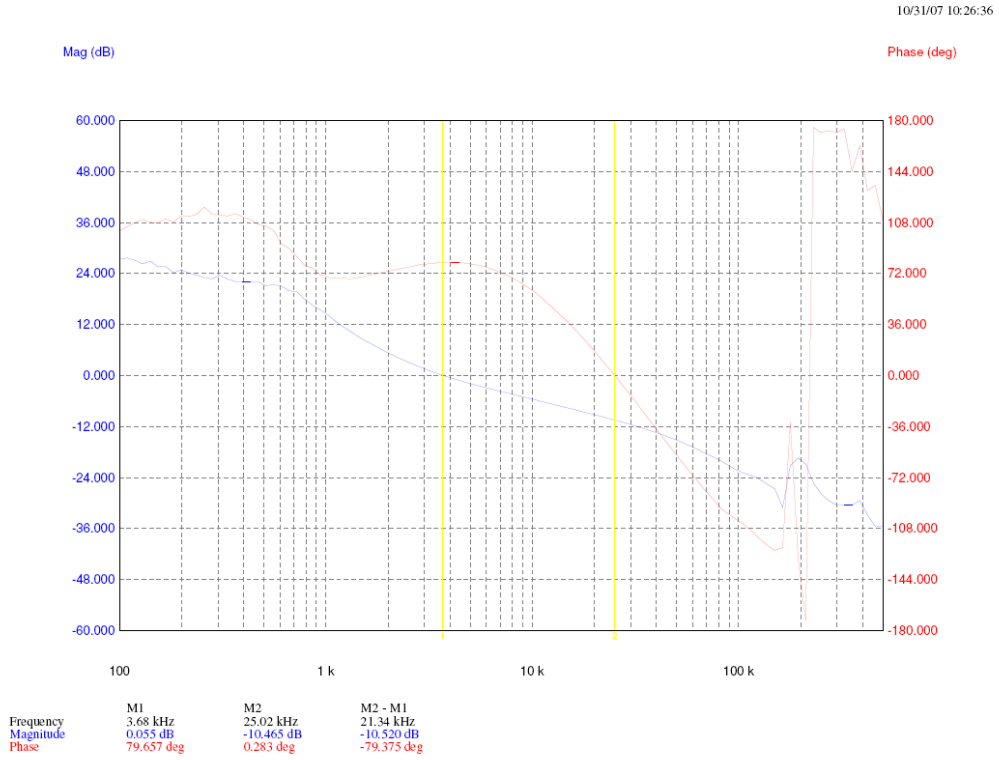


Frequency Response plots

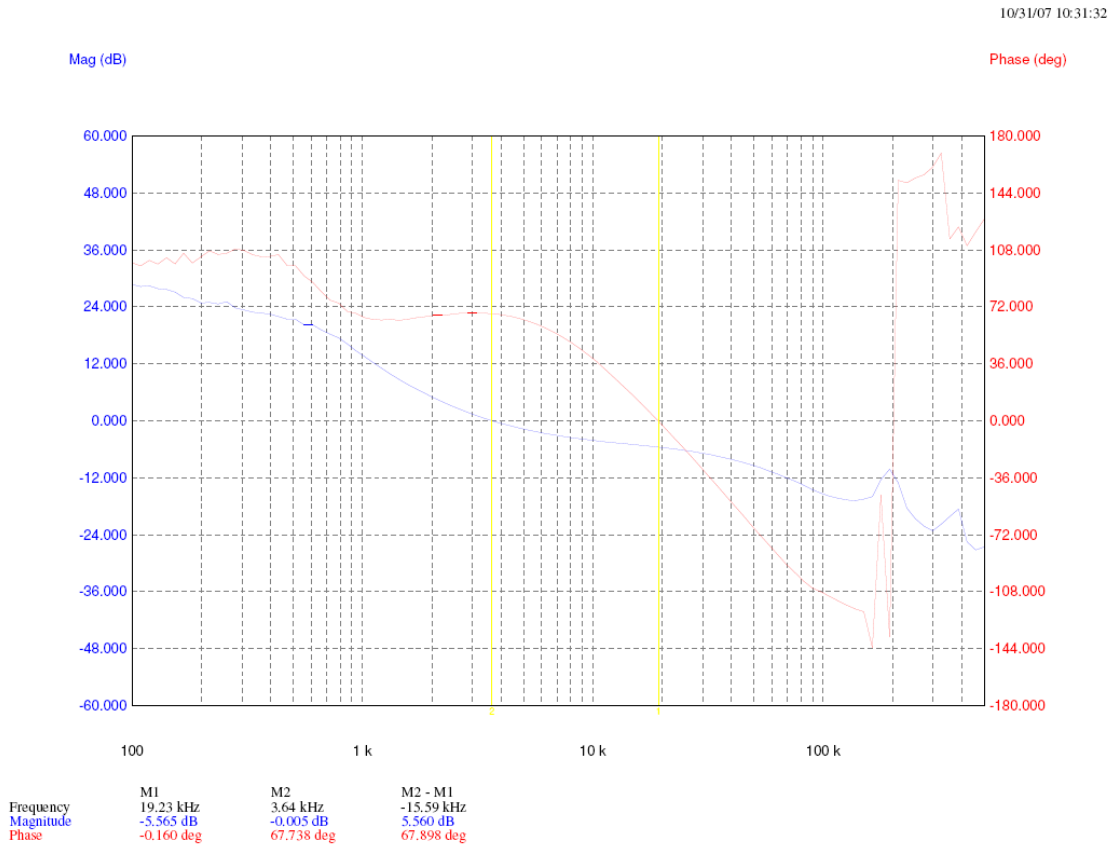
12Vin 0.5A load loop plot (84deg, 15dB, 3.6KHz BW):



12Vin 1A load loop plot (79deg, 10dB, 3.7KHz BW):



12V in 2A load loop plot (67deg, 5.5dB, 3.6KHz BW):



	M1	M2	M2 - M1
Frequency	19.23 kHz	3.64 kHz	-15.59 kHz
Magnitude	-5.565 dB	-0.005 dB	5.560 dB
Phase	-0.160 deg	67.738 deg	67.898 deg

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