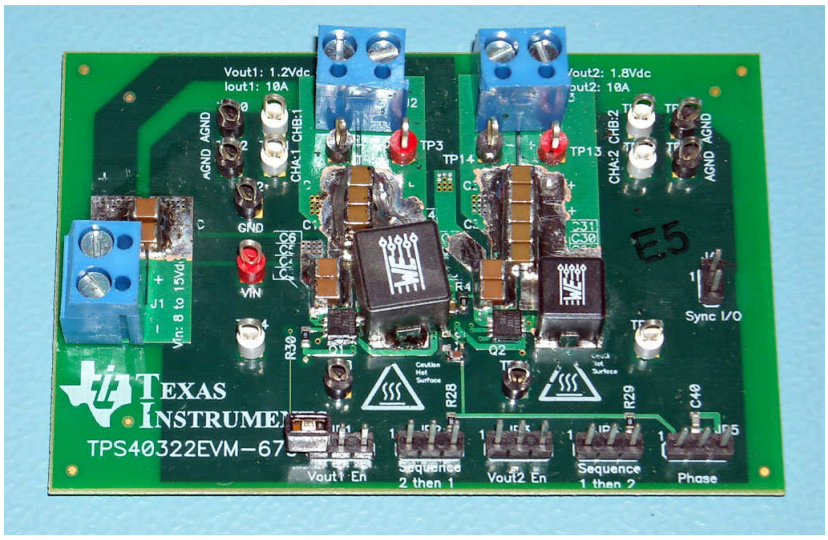
Dual Output Synchronous Buck – 5.0V @ 7.0A / 3.3V @ 4.0A

- Input 12.0V DC
- Output 5.0V @ 7.0A (VOUT1) & 3.3V @ 4.0A (VOUT2)
- Controller TPS40322 & CSD86330Q3D PowerBlocks
- Free-running switching frequency of 500 kHz
- Modified EVM TPS40322EVM-679



1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 12V, with no load on the 5.0V and 3.3V output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **5.0V Output voltage**
2V/div, 5ms/div

Channel C3: **3.3V Output voltage**
2V/div, 5ms/div

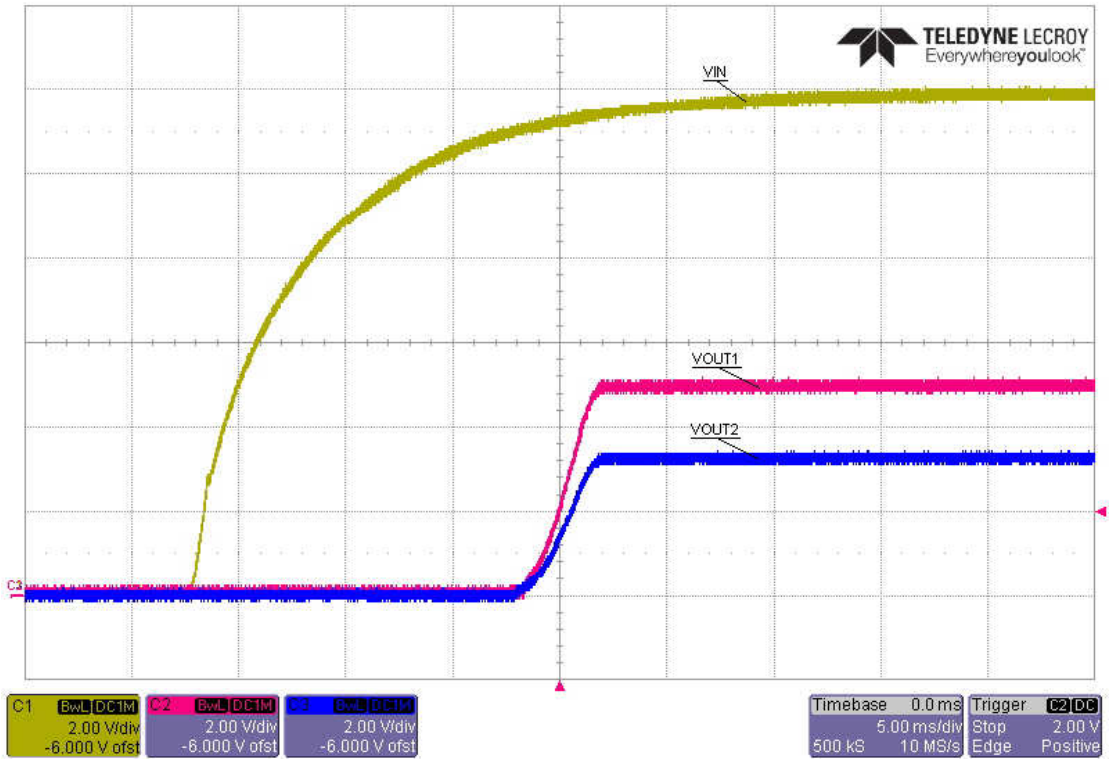


Figure 1

2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 12.0V with 7.0A load on the 5.0V output and 4.0A load on the 3.3V output.

Channel C1: **12.0V Input voltage**
2V/div, 5ms/div

Channel C2: **5.0V Output voltage**
2V/div, 5ms/div

Channel C3: **3.3V Output voltage**
2V/div, 5ms/div

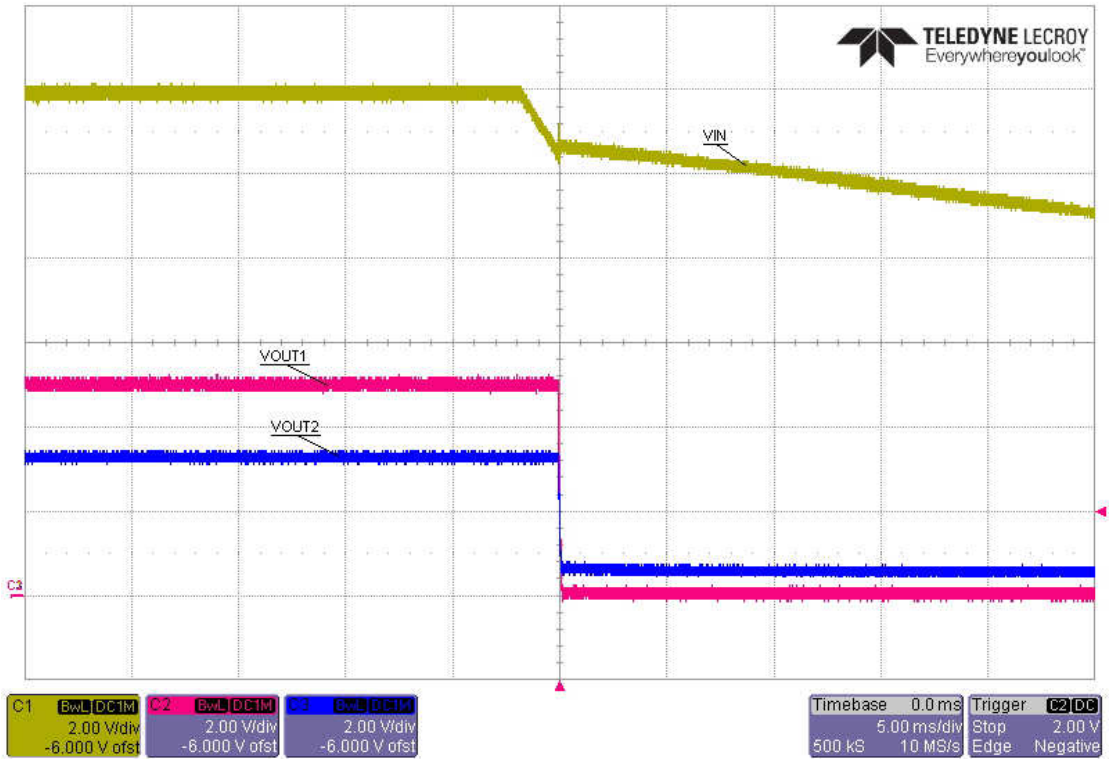


Figure 2

3 Efficiency

The efficiency and load regulation are shown in Figure 3 and Figure 4.

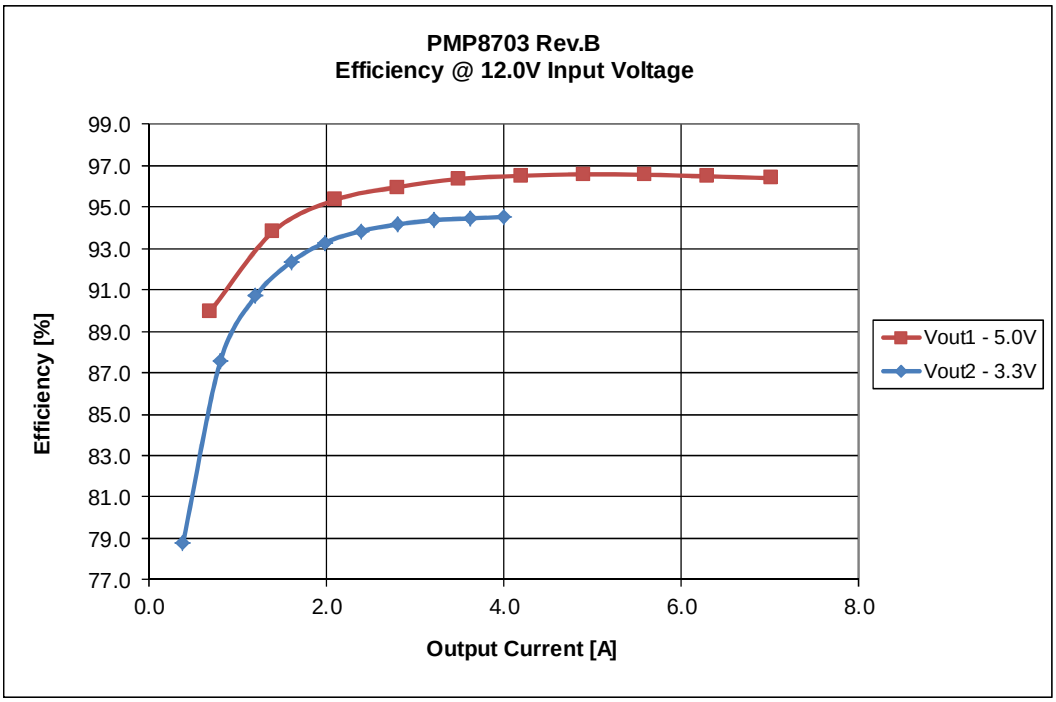


Figure 3

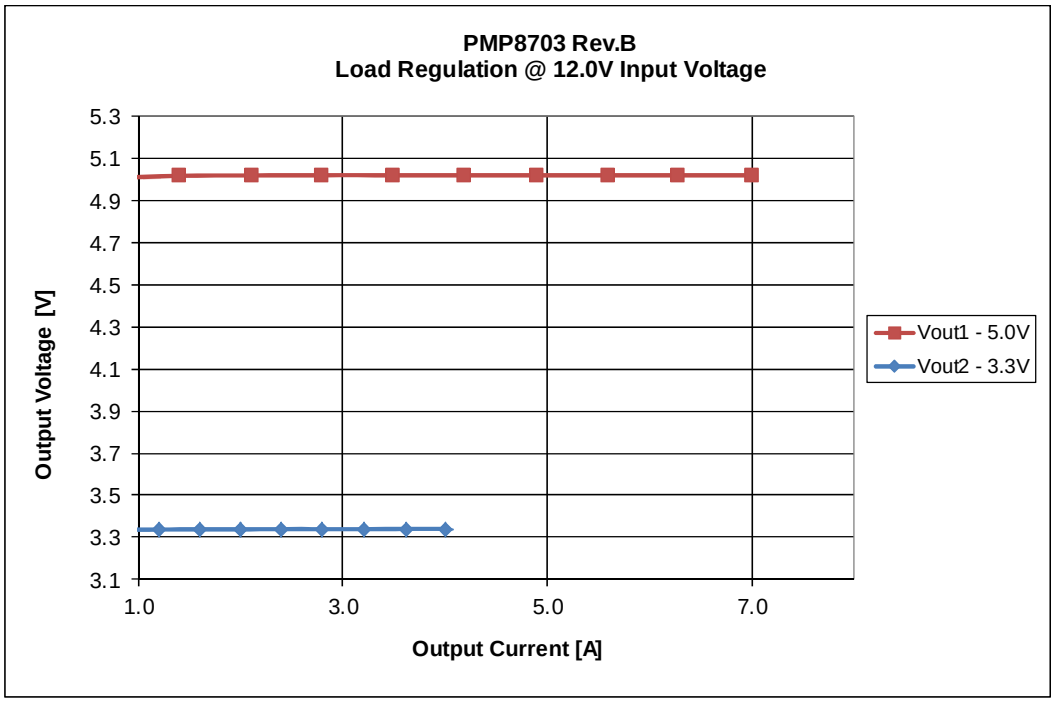


Figure 4

4 Load step

The response to a load step and a load dump are shown in Figure 5 and Figure 6.

Channel C2: **5.0V output**, -89mV undershoot, 91mV overshoot (1.8%)
50mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 3.5A to 7.0A and vice versa
5A/div, 1ms/div

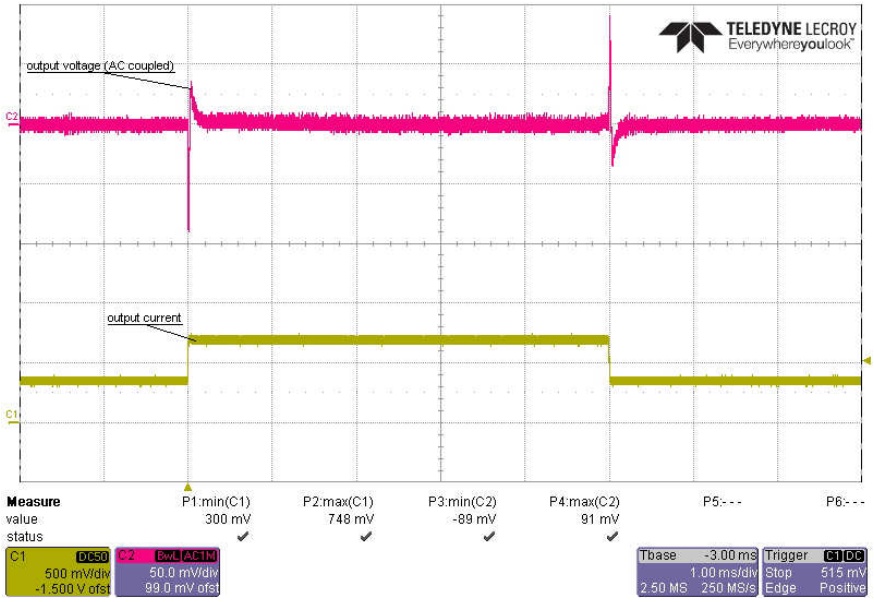


Figure 5

Channel C2: **3.3V output**, -62mV undershoot, 61mV overshoot (1.9%)
50mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 2.0A to 4.0A and vice versa
2A/div, 1ms/div

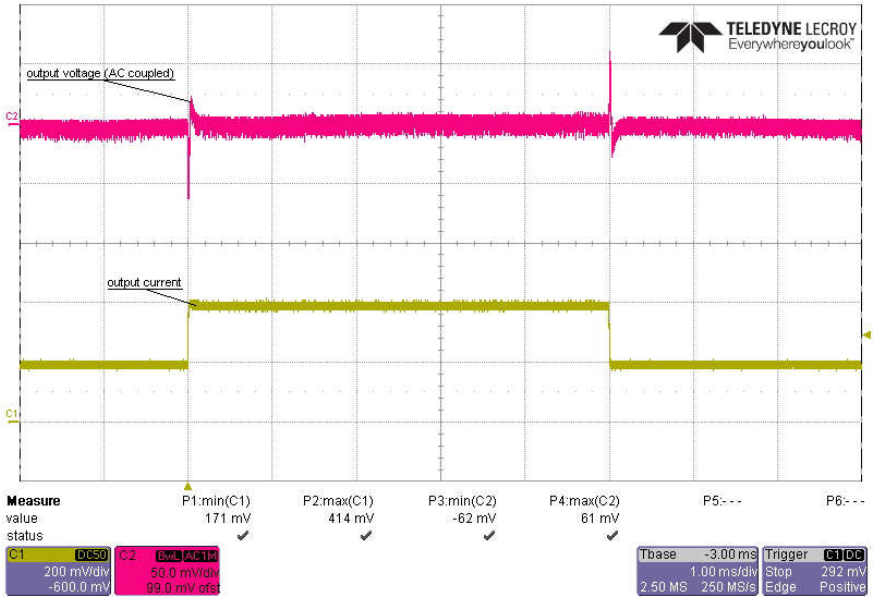


Figure 6

5 Frequency response

Figure 7 and Figure 8 show the loop response at 12.0V input voltage.

Vout1 – 5.0V

0.5A load	65 deg phase margin @ 40.1 kHz bandwidth -18 dB gain margin
3.5A load	57 deg phase margin @ 42.0 kHz bandwidth -16 dB gain margin
7.0A load	58 deg phase margin @ 41.1 kHz bandwidth -14 dB gain margin

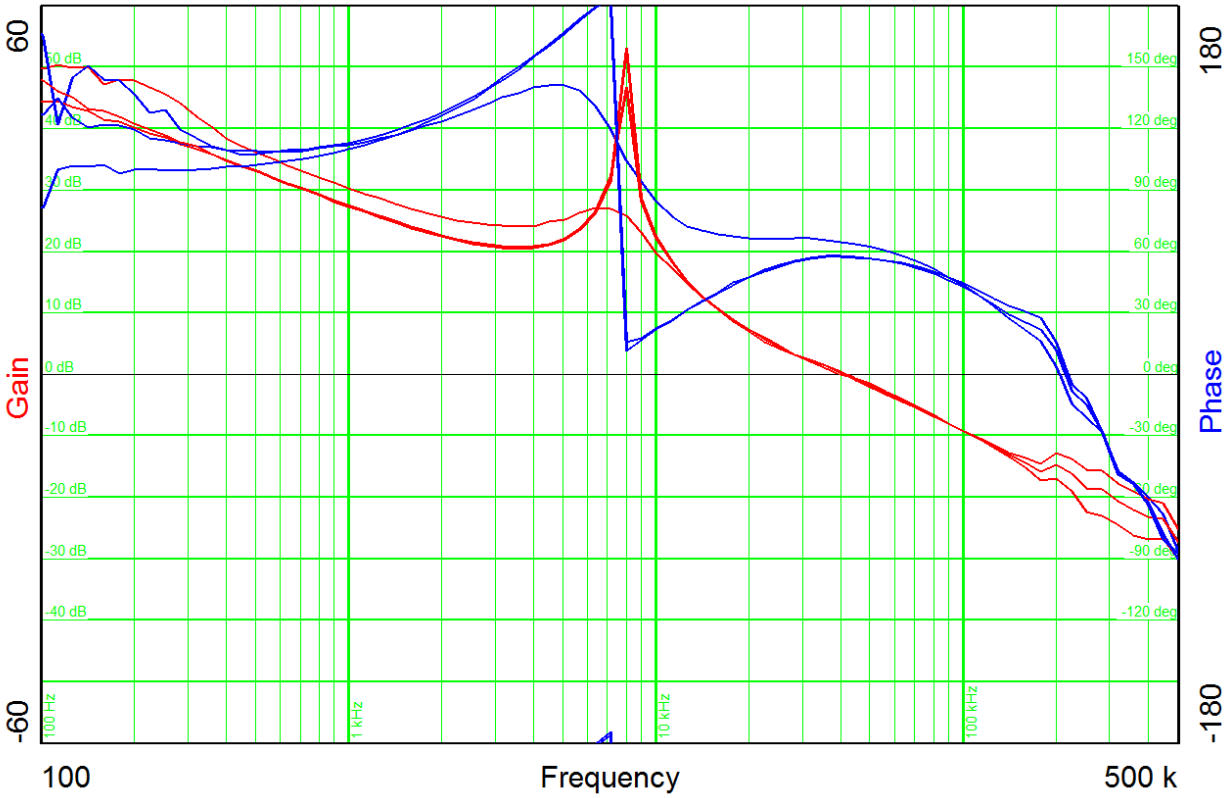


Figure 7

Vout2 – 3.3V

0.5A load	57 deg phase margin @ 37.0 kHz bandwidth -18 dB gain margin
2.0A load	56 deg phase margin @ 36.7 kHz bandwidth -18 dB gain margin
4.0A load	56 deg phase margin @ 36.8 kHz bandwidth -19 dB gain margin

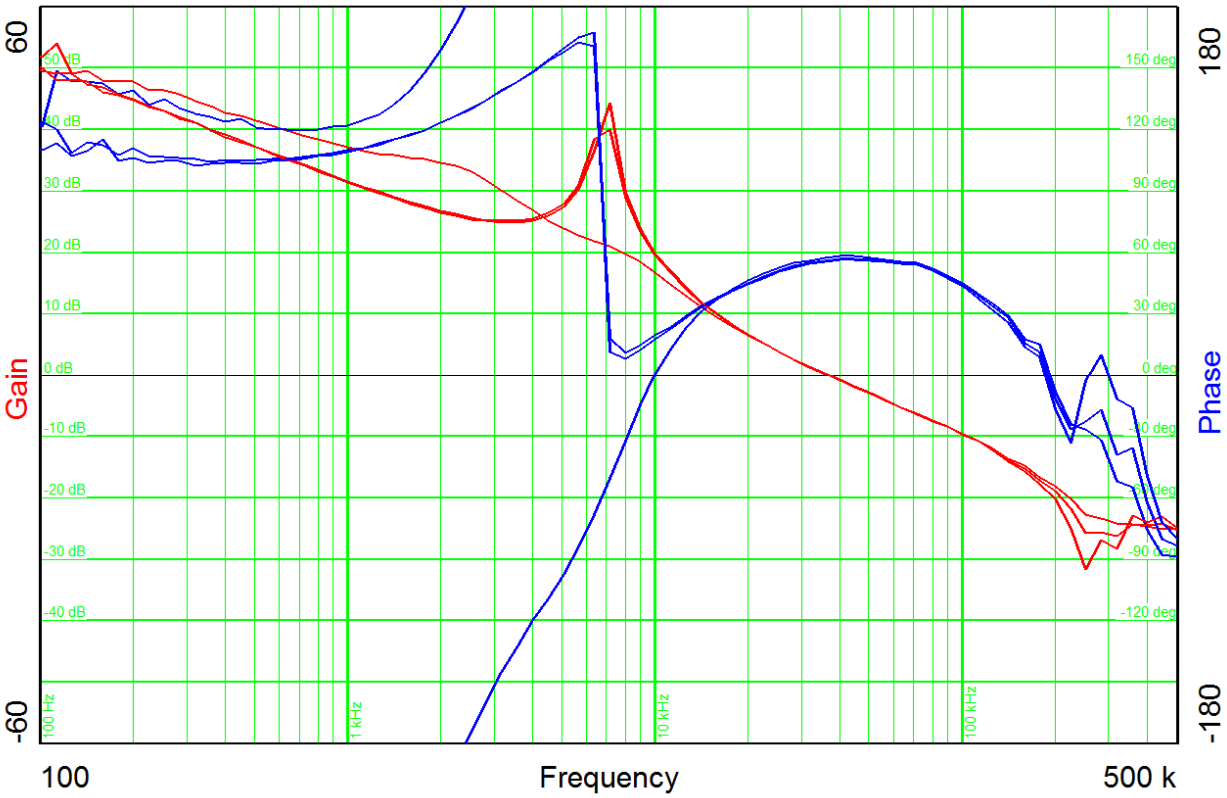


Figure 8

6 Switching Node

The drain-source voltage on the switching node is shown in Figure 9 and Figure 10.

Channel C2: **Drain-source voltage, Vout 1 / 5.0V @ 7.0A,** -1.2V min. / 19.8V max. 5V/div, 1us/div

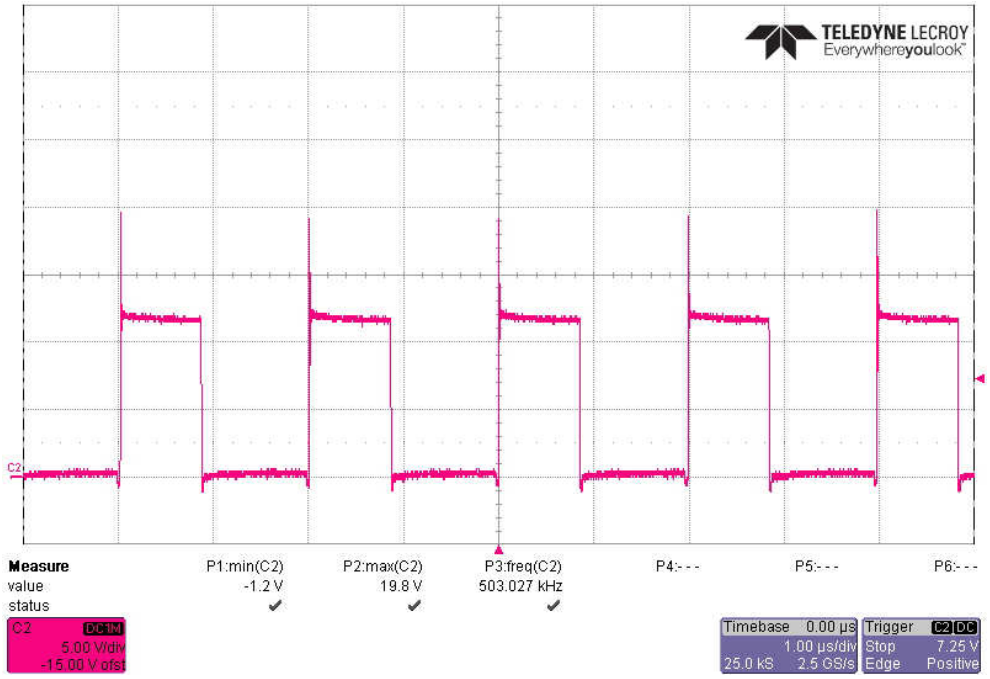


Figure 9

Channel C2: **Drain-source voltage, Vout 2 / 3.3V @ 4.0A,** -0.4V min. / 14.5V max. 5V/div, 1us/div

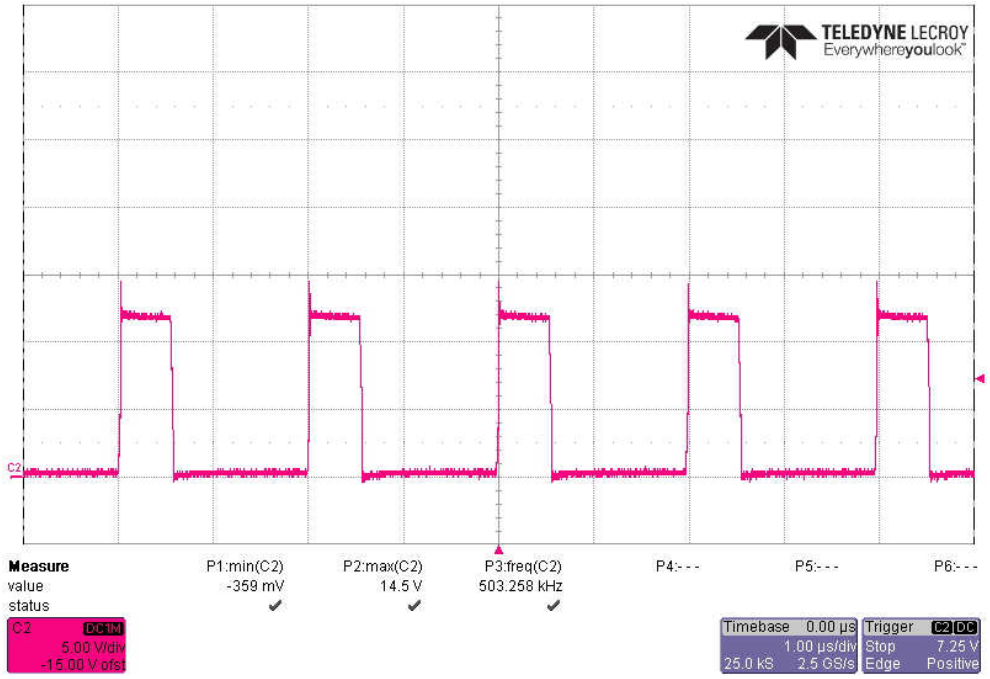


Figure 10

7 Output Ripple

The output ripple at 12.0V input voltage is shown in Figure 11 and Figure 12.

Channel C2: **Output ripple, Vout 1 / 5.0V @ 7.0A,** 9mV peak-peak.
20mV/div, 2us/div, AC coupled

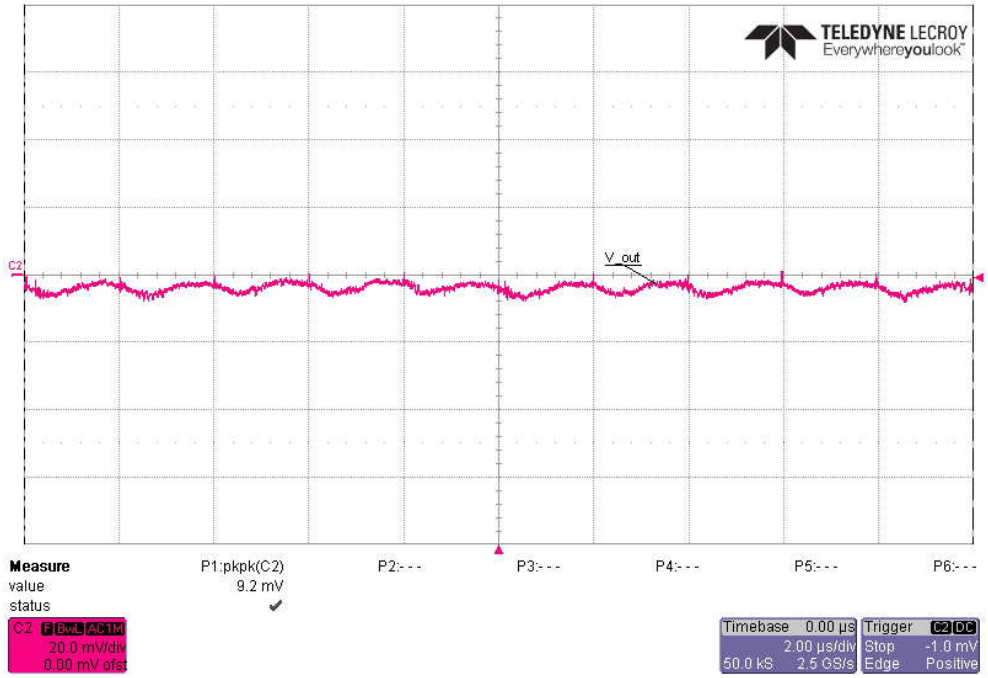


Figure 11

Channel C2: **Output ripple, Vout 2 / 3.3V @ 4.0A,** 12mV peak-peak
20mV/div, 2us/div, AC coupled

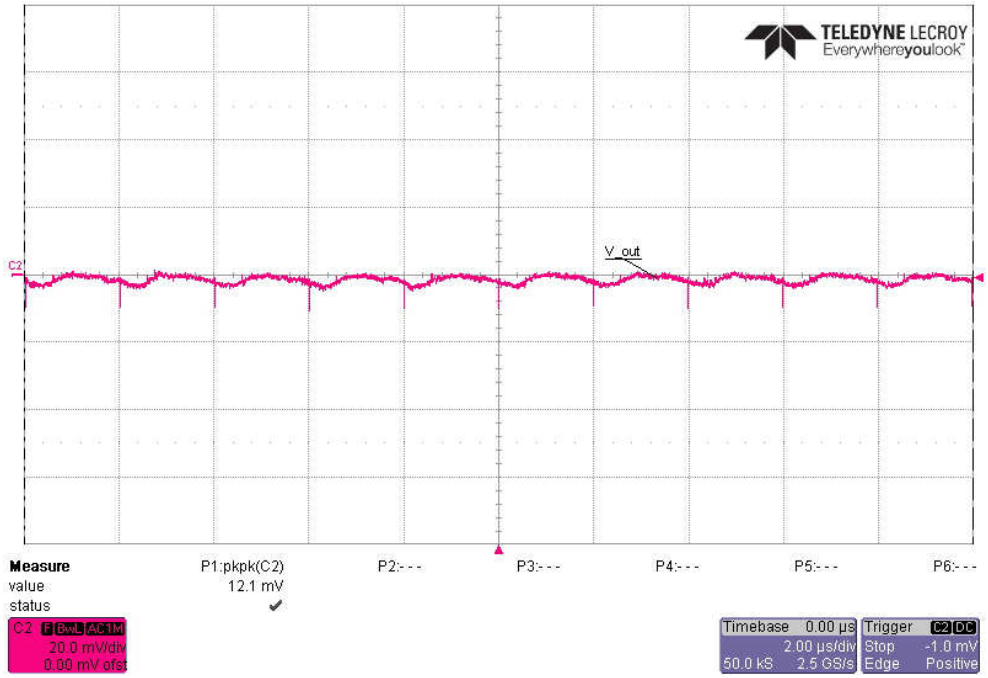


Figure 12

8 Thermal measurement

The thermal image (Figure 13) shows the circuit at an ambient temperature of 21 °C with an input voltage of 12.0V and full load on both outputs (5.0V @ 7.0A, 3.3V @ 4.0A).

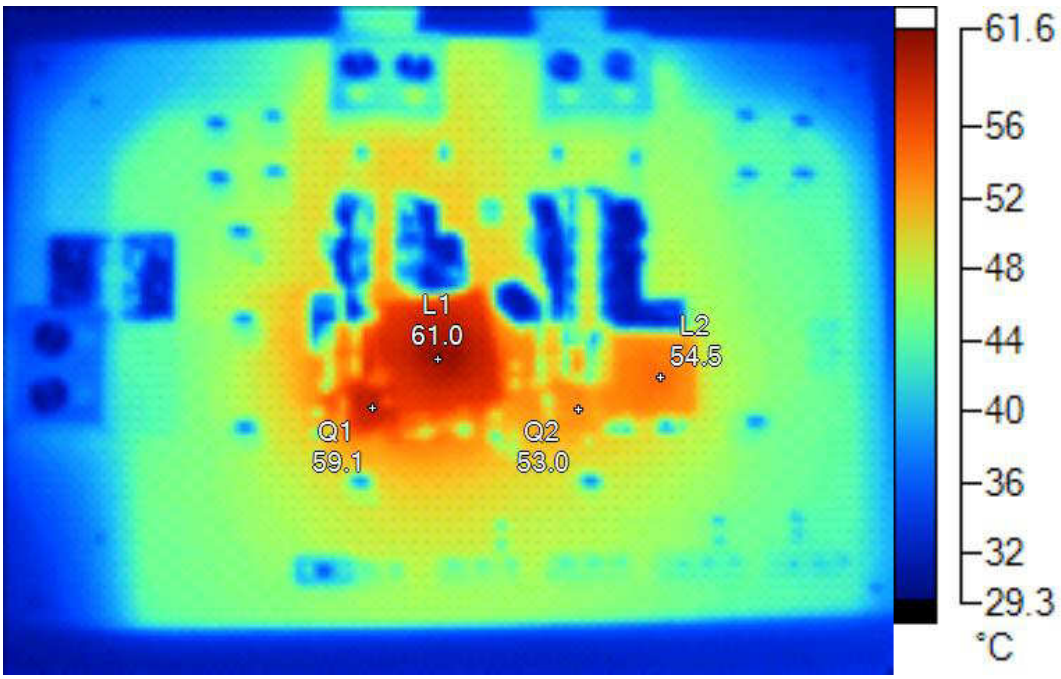


Figure 13

Markers

Label	Temperature	Emissivity	Background
L1	61.0 °C	0.95	21.0 °C
L2	54.5 °C	0.95	21.0 °C
Q1	59.1 °C	0.95	21.0 °C
Q2	53.0 °C	0.95	21.0 °C

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