

Using the TPS53667EVM-769, 6-Phase, D-CAP+ Step-Down, DC-DC Analog with PMBus™ Interface

This User Guide describes the evaluation module (EVM) for the TPS53667 analog power controller, a driverless D-CAP+™ buck controller, which manages six 30-A phases of the CSD95490, a NexFet™ Smart Synchronous Buck Power Stage. In addition, this document provides instructions for accessing the controller's non-volatile memory (NVM) with the integrated PMBus™ interface to allow access to additional configuration, monitoring and control functions/options.

Contents

1	Description	1
2	Typical Applications	2
	2.1 Features	2
3	Electrical Performance Specifications	2
4	Schematic	3
5	Test Setup	6
	5.1 Test and Configuration Software	6
	5.2 Test Equipment	6
	5.3 Recommended Test Setup	7
	5.4 USB Interface Adapter and Cable	8
	5.5 List of Test Points and Connectors	9
6	EVM Configuration Using the Fusion GUI	11
	6.1 Configuration Procedure	11
7	Test Procedure	11
	7.1 Line/Load Regulation and Efficiency Measurement Procedure	11
	7.2 Control Loop Gain and Phase Measurement Procedure	12
	7.3 Efficiency	13
	7.4 Equipment Turn-on and Shutdown	14
8	Performance Data and Typical Characteristic Curves	15
9	EVM Assembly Drawing and PCB Layout	17
10	List of Materials	19
11	Fusion GUI	22

1 Description

The TPS53667EVM-769 implements a typical application for a low-voltage, high current single output power converter, operating from a nominal 12-V input rail to produce a 1.0-V output rail at up to 180 A of load current. The EVM includes test points for evaluating the performance of the TPS53667 controller and CSD95490 power stages.

For the ease of evaluation, the EVM is supplied using the pin-strapped configuration mode and requires only two (12-V and 5-V) input supplies and an output load to get started with testing. With the addition of the Fusion Digital Power™ Designer software download, the EVM's PMBus™ interface allows access to the controller NVM for evaluation of additional configuration, control and monitoring possibilities. Refer to the TPS53667 datasheet ([SLUSC40](#)) for complete information on configuring multi-phase operation with this controller.

2 Typical Applications

- ASIC power in communications equipment
- High density power solutions
- Server power
- Smart power systems

2.1 Features

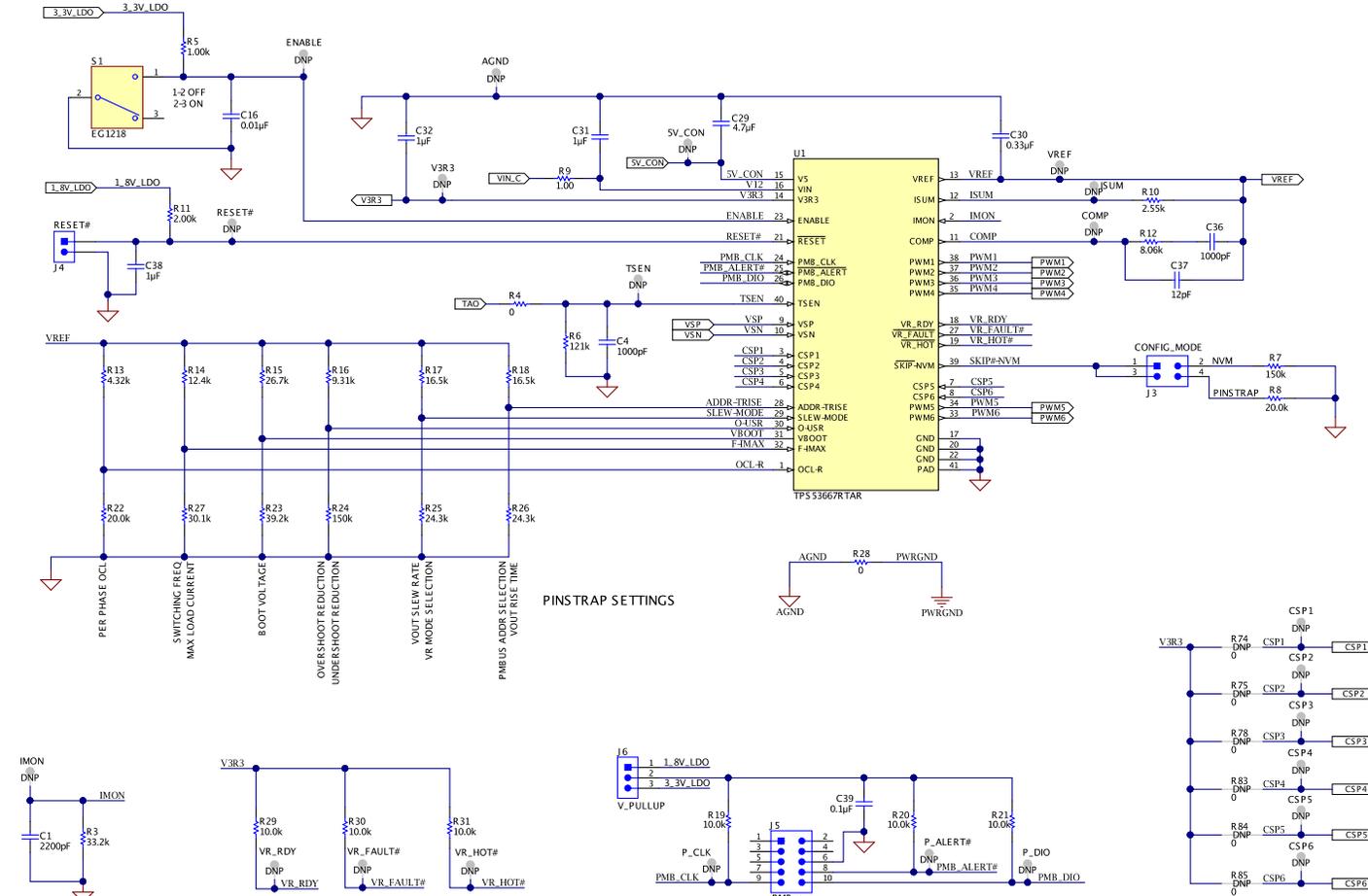
- Regulated 1.0-V output up to 180-A DC steady state output current
- Programmable settings available through PMBus™ interface
 - Output voltage trim
 - Output voltage margin levels (High / Low) within a maximum range
 - UVLO protection threshold
 - Soft-start slew-rate
 - Device enable and disable
 - Overcurrent warning and fault limits
 - SW frequency
 - BOOT voltage
- Convenient test points for probing critical waveforms

3 Electrical Performance Specifications

Table 1. TPS53667EVM-769 Electrical Performance Specifications

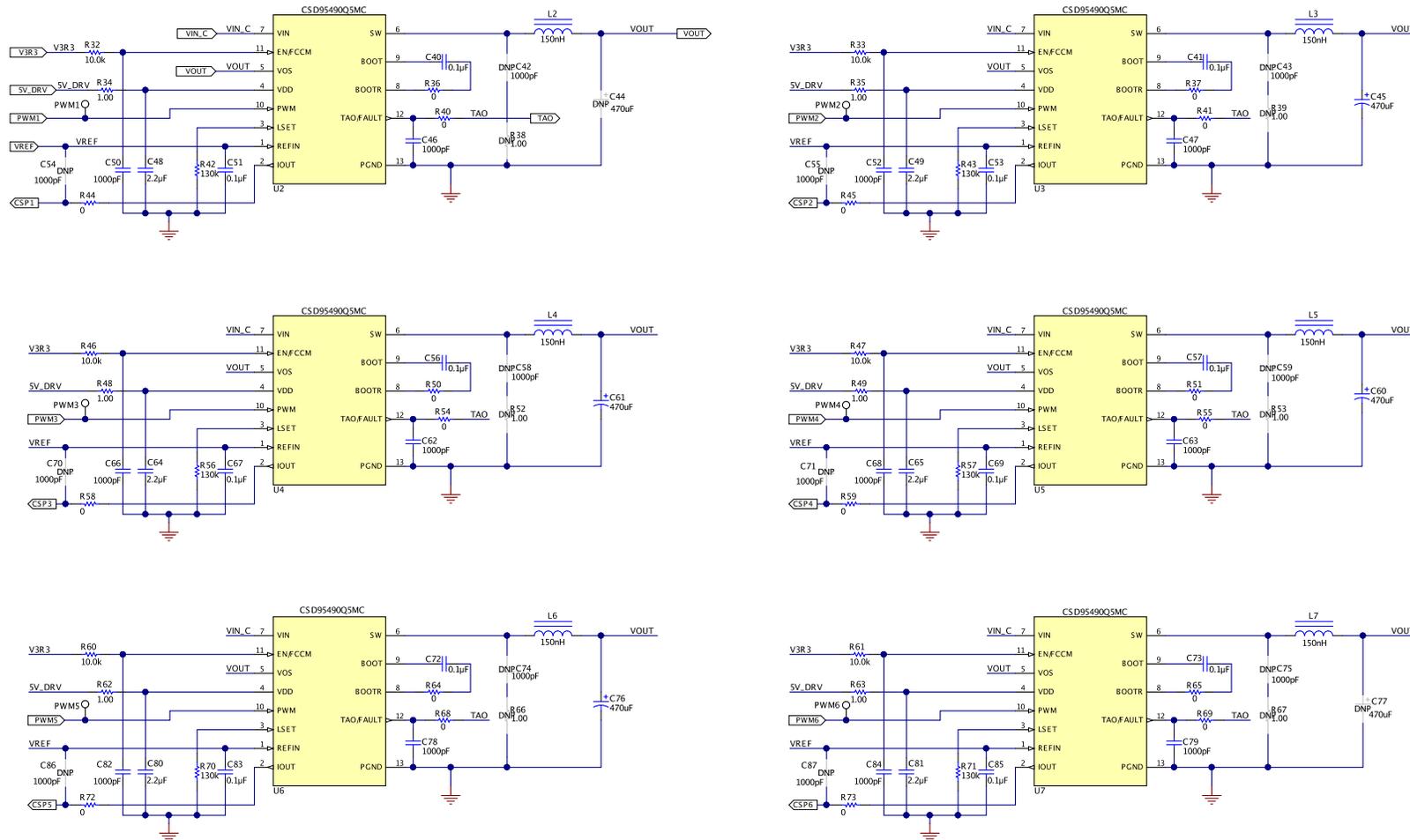
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
V _{IN}	Voltage range	8	12	14	V
I _{IN(max)}	Maximum input current	V _{IN} = 8 V, I _{OUT} = 180 A		26	A
	No load input current	V _{IN} = 14 V, I _{OUT} = 0 A		125	mA
OUTPUT CHARACTERISTICS					
V _{OUT}	Output voltage	1.0			V
I _{OUT}	Output load current	0		180	A
	Output voltage line regulation	8 V ≤ V _{IN} ≤ 14 V		0.03%	%
	Output voltage load regulation	0 A ≤ I _{OUT} ≤ 180 A		0.15%	%
V _{RIPPLE}	Output voltage ripple	V _{IN} = 12 V, I _{OUT} = 180 A		3.5	mVpp
	Output overcurrent protection (OCP)	185			A
SYSTEMS CHARACTERISTICS					
f _{SW}	Switching frequency	V _{IN} = 12 V		500	kHz
	Peak efficiency	V _{IN} = 12 V, I _{OUT} = 100 A		92.0	%
	Full-load efficiency	V _{IN} = 12 V, I _{OUT} = 180 A		90.6	%
T _A	Operating temperature	25			°C

4 Schematic



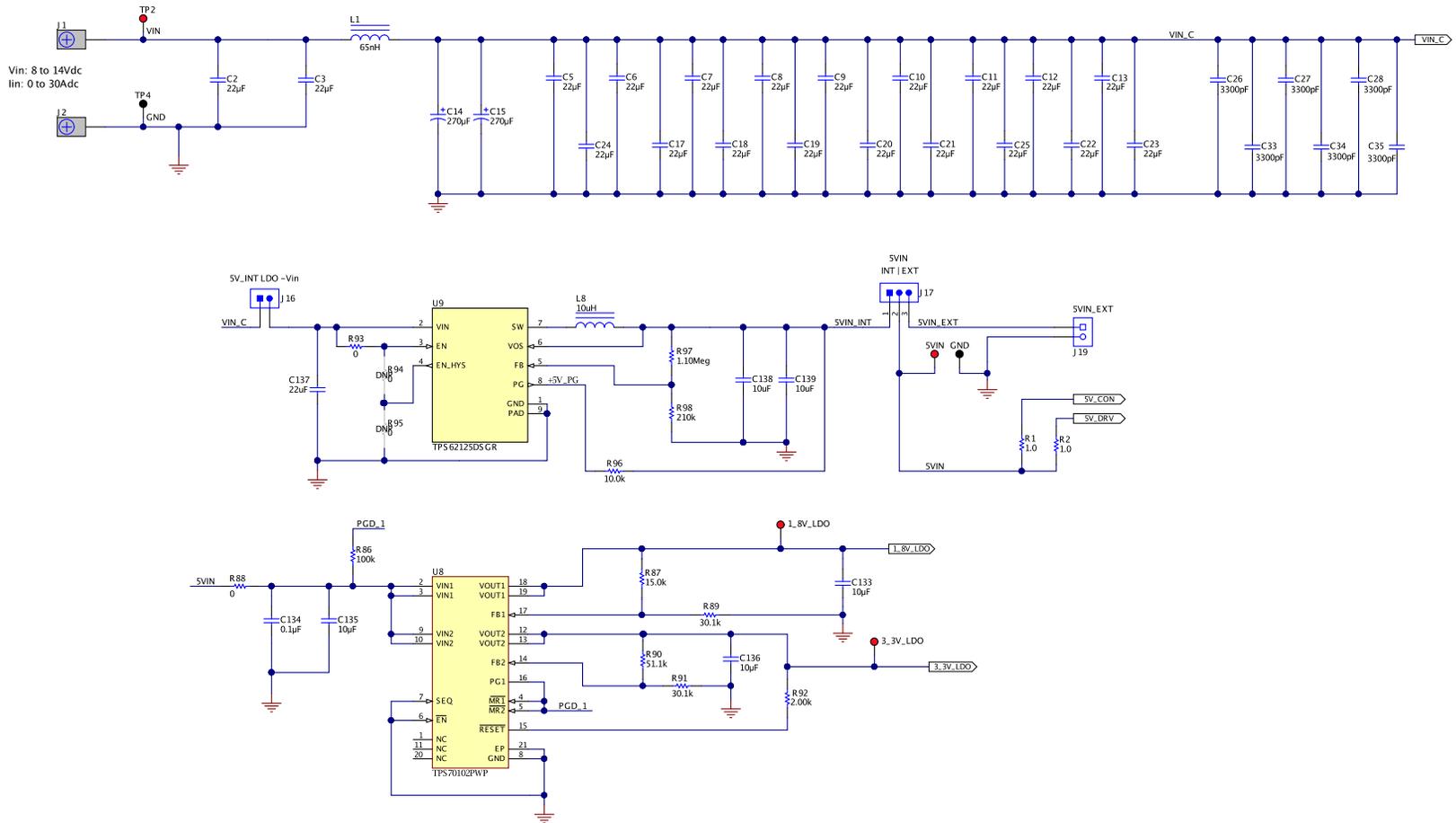
Copyright © 2017, Texas Instruments Incorporated

Figure 1. TPS53667EVM-769 - Controller Schematic



Copyright © 2017, Texas Instruments Incorporated

Figure 2. TPS53667EVM-769 - Power Stages 1 - 6 Schematic



Copyright © 2017, Texas Instruments Incorporated

Figure 3. TPS53667EVM-769 - VIN, 5VIN and AUX Voltages Schematic

5 Test Setup

5.1 Test and Configuration Software

The Texas Instruments Fusion Digital Power Designer software can expand the functionality of the EVM. To download this software, visit the [Digital Power Software](#) page.

5.1.1 Description

The Fusion Digital Power Designer is a graphical user interface (GUI) used to configure, control and monitor the TPS53667 controller on the EVM. The software uses the PMBus™ protocol to communicate with the controller over a serial bus by way of the TI USB-to-GPIO Interface Adapter (see [Figure 5](#)).

5.1.2 TI Fusion Digital Power Designer Features

The software offers these features:

- Turn on or off the power supply output, either through the hardware control line or the PMBus™ Operation command.
- Monitor real-time data. Items such as input voltage, output voltage, output current, temperature, warnings and faults are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as output voltage trim and margin, V_{IN} UVLO, soft-start slew rate, switching frequency, and warning and fault thresholds.

5.2 Test Equipment

5.2.1 Voltage Sources

Two DC input voltage sources are needed (V_{IN} and 5VIN). The V_{IN} input voltage source should be a 0 V to 14 V variable DC source capable of supplying 30 Adc. The 5VIN input voltage source should be a 5 V fixed DC source capable of supplying 1Adc. Connect V_{IN} to J1, J2 and connect 5VIN to J19 as shown in [Figure 4](#).

5.2.2 Multimeters

It is recommended to use two separate multimeters, one meter to measure V_{IN} and the other to measure V_{OUT} .

5.2.3 Output Load

An electronic load is recommended for the test setup as shown in [Figure 4](#). The load should be capable of sinking 180 A at 1 V.

5.2.4 Oscilloscope

Use an oscilloscope to measure output noise and ripple. Use a coaxial cable to measure output ripple across the output ceramic capacitor, C105.

5.2.5 Fan

During prolonged operation at high load, it may be necessary to provide forced air cooling with a small fan aimed at the EVM. Maintain the temperature of the devices on the EVM under 105°C.

5.2.6 USB-to-GPIO Interface Adapter

A communications adapter is required between the EVM and the host computer. This EVM is designed to use the Texas Instruments USB-to-GPIO adapter, see [Figure 5](#). To purchase this adapter visit the TI [usb-to-gpio](#) tool page.

5.2.7 Recommended Wire Gauge

Table 2. Recommended Wire Gauge

Voltage (V)	CONNECT	RECOMMENDED WIRE SIZE	MAXIMUM TOTAL WIRE LENGTH ⁽¹⁾ (FEET)		
			RETURN	INPUT	OUTPUT
12	VIN to J1, GND to J2	2 x AWG #10	2	2	n/a
5	5VIN to J19	2 x AWG #18		2	n/a
1	Load+ to J10, J11 and J12, Load- to J13, J14 and J15	6 x AWG #10		n/a	2

⁽¹⁾ Total length of wire less than 4 feet (2 feet input or output, 2 feet return).

5.3 Recommended Test Setup

Figure 4 shows the recommended test setup, which includes VIN and 5VIN input voltage sources, output load, and USB-to-GPIO adapter.

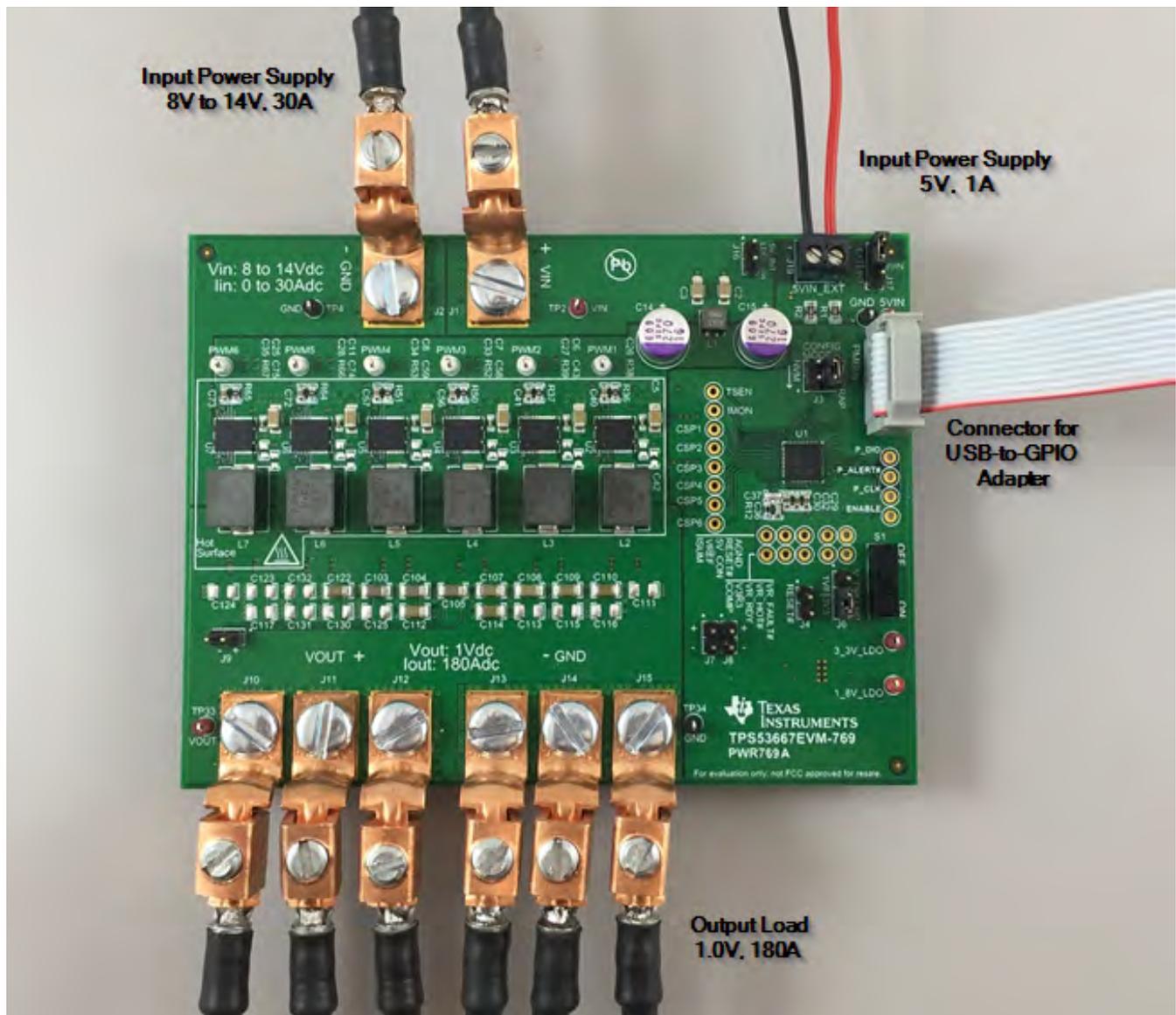


Figure 4. TPS53667EVM-769 Recommended Test Setup

5.4 USB Interface Adapter and Cable

Figure 5 shows the USB interface adapter and cable.

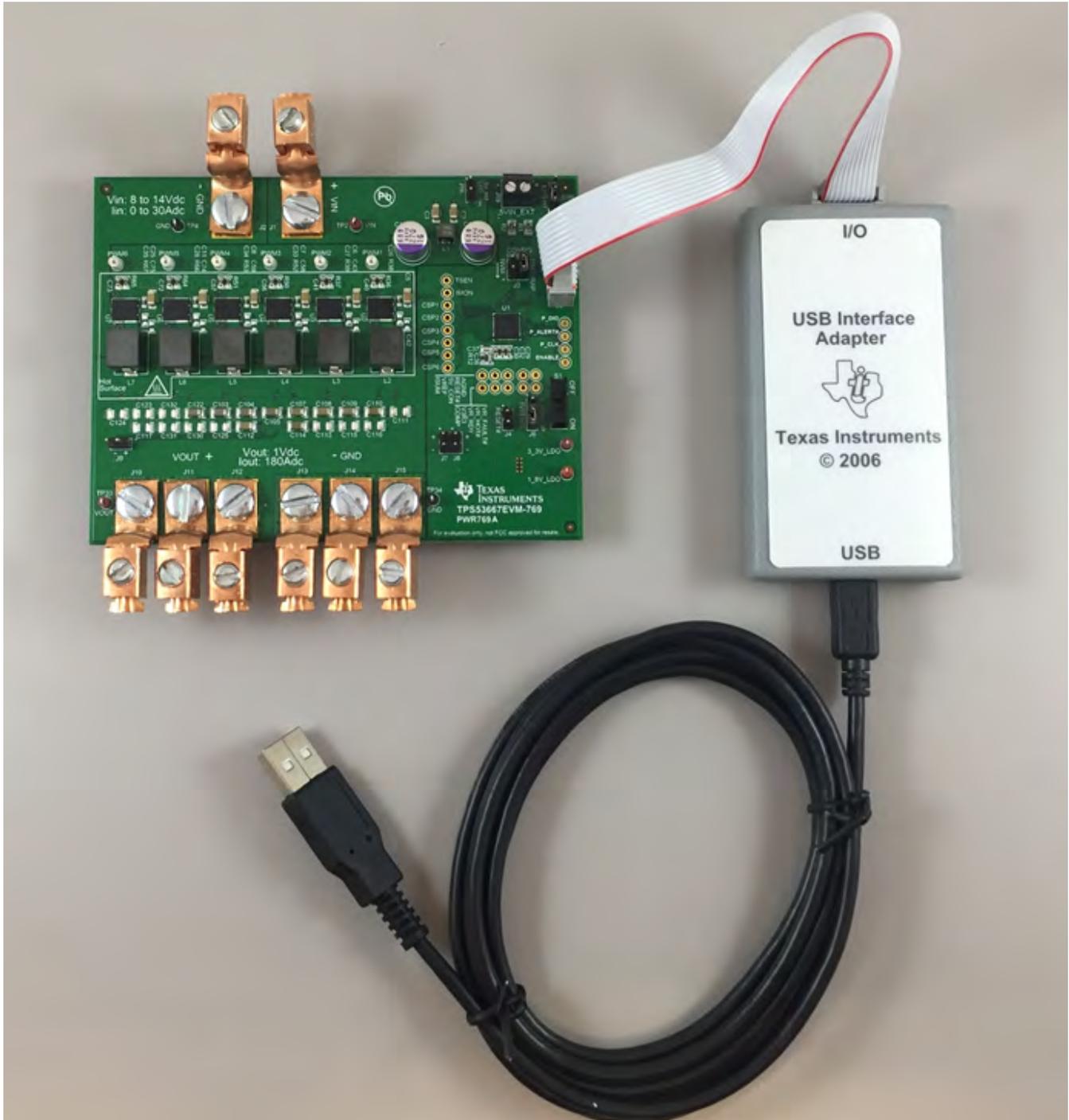


Figure 5. Texas Instruments USB-to-GPIO Adapter and Cable

5.5 List of Test Points and Connectors

Table 3 lists the test point functions.

Table 3. Test Point Functions

NAME	DESCRIPTION
VIN (TP2)	VIN+ measurement point
GND (TP4)	VIN- measurement point
5VIN	5VIN+ measurement point
GND	5VIN- measurement point
VOU (TP33)	V _{OUT+} measurement point
GND (TP34)	V _{OUT-} measurement point
P_DIO	PMBus digital I/O signal
P_ALERT#	PMBus alert signal
P_CLK	PMBus clock signal
ENABLE	ENABLE signal
AGND	Analog Ground
RESET#	Resets Output Voltage to VBOOT level if pin is held low for more than 1000ns
5V_CON	5-V controller input power measurement point
VREF	Internal reference voltage measurement point
ISUM	Voltage droop summing measurement point
VR_FAULT#	VR Fault Indicator
VR_HOT#	Thermal Flag indicator
VR_RDY	Power Good Indicator
V3R3	Internal 3.3-V LDO output measurement point
COMP	Error Amplifier output measurement point
PWM1	PWM signal of Phase 1
PWM2	PWM signal of Phase 2
PWM3	PWM signal of Phase 3
PWM4	PWM signal of Phase 4
PWM5	PWM signal of Phase 5
PWM6	PWM signal of Phase 6
TSEN	Power Stages Thermal measurement point / Power Stages Fault indicator
IMON	Output Current Monitor measurement point
CSP1	Current sense signal of Phase 1
CSP2	Current sense signal of Phase 2
CSP3	Current sense signal of Phase 3
CSP4	Current sense signal of Phase 4
CSP5	Current sense signal of Phase 5
CSP6	Current sense signal of Phase 6
1_8V_LDO	1.8-V external LDO output measurement point
3_3V_LDO	3.3-V external LDO output measurement point

Table 4 lists the EVM connector functions.

Table 4. Connector Functions

Connector	TYPE	DESCRIPTION
J1	CB35-36-CY	VIN+ connector
J2	CB35-36-CY	VIN- connector
J3	TSW-102-07-G-D	Configuration Mode selection - NVM (Jumper Pin 1/2) or Pin Strap (Jumper Pin 3/4)
J4	TSW-102-07-G-S	Reset (Jumper Pin 1/2)
J5	TSW-105-07-G-D	PMBus connector
J6	TSW-103-07-G-S	PMBus pull up voltage selection - 1.8V (Jumper Pin 1/2) or 3.3V (Jumper Pin 2/3)
J7	TSW-102-07-G-S	V _{OUT} connector for bode plot measurement
J8	TSW-102-07-G-S	V _{OUT} connector for bode plot measurement
J9	TSW-102-07-G-S	V _{OUT} measurement connector
J10	CB35-36-CY	V _{OUT+} connector
J11	CB35-36-CY	V _{OUT+} connector
J12	CB35-36-CY	V _{OUT+} connector
J13	CB35-36-CY	V _{OUT-} connector
J14	CB35-36-CY	V _{OUT-} connector
J15	CB35-36-CY	V _{OUT-} connector
J16	CB35-36-CY	5VIN_INT connector (unused)
J19	ED555/2DS	5VIN connector

6 EVM Configuration Using the Fusion GUI

The controller on this EVM leaves the factory pre-configured. [Table 5](#) lists some key factory configuration parameters from the configuration file.

Table 5. Key Factory Configuration Parameters

CMD NAME	PMBus Command Code	Hex Value	Physical Setting	COMMENTS
VIN UVLO	0xE0	0x01	7.25 V	Input voltage turn on threshold
IOUT_OC_FAULT_LIMIT	0x46	0x00E2	226.00 A	OC fault level
IOUT_OC_WARN_LIMIT	0x4A	0x00B5	181.0 A	OC warning level
ON_OFF_CONFIG	0x02	0x17	Control Pin only	Power is converted when the control pin is active
OT_FAULT_LIMIT	0x4F	0x007D	125 °C	OT fault level
OT_WARN_LIMIT	0x51	0x005F	95 °C	OT warn level
Max Num Phases	0xE4	0x05	6 Phase	phase numbers
SWITCHING FREQUENCY	0xDC	0x20	500kHz	switching frequency
VBOOT	0xDB	0x97	1.000V	VBOOT voltage

To configure the EVM with other than the factory settings shown in [Table 5](#), use the *TI Fusion Digital Power Designer* software for reconfiguration. Be sure to apply the 5VIN input voltage to the EVM prior to launching the software. This sequence ensures that the controller and GUI recognize each other.

6.1 Configuration Procedure

1. Adjust the input supply 5VIN to provide 5 VDC, current limited to 1 A.
2. Apply the input power source VIN to the EVM. Refer to [Figure 4](#) and [Figure 5](#) for connections and test setup.
3. Launch the Fusion GUI software. Refer to the screenshots in [Section 11](#) for more information.
4. Configure the EVM operating parameters as desired.

7 Test Procedure

7.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Set up EVM as described in [Figure 4](#).
2. Ensure the electronic load is set to draw 0 Adc.
3. Increase 5VIN from 0 V to 5 V.
4. Increase VIN from 0 V to 12 V.
5. Put switch S1 to *ON* position.
6. Turn on the external fan if necessary.
7. Vary the load from 0 Adc to 180 Adc. Ensure V_{OUT} remains in regulation as defined in [Table 1](#).
8. Vary VIN from 8 V to 14 V. Ensure V_{OUT} remains in regulation as defined in [Table 1](#).
9. Decrease the load to 0 A.
10. Put switch S1 to *OFF* position.
11. Decrease VIN to 0 V.
12. Decrease 5VIN to 0 V.
13. Shut down the external fan if in use.

7.2 Control Loop Gain and Phase Measurement Procedure

The TPS53667EVM-769 includes a 0- Ω series resistor R77 in the feedback loop. This resistor value can be changed to 10 Ω to create an injection point for the loop perturbation needed to perform the loop response analysis. The injection point is accessible across the J7+ and J8+ connector pins. The loop response measurement probes should be placed across the J8 connector for the Input and the J7 connector for the Output with the resulting magnitude and phase plots derived from the Output/Input calculation (J7/J8). See short description below in [Table 6](#).

Table 6. Test Points for Loop Response Measurements

TEST POINT	NODE	DESCRIPTION	COMMENT
J8	INPUT	Input to feedback of V_{OUT}	The amplitude of the perturbation at this node should be limited to less than 100 mV.
J7	OUTPUT	Resulting output of V_{OUT}	Bode can be measured by a network analyzer as J7 / J8.

7.2.1 Procedure

1. Set up EVM as described in [Figure 4](#).
2. Connect the network analyzer isolation transformer across J8+ to J7+.
3. Connect the input signal measurement probe to J8+.
4. Connect output signal measurement probe to J7+.
5. Connect the ground leads of both probe channels to J7– or J8–.
6. On the network analyzer, measure the Bode as J7+ / J8+ (Out / In).
7. Disconnect the isolation transformer from the bode plot test points and change the resistor R77 back to 0 Ω before making other measurements, because the signal injection into the feedback loop may interfere with the accuracy of other measurements.

7.3 Efficiency

In order to derive the efficiency of the power train on the EVM, it is important to measure the input and output voltages at specific locations. This is necessary to prevent the inclusion of losses that are not specifically related to the power train itself, such as, losses incurred by the voltage drop in the copper traces or in the input and output connectors.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

Figure 6 shows the measurement points that were used for the input voltage and output voltage. Using these measurement points results in an efficiency derivation which does not include losses due to the connectors and PCB traces.

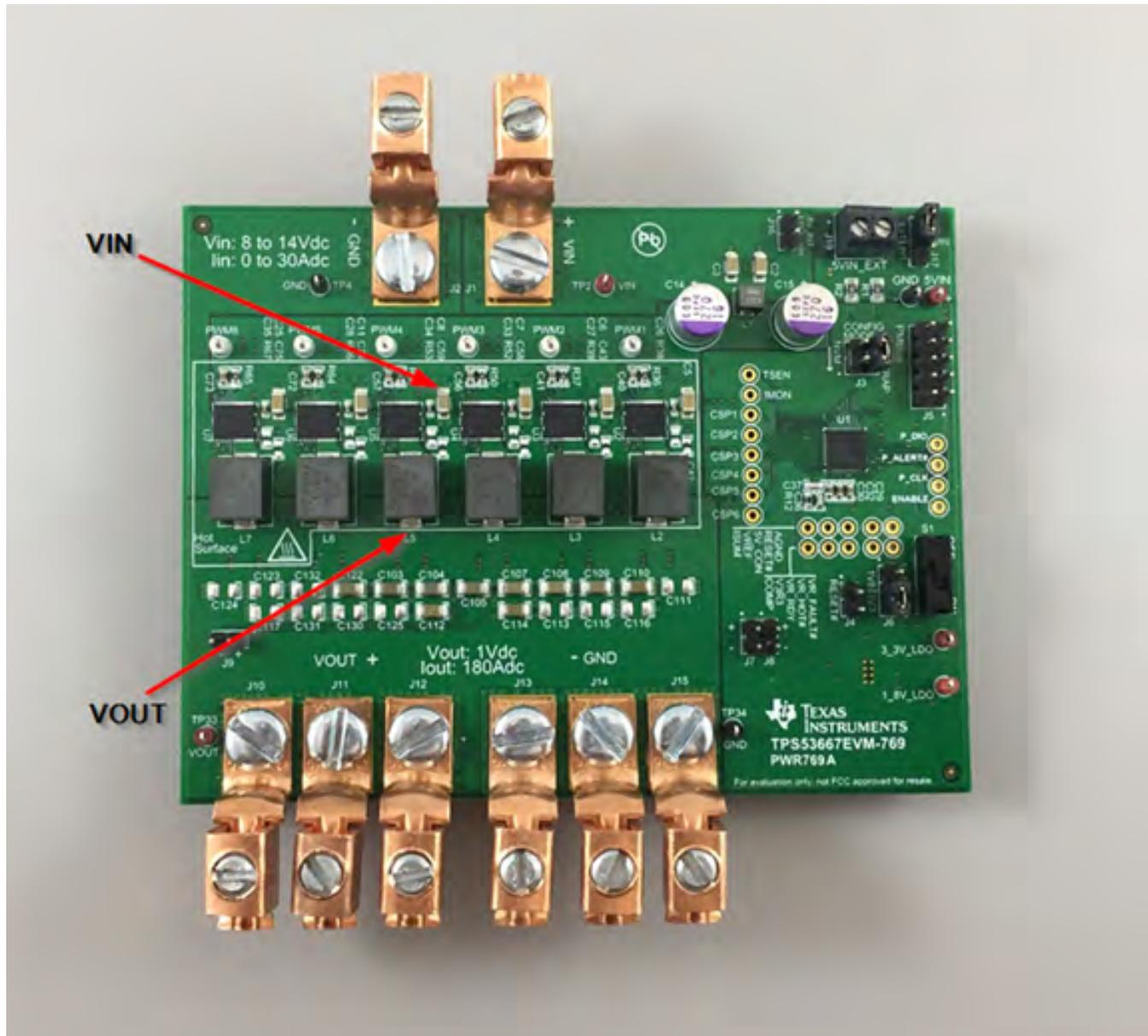


Figure 6. Test Setup for Efficiency Measurement

7.4 Equipment Turn-on and Shutdown

7.4.1 Turn-on Sequence

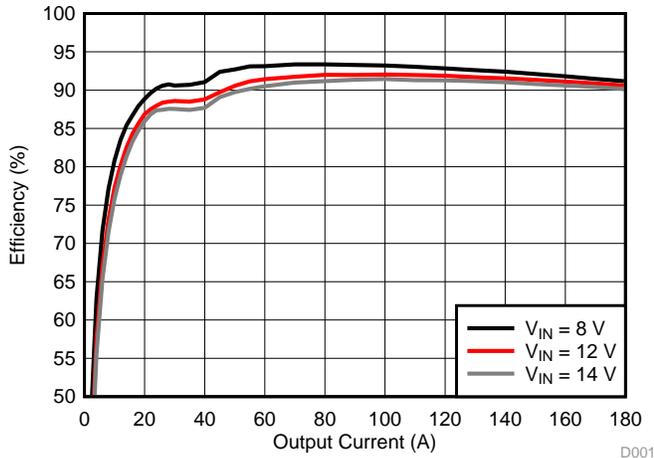
1. Turn on input power supply 5VIN.
2. Turn on input power supply VIN and increase VIN above 8 V.
3. Switch S1 to 'ON' position.
4. Adjust load current as desired.
5. Turn on the external fan if necessary.

7.4.2 Shutdown Sequence

1. Reduce the load current to 0 A.
2. Switch S1 to 'OFF' position.
3. Reduce input voltage to 0 V and shut down input power supply VIN.
4. Shut down input power supply 5VIN.
5. Shut down the external FAN if in use.

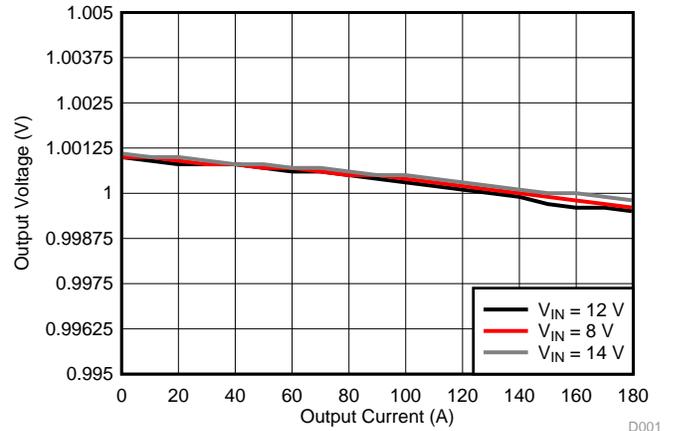
8 Performance Data and Typical Characteristic Curves

Figure 7 through Figure 9 show the typical performance curves for the TPS53667EVM-769.



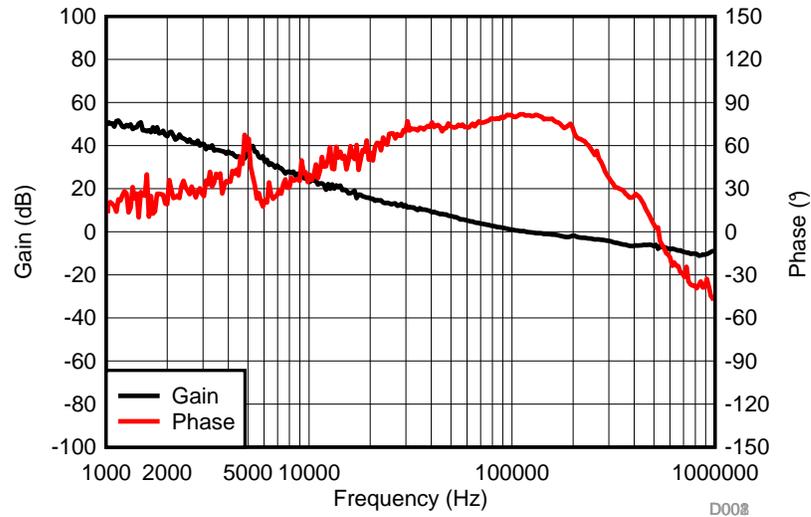
V_{OUT} = 1.0 V

Figure 7. Power Stage Efficiency vs Line and Load



V_{OUT} = 1.0 V

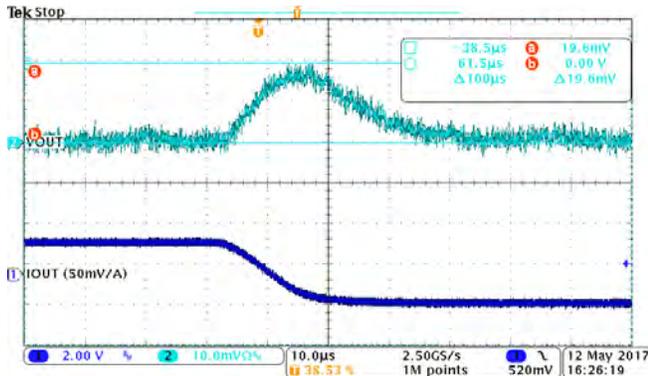
Figure 8. Load Regulation



V_{IN} = 12 V V_{OUT} = 1.0 V I_{OUT} = 180 A

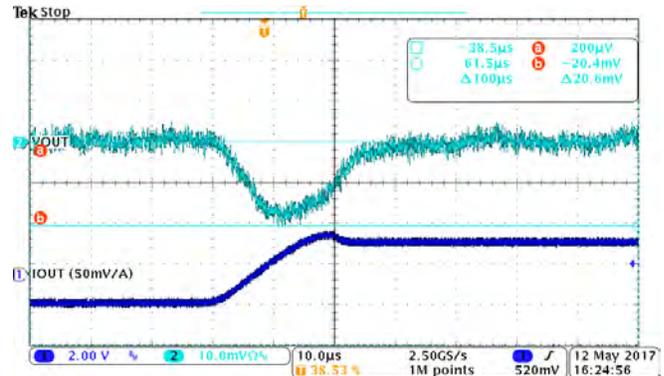
Figure 9. Bode Plot

Figure 11 through Figure 15 show the waveforms for the TPS53667EVM-769.



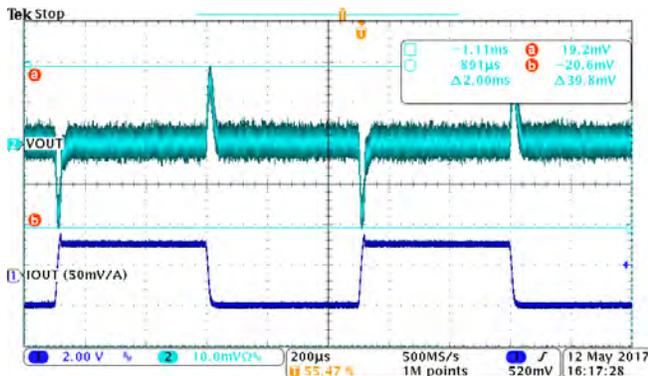
VIN = 12 V, VOUT = 1.0 V

Figure 10. Transient Response (Load Step 60 A to 0 A, 5A/us Slew Rate)



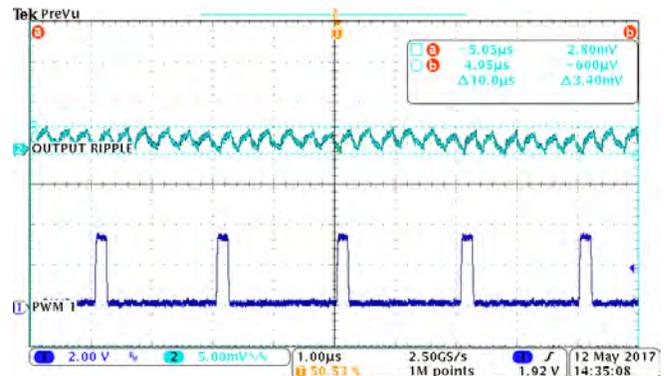
VIN = 12 V, VOUT = 1.0 V

Figure 11. Transient Response (Load Step 0 A to 60 A, 5A/us Slew Rate)



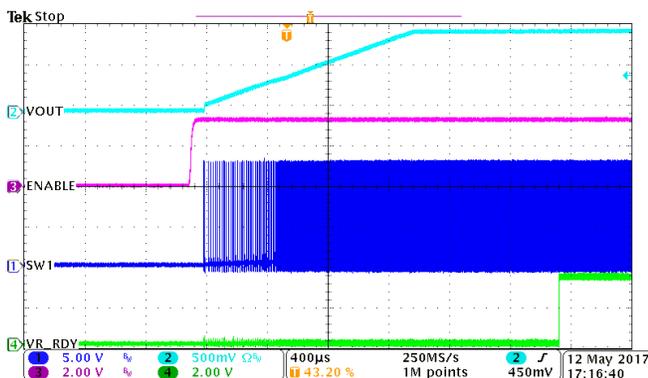
VIN = 12 V, VOUT = 1.0 V

Figure 12. Transient Response (Load Step 0 A to 60 A to 0A, 5A/us Slew Rate)



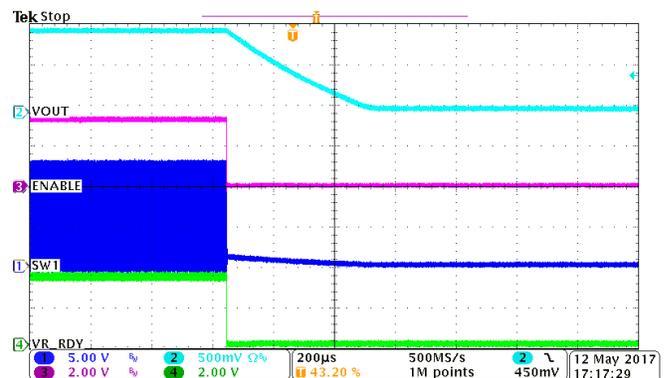
VIN = 12 V, VOUT = 1.0 V, IOUT = 180 A

Figure 13. Output Ripple



VIN = 12 V, VOUT = 1.0 V, IOUT = 0 A

Figure 14. Enable Startup



VIN = 12 V, VOUT = 1 V, IOUT = 6 A

Figure 15. Enable Shutdown

9 EVM Assembly Drawing and PCB Layout

Figure 16 through Figure 25 show the design of the TPS53667EVM-769 printed circuit board.

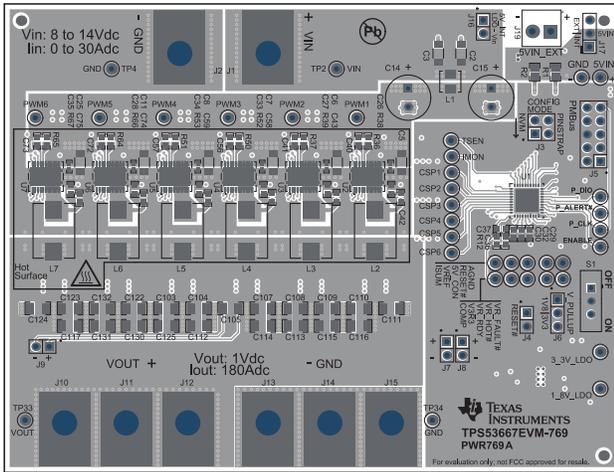


Figure 16. Top Layer Assembly Drawing (Top View)

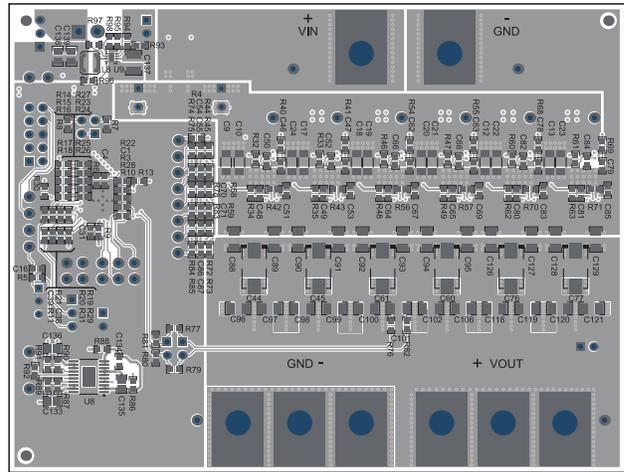


Figure 17. Bottom Layer Assembly Drawing (Bottom View)

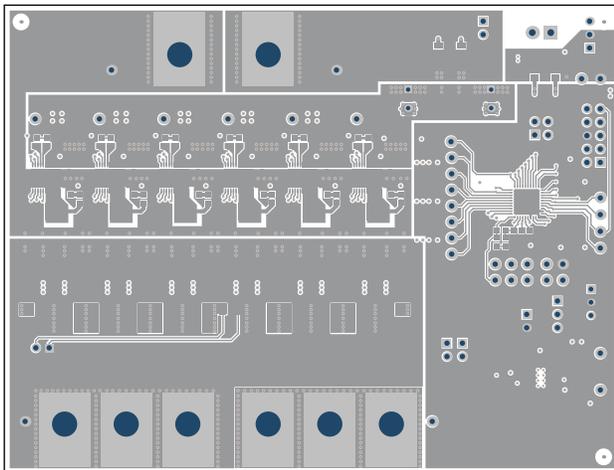


Figure 18. Top Copper (Top View)

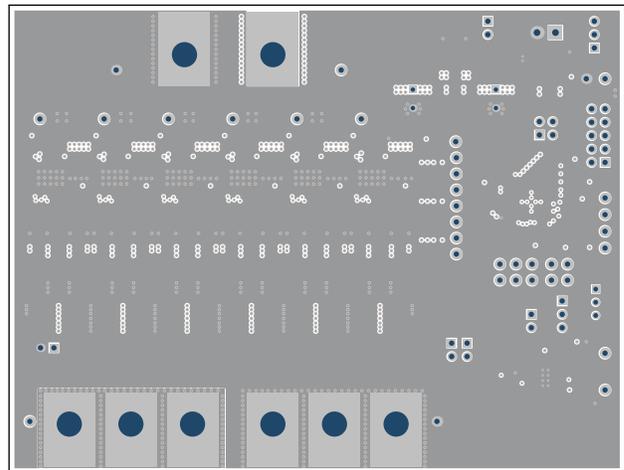


Figure 19. Internal Layer 1 (Top View)

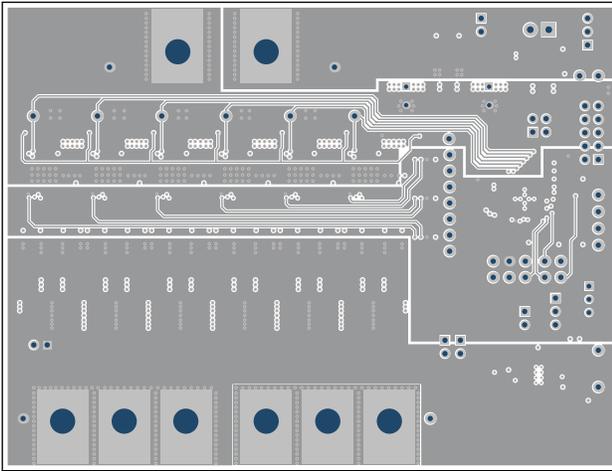


Figure 20. Internal Layer 2 (Top View)

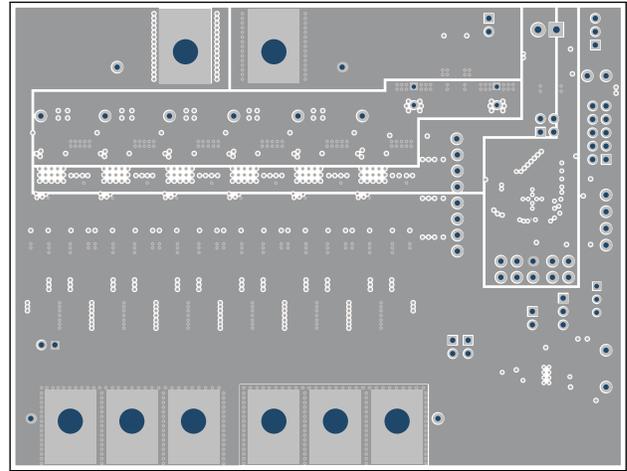


Figure 21. Internal Layer 3 (Top View)

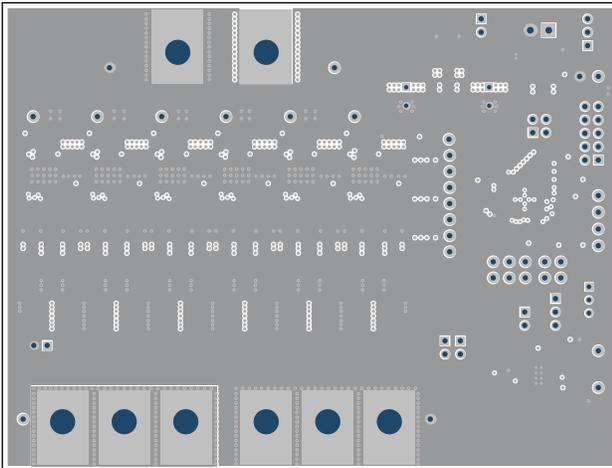


Figure 22. Internal Layer 4 (Top View)

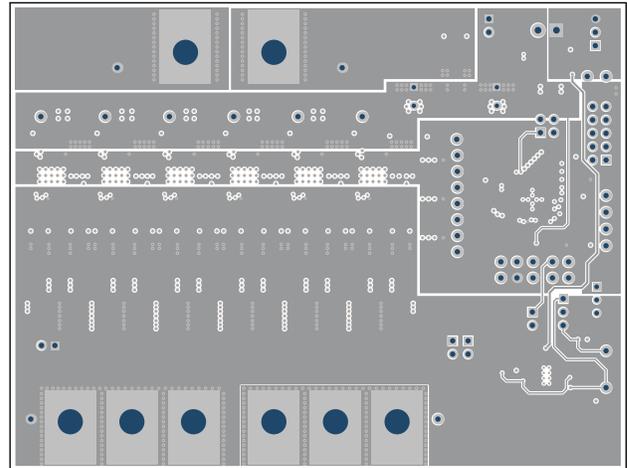


Figure 23. Internal Layer 5 (Top View)

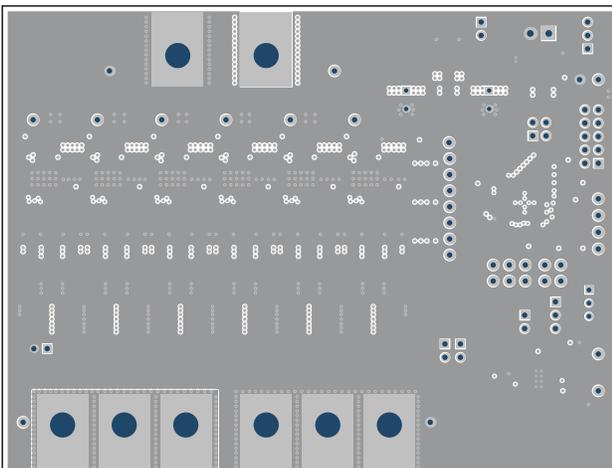


Figure 24. Internal Layer 6 (Top View)

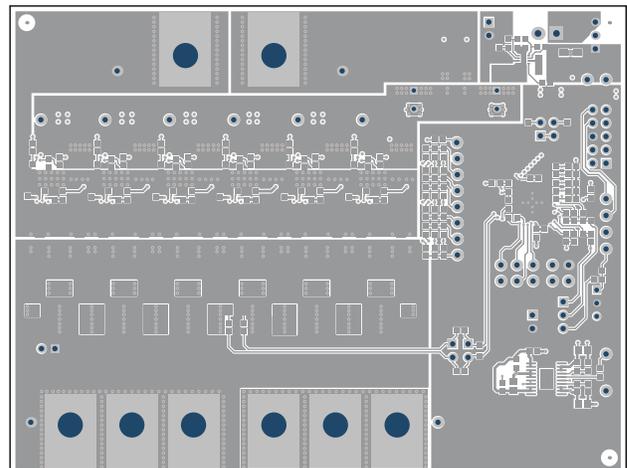


Figure 25. Bottom Copper (Top View)

10 List of Materials

Table 7. List of Materials

QTY ⁽¹⁾	REF DES	DESCRIPTION	PART NUMBER	MANUF
1	PCB1	Printed Circuit Board	PWR769	Any
1	C1	CAP, CERM, 2200 pF, 50 V, ± 10%, X7R, 0603	C0603C222K5RACTU	Kemet
20	C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C17, C18, C19, C20, C21, C22, C23, C24, C25	CAP, CERM, 22 µF, 25 V, ± 20%, X5R, 1206_190	C3216X5R1E226M160AB	TDK
1	C4	CAP, CERM, 1000 pF, 16 V, ± 10%, X7R, 0603	GRM188R71C102KA01D	MuRata
2	C14, C15	CAP, AL, 270 µF, 16 V, ± 20%, 0.01 ohm, TH	16SEPC270MX	Panasonic
1	C16	CAP, CERM, 0.01 µF, 25 V, ± 10%, X7R, 0603	GRM188R71E103KA01D	MuRata
6	C26, C27, C28, C33, C34, C35	CAP, CERM, 3300 pF, 50 V, ± 10%, X7R, 0402	C1005X7R1H332K050BA	TDK
1	C29	CAP, CERM, 4.7 µF, 16 V, ± 10%, X5R, 0603	GRM188R61C475KAAJD	MuRata
1	C30	CAP, CERM, 0.33 µF, 10 V, ± 10%, X7R, 0603	GRM188R71A334KA61D	MuRata
1	C31	CAP, CERM, 1 µF, 25 V, ± 10%, X7R, 0603	GRM188R71E105KA12D	MuRata
2	C32, C38	CAP, CERM, 1 µF, 10 V, ± 10%, X7R, 0603	GRM188R71A105KA61D	MuRata
1	C36	CAP, CERM, 1000 pF, 25 V, ± 5%, C0G/NP0, 0603	GRM1885C1E102JA01D	MuRata
1	C37	CAP, CERM, 12 pF, 50 V, ± 5%, C0G/NP0, 0603	GRM1885C1H120JA01D	MuRata
14	C39, C40, C41, C51, C53, C56, C57, C67, C69, C72, C73, C83, C85, C134	CAP, CERM, 0.1 µF, 25 V, ± 10%, X7R, 0603	GRM188R71E104KA01D	MuRata
4	C45, C60, C61, C76	CAP, Aluminum Polymer, 470 µF, 2.5 V, ± 20%, 0.003 ohm, SMD_7.3x1.9x4.3mm SMD	EEF-GX0E471R	Panasonic
12	C46, C47, C50, C52, C62, C63, C66, C68, C78, C79, C82, C84	CAP, CERM, 1000 pF, 25 V, ± 10%, X7R, 0603	GRM188R71E102KA01D	MuRata
6	C48, C49, C64, C65, C80, C81	CAP, CERM, 2.2 µF, 10 V, ± 10%, X7R, 0603	GRM188R71A225KE15D	MuRata
20	C90, C92, C94, C98, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C112, C114, C122, C126, C128	CAP, CERM, 100 µF, 4 V, ± 20%, X5R, 1206	GRM31CR60G107ME39L	MuRata
3	C133, C135, C136	CAP, CERM, 10 µF, 10 V, ± 20%, X5R, 0805	GRM219R61A106ME47L	MuRata
1	C137	CAP, CERM, 22 µF, 25V, ±10%, X5R, 1210	GRM32ER61E226KE15L	MuRata
2	C138, C139	CAP, CERM, 10 µF, 10V, ±10%, X5R, 0805	GRM21BR61A106KE19L	MuRata
8	H1, H2, H3, H4, H5, H6, H7, H8	Machine Screw Nut, Hex, 3/8", Stn, Steel, 10-32	HNSS 102	BF Fastener Supply
8	H9, H10, H11, H12, H13, H14, H15, H16	Machine Screw Pan Philips 10-32	PMSSS 102 0050 PH	BF Fastener Supply
8	H17, H18, H19, H20, H21, H22, H23, H24	Washer, Split Lock, #10	1477	Keystone

⁽¹⁾ component of quantity 0 indicates not populated.

Table 7. List of Materials (continued)

QTY ⁽¹⁾	REF DES	DESCRIPTION	PART NUMBER	MANUF
8	J1, J2, J10, J11, J12, J13, J14, J15	Terminal 50A Lug	CB35-36-CY	Panduit
1	J3	Header, 100mil, 2x2, Gold, TH	TSW-102-07-G-D	Samtec
5	J4, J7, J8, J9, J16	Header, 100mil, 2x1, Gold, TH	TSW-102-07-G-S	Samtec
1	J5	Header, 100mil, 5x2, Gold, TH	TSW-105-07-G-D	Samtec
2	J6, J17	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
1	J19	Terminal Block, 3.5mm Pitch, 2x1, TH	ED555/2DS	On-Shore Technology
1	L1	Inductor, 65 nH, 24 A, 0.00032 ohm, SMD	59PR65-650	Vitec Corporation
6	L2, L3, L4, L5, L6, L7	Inductor, Ferrite, 150 nH, 41 A, 0.00029 ohm, SMD	PA2607.151NLT	Pulse Engineering
1	L8	Inductor, Shielded Drum Core, Ferrite, 10uH, 0.7A, 0.33 ohm, SMD	LPS3314-103MRB	Coilcraft
2	R1, R2	RES, 1.0, 5%, 0.125 W, 0805	CRCW08051R00JNEA	Vishay-Dale
1	R3	RES, 33.2 k, 1%, 0.1 W, 0603	CRCW060333K2FKEA	Vishay-Dale
26	R4, R28, R36, R37, R40, R41, R44, R45, R50, R51, R54, R55, R58, R59, R64, R65, R68, R69, R72, R73, R76, R77, R79, R82, R88, R93	RES, 0, 5%, 0.1 W, 0603	MCR03EZPJ000	Rohm
1	R5	RES, 1.00 k, 1%, 0.1 W, 0603	CRCW06031K00FKEA	Vishay-Dale
1	R6	RES, 121 k, 1%, 0.1 W, 0603	CRCW0603121KFKEA	Vishay-Dale
2	R7, R24	RES, 150 k, 1%, 0.1 W, 0603	CRCW0603150KFKEA	Vishay-Dale
2	R8, R22	RES, 20.0 k, 1%, 0.1 W, 0603	CRCW060320K0FKEA	Vishay-Dale
7	R9, R34, R35, R48, R49, R62, R63	RES, 1.00, 1%, 0.1 W, 0603	CRCW06031R00FKEA	Vishay-Dale
1	R10	RES, 2.55 k, 1%, 0.1 W, 0603	CRCW06032K55FKEA	Vishay-Dale
2	R11, R92	RES, 2.00 k, 1%, 0.1 W, 0603	CRCW06032K00FKEA	Vishay-Dale
1	R12	RES, 8.06 k, 1%, 0.1 W, 0603	CRCW06038K06FKEA	Vishay-Dale
1	R13	RES, 4.32 k, 1%, 0.1 W, 0603	CRCW06034K32FKEA	Vishay-Dale
1	R14	RES, 12.4 k, 1%, 0.1 W, 0603	CRCW060312K4FKEA	Vishay-Dale
1	R15	RES, 26.7 k, 1%, 0.1 W, 0603	CRCW060326K7FKEA	Vishay-Dale
1	R16	RES, 9.31 k, 1%, 0.1 W, 0603	CRCW06039K31FKEA	Vishay-Dale
2	R17, R18	RES, 16.5 k, 1%, 0.1 W, 0603	CRCW060316K5FKEA	Vishay-Dale
13	R19, R20, R21, R29, R30, R31, R32, R33, R46, R47, R60, R61, R96	RES, 10.0 k, 1%, 0.1 W, 0603	CRCW060310K0FKEA	Vishay-Dale
1	R23	RES, 39.2 k, 1%, 0.1 W, 0603	CRCW060339K2FKEA	Vishay-Dale
2	R25, R26	RES, 24.3 k, 1%, 0.1 W, 0603	CRCW060324K3FKEA	Vishay-Dale
3	R27, R89, R91	RES, 30.1 k, 1%, 0.1 W, 0603	CRCW060330K1FKEA	Vishay-Dale
6	R42, R43, R56, R57, R70, R71	RES, 130 k, 1%, 0.1 W, 0603	RC0603FR-07130KL	Yageo America
1	R86	RES, 100 k, 1%, 0.1 W, 0603	CRCW0603100KFKEA	Vishay-Dale
1	R87	RES, 15.0 k, 1%, 0.1 W, 0603	CRCW060315K0FKEA	Vishay-Dale
1	R90	RES, 51.1 k, 1%, 0.1 W, 0603	CRCW060351K1FKEA	Vishay-Dale
1	R97	RES, 1.10Meg ohm, 1%, 0.1W, 0603	CRCW06031M10FKEA	Vishay-Dale

Table 7. List of Materials (continued)

QTY ⁽¹⁾	REF DES	DESCRIPTION	PART NUMBER	MANUF
1	R98	RES, 210k ohm, 1%, 0.1W, 0603	CRCW0603210KFKEA	Vishay-Dale
1	S1	Switch, SPDT, Slide, On-On, 2 Pos, TH	EG1218	E-Switch
3	SH-J3, SH-J6, SH-J17	Shunt, 100mil, Gold plated, Black	969102-0000-DA	3M
5	TP2, TP3, TP33, TP35, TP36	Test Point, Miniature, Red, TH	5000	Keystone
3	TP4, TP5, TP34	Test Point, Miniature, Black, TH	5001	Keystone
6	TP21, TP22, TP23, TP24, TP25, TP26	Test Point, Miniature, White, TH	5002	Keystone
1	U1	TPS53667RTAR, RTA0040B	TPS53667RTAR	Texas Instruments
6	U2, U3, U4, U5, U6, U7	Synchronous Buck NexFET Power Stage, DMC0012A	CSD95490Q5MC	Texas Instruments
1	U8	Dual Output LDO, 500 mA, 2.7 to 6 V Input, 20-pin HTSSOP (PWP), -40 to 125 degC, Green (RoHS & no Sb/Br)	TPS70102PWP	Texas Instruments
1	U9	3V-17V, 300mA Step Down Converter With Adjustable Enable Threshold And Hysteresis, DSG0008A	TPS62125DSGR	Texas Instruments
0	C42, C43, C58, C59, C74, C75	CAP, CERM, 1000 pF, 50 V, ± 10%, X7R, 0402	GRM155R71H102KA01D	MuRata
0	C44, C77	CAP, Aluminum Polymer, 470 µF, 2.5 V, ± 20%, 0.003 ohm, SMD_7.3x1.9x4.3mm SMD	EEF-GX0E471R	Panasonic
0	C54, C55, C70, C71, C86, C87	CAP, CERM, 1000 pF, 50 V, ± 5%, C0G/NP0, 0603	GRM1885C1H102JA01D	MuRata
0	C88, C89, C91, C93, C95, C96, C97, C99, C111, C113, C115, C116, C117, C118, C119, C120, C121, C123, C124, C125, C127, C129, C130, C131, C132	CAP, CERM, 100 µF, 4 V, ± 20%, X5R, 1206	GRM31CR60G107ME39L	MuRata
0	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
0	R38, R39, R52, R53, R66, R67	RES, 1.00, 1%, 0.1 W, 0603	CRCW06031R00FKEA	Vishay-Dale
0	R74, R75, R78, R83, R84, R85, R94, R95	RES, 0, 5%, 0.1 W, 0603	MCR03EZPJ000	Rohm
0	R80, R81	RES, 10.0 k, 1%, 0.1 W, 0603	CRCW060310K0FKEA	Vishay-Dale
0	TP1, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP27, TP28, TP29, TP30, TP31, TP32	Test Point, Miniature, White, TH	5002	Keystone

11 Fusion GUI

When the Fusion GUI launches, it restores user preferences and data.



Figure 26. Launch Fusion GUI

The Fusion GUI will open with the rail associated with the TPS53667 controller on the [System View] screen as shown in [Figure 27](#) . If this were a power system that was populated with multiple Fusion GUI compatible devices, all of them would show up in the System View window.

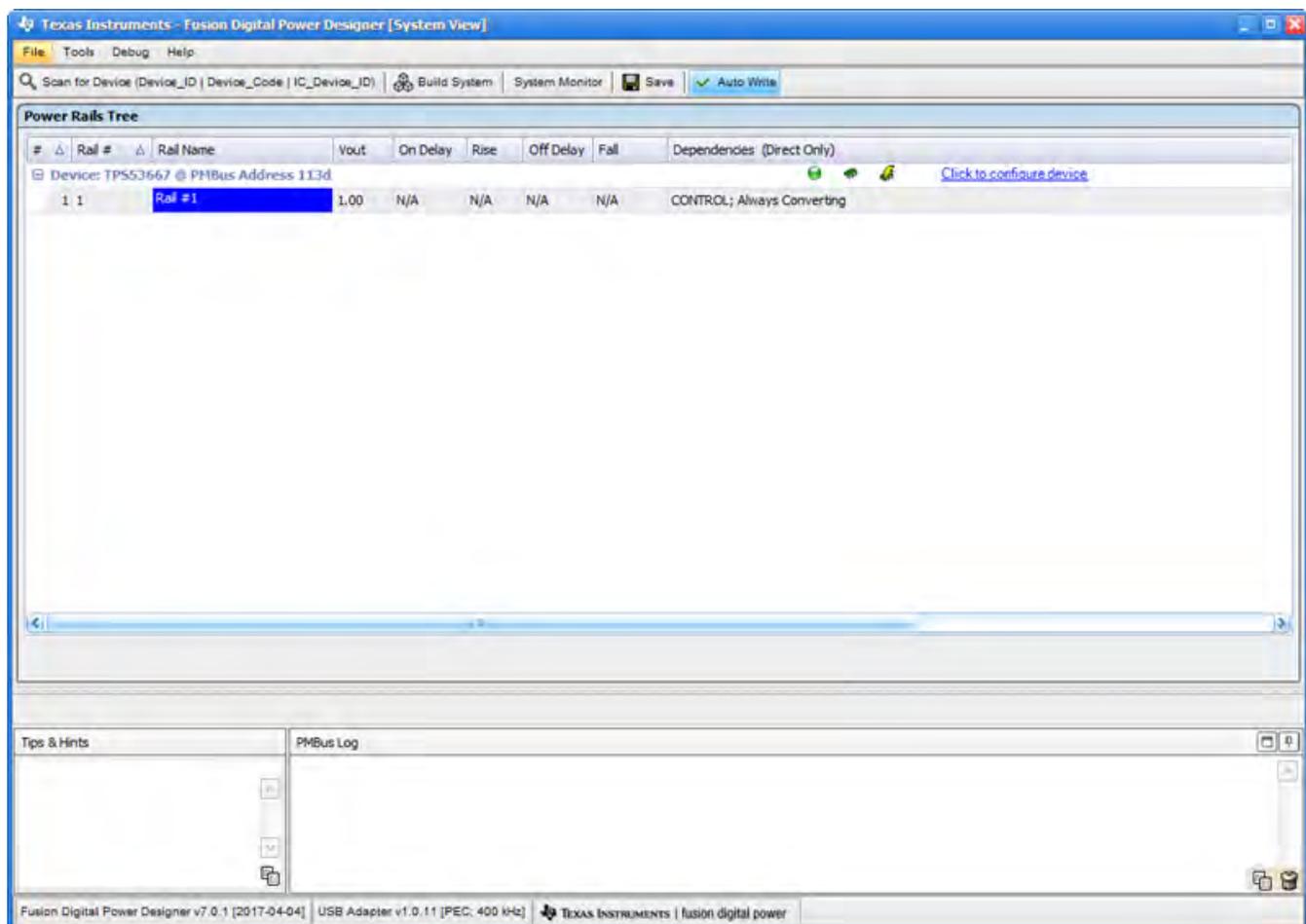


Figure 27. System View

Selecting [System Monitor] tab from the System View adds a new window which displays real-time system level information about all Fusion compatible devices connected as shown in Figure 28.

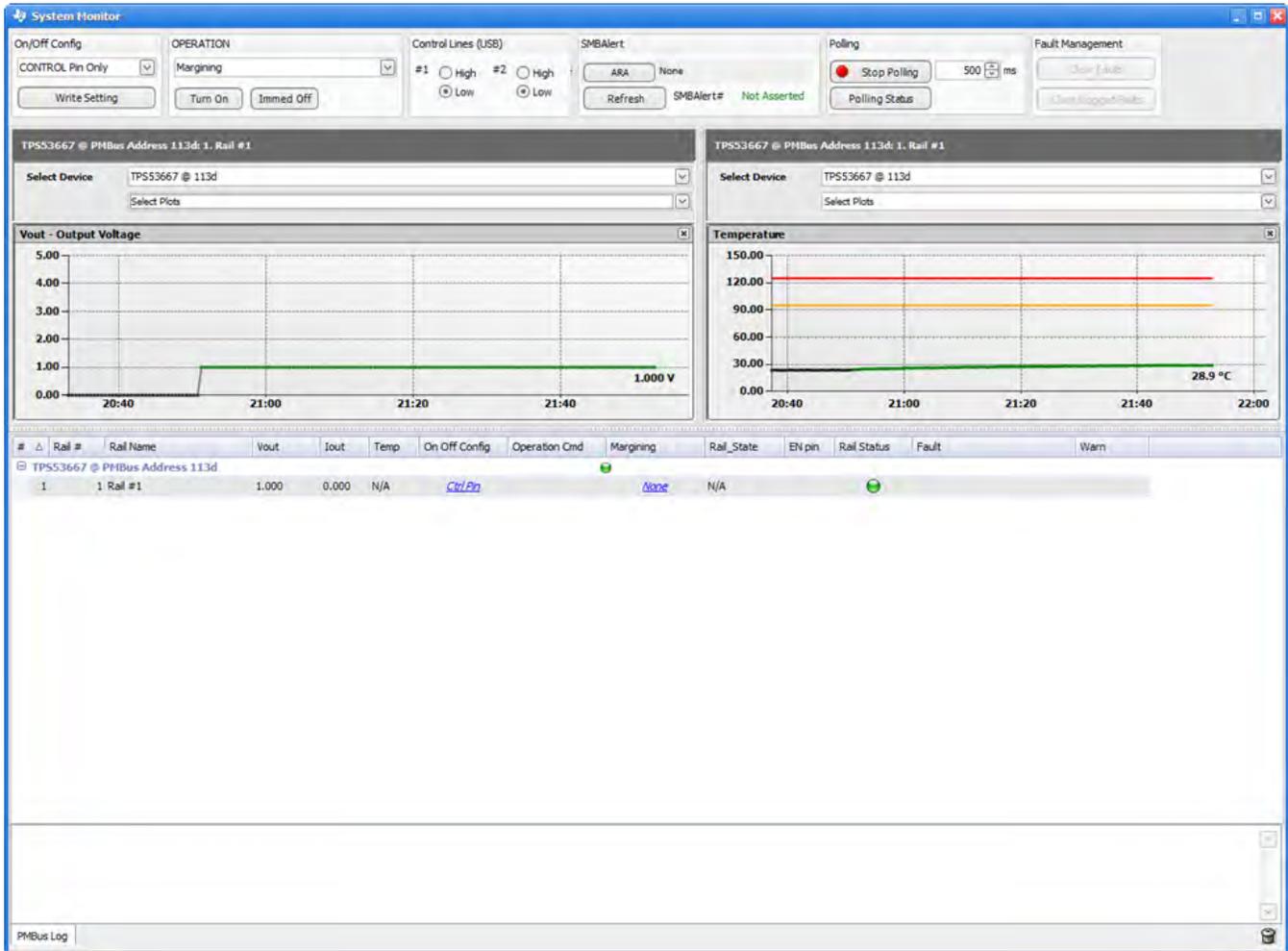


Figure 28. System Monitor

The configuration of a specific device can be accessed by selecting the [Click to Configure Device] associated with that device from the System View and a new window will open to the [General] tab on the [Configure] page of the GUI as shown in Figure 29, this screen can be used to verify/modify the following parameters:

- VBOOT
- V_{OUT} Command
- V_{IN} UVLO
- I_{IN} OC Fault and OC Warn Limits
- I_{OUT} OC Fault and OC Warn Limits
- OT Fault and Warn Limits
- I_{MAX}
- On/Off Config
- Margin High and Margin Low voltages
- Phase numbers

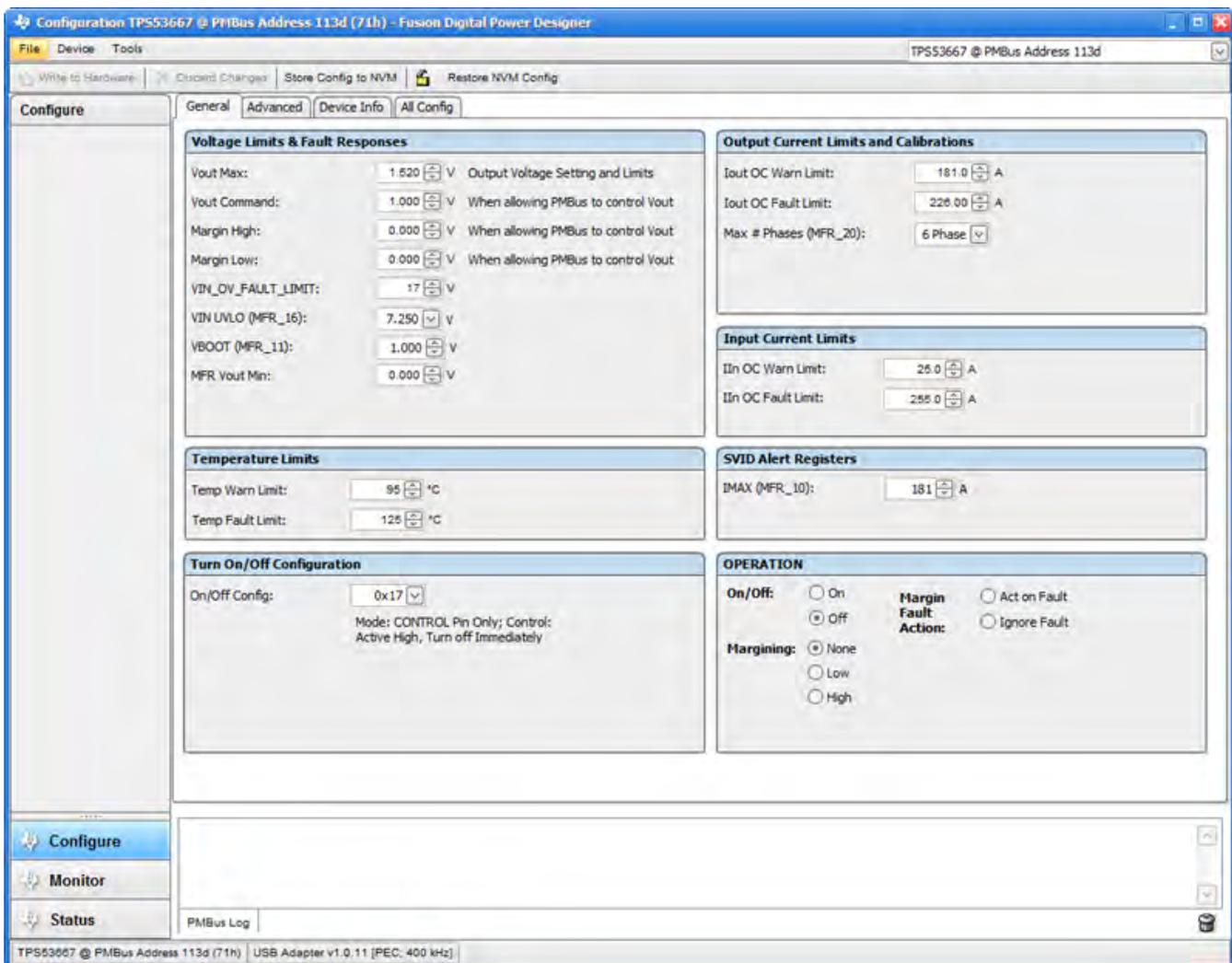


Figure 29. General Configure

Switch to the [Advanced] tab on the [Configure] page as shown in Figure 30 to verify/modify any of the following parameters:

- USR and OSR
- Switching Frequency
- RAMP
- OCL
- Mode
- Phase Interleaving
- Dynamic Phase Shedding
- Slew Rate
- Load-line

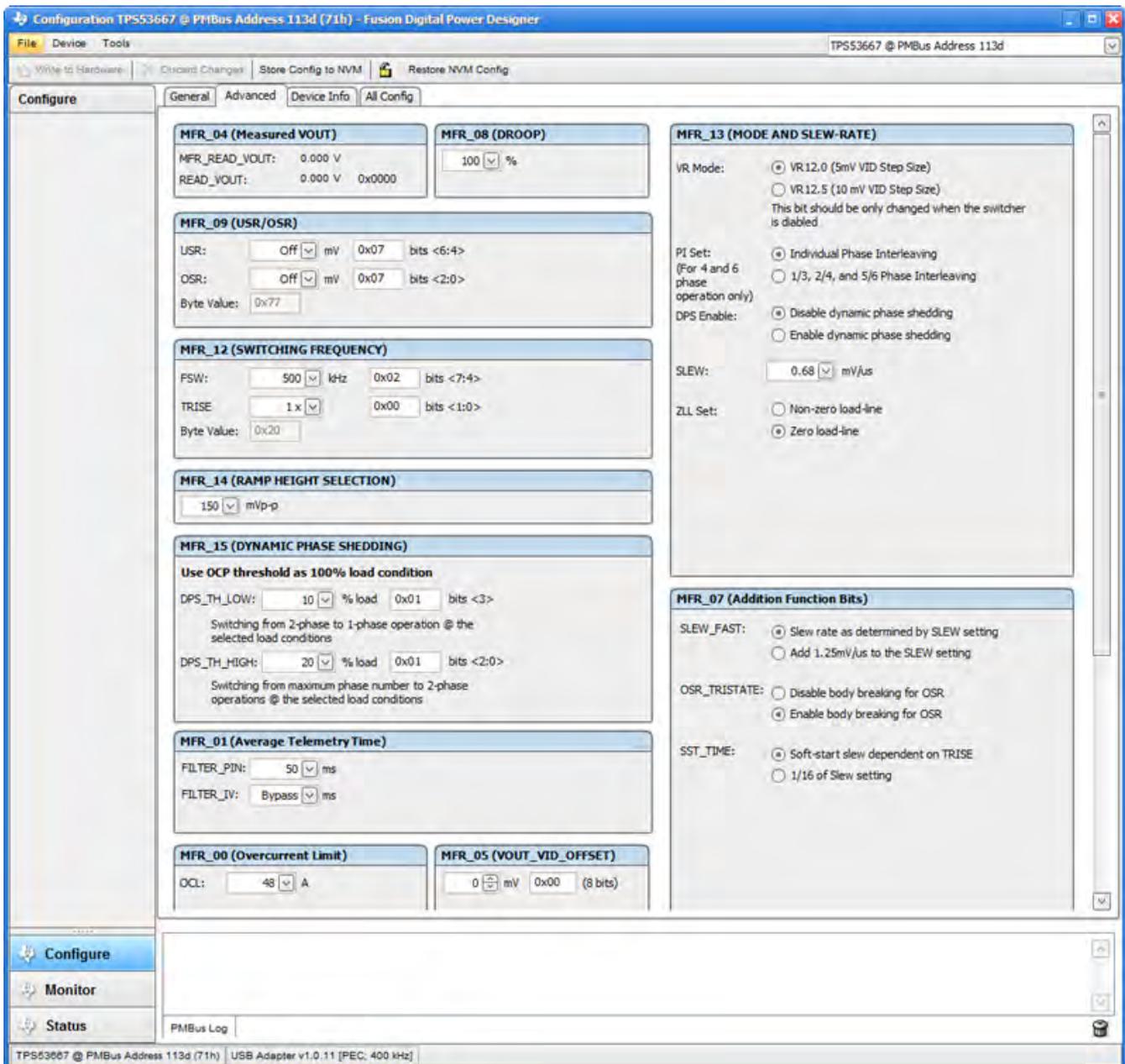


Figure 30. Advanced Configure

The [All Config] tab on the [Configure] page as shown in Figure 31 summarizes all the configurable parameters. This screen contains additional details such as the Hexadecimal encoding for the parameters.

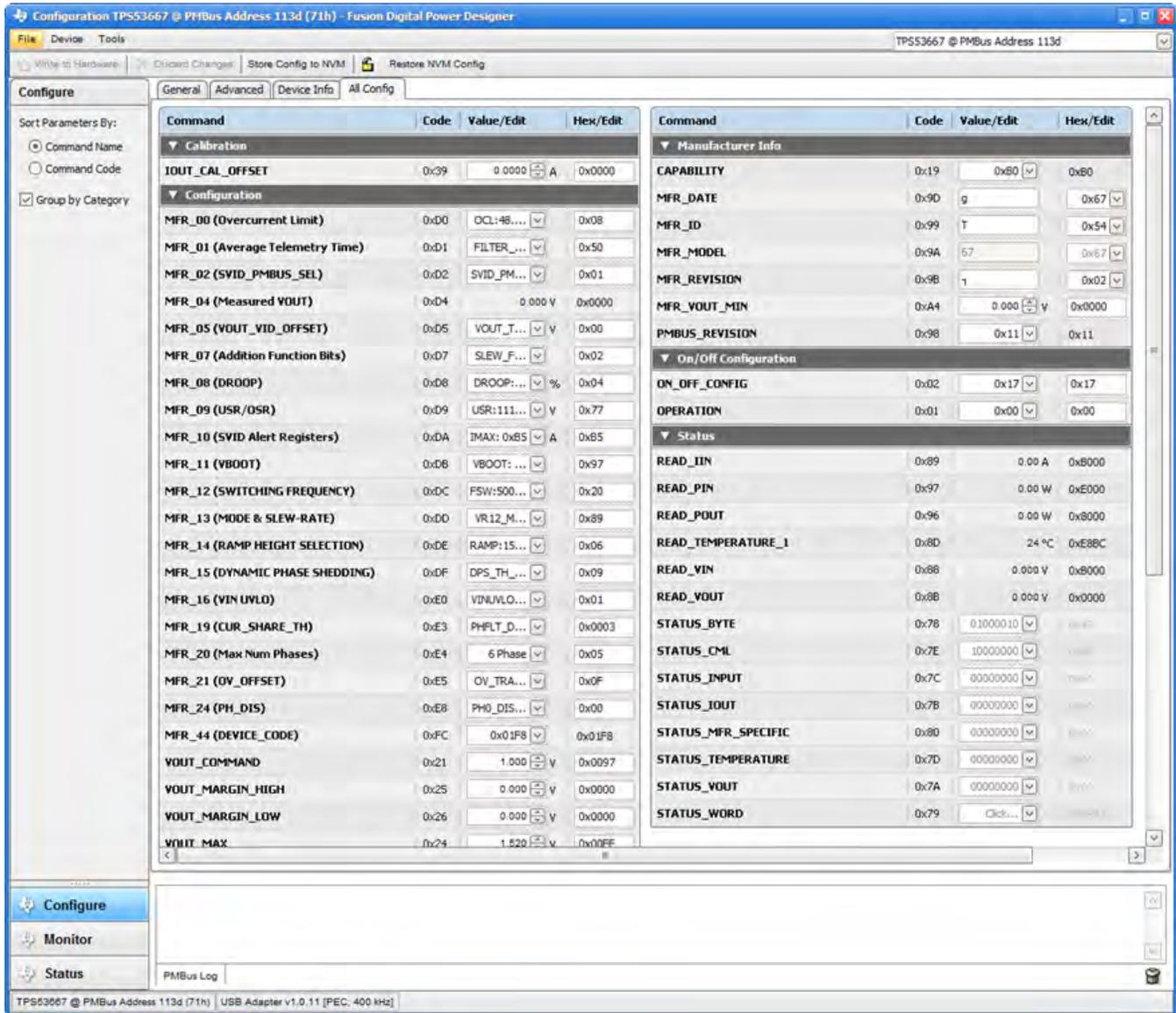


Figure 31. All Configure

If the user selects to change a parameter then the GUI will display an orange “U” icon, which is offering an [Undo Change] option, as shown in Figure 32. The software will not update the controller with the change until the user performs a [Write to Hardware].

When a [Write to Hardware] is performed, the change will be implemented in the controller and stored in it's volatile memory. Given that the parameter is stored in volatile memory, if the EVM is power cycled, the parameter will revert back to the previous setting.

If the user wishes to make this the new default value for the parameter then a [Store Config to NVM] must be performed, which commits the value to non-volatile memory.

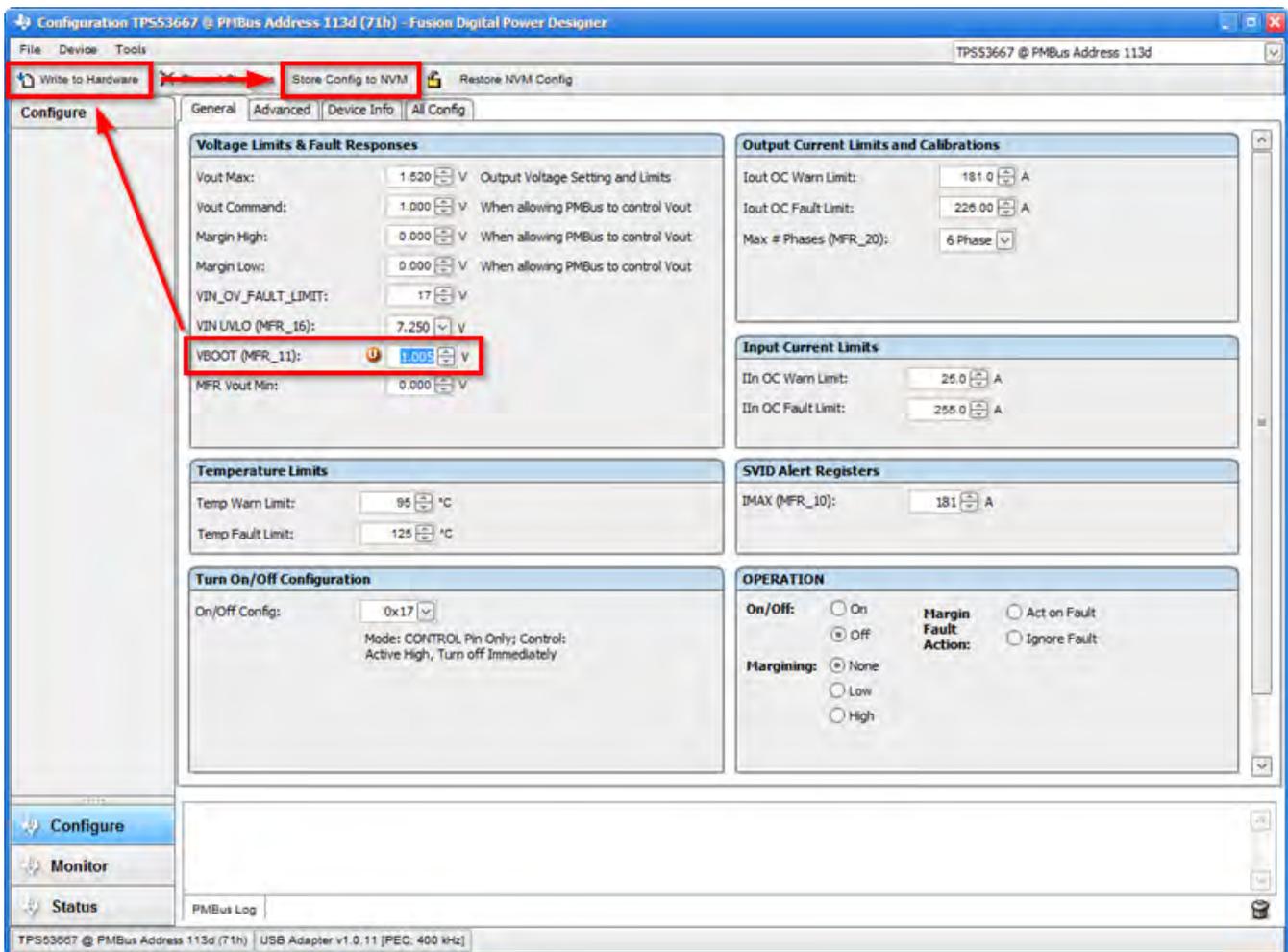


Figure 32. General Configure Pop-Up

Selecting the [Monitor] page from the lower left corner of the TPS53667 Configuration window will display the [Figure 33](#) which shows real-time parameter data as measured by the controller. This screen provides access to the following parameters:

- Graphs of
 - V_{IN}
 - V_{OUT}
 - I_{OUT}
 - Temperature
- Start/Stop Polling controls the updating of the real-time display of data
- Quick access to ON or OFF configuration
- Control pin activation and OPERATION command
 - Note: TPS53667 Enable pin is hardwired to Switch S1 on EVM, it is not connected to PMBus_CNTL line
- Margin control
- Clear Fault clears any prior fault flags

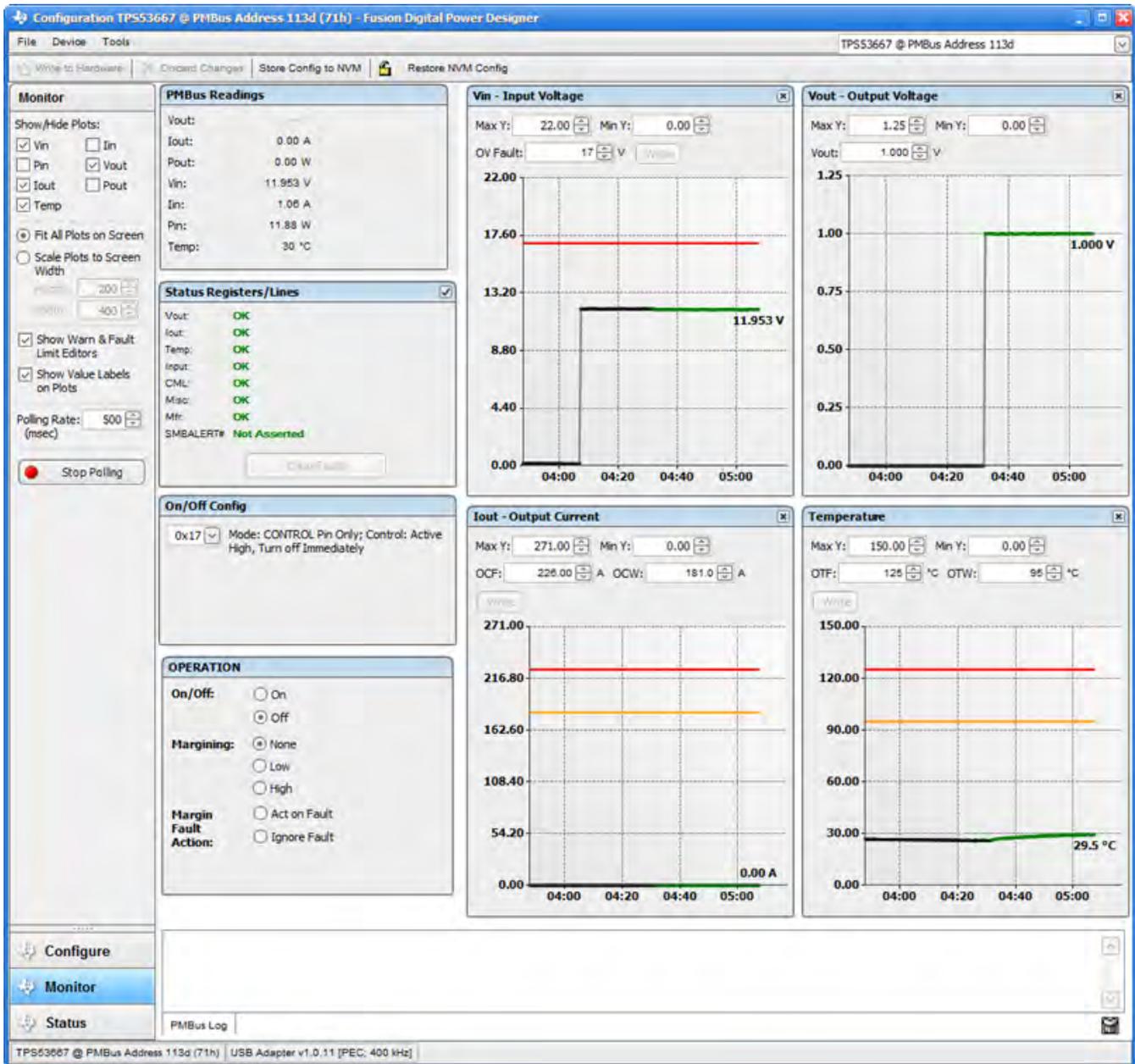


Figure 33. Monitor Screen

Selecting [Status] from lower left corner shows the current status of the controller as well as any prior faults or warnings which had not been cleared, as shown on the [Figure 34](#).

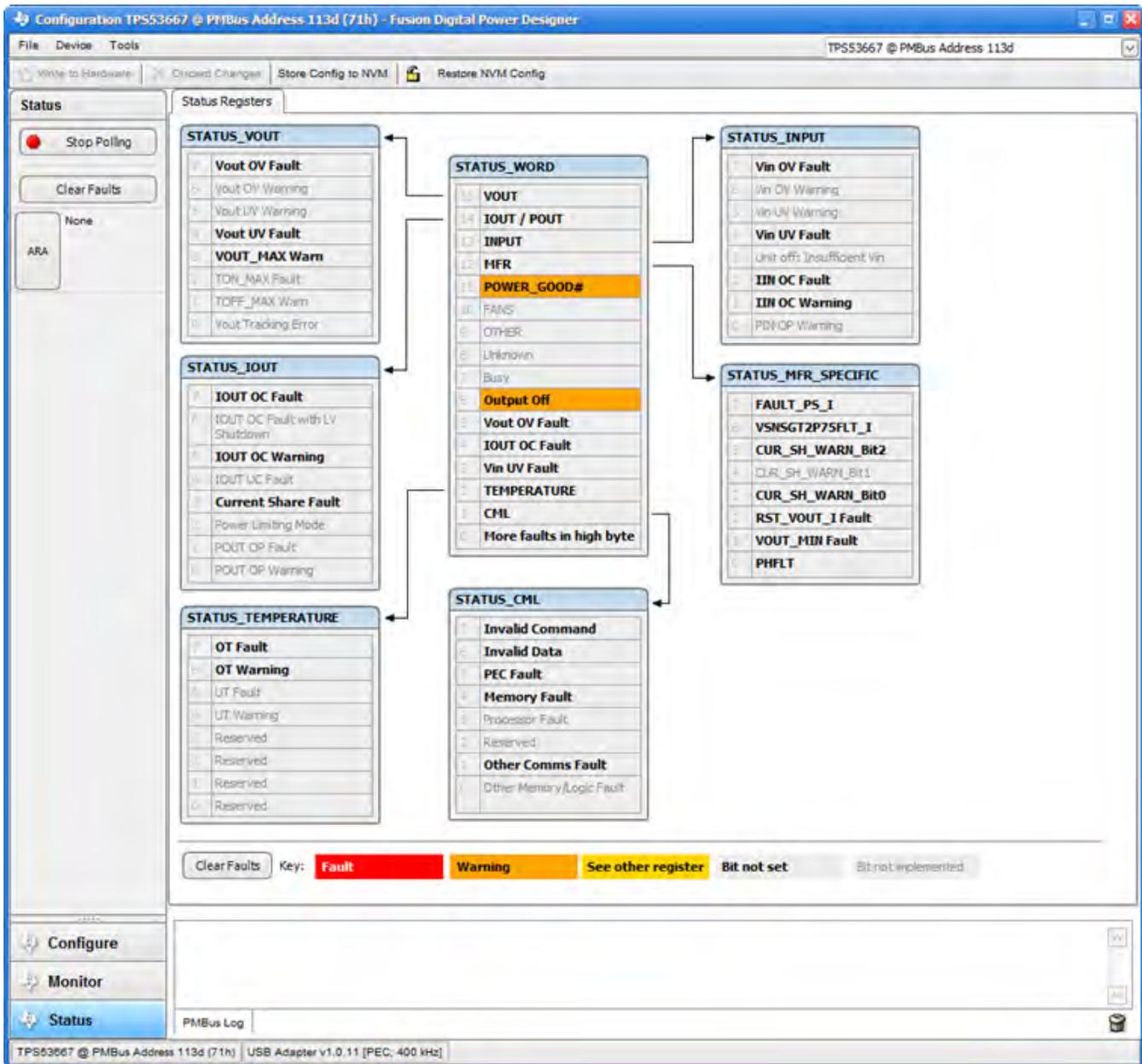


Figure 34. Status Screen

To overwrite the current configuration with a new off-line version or to revert back to a “known-good” previously saved version, use the pull down menu [File] → [Import Project] from the upper left menu bar to re-write all parameters in the device at once with the desired configuration (as shown in Figure 35) . This action results in a browse-type sequence that allows the user to locate and load the desired configuration file.

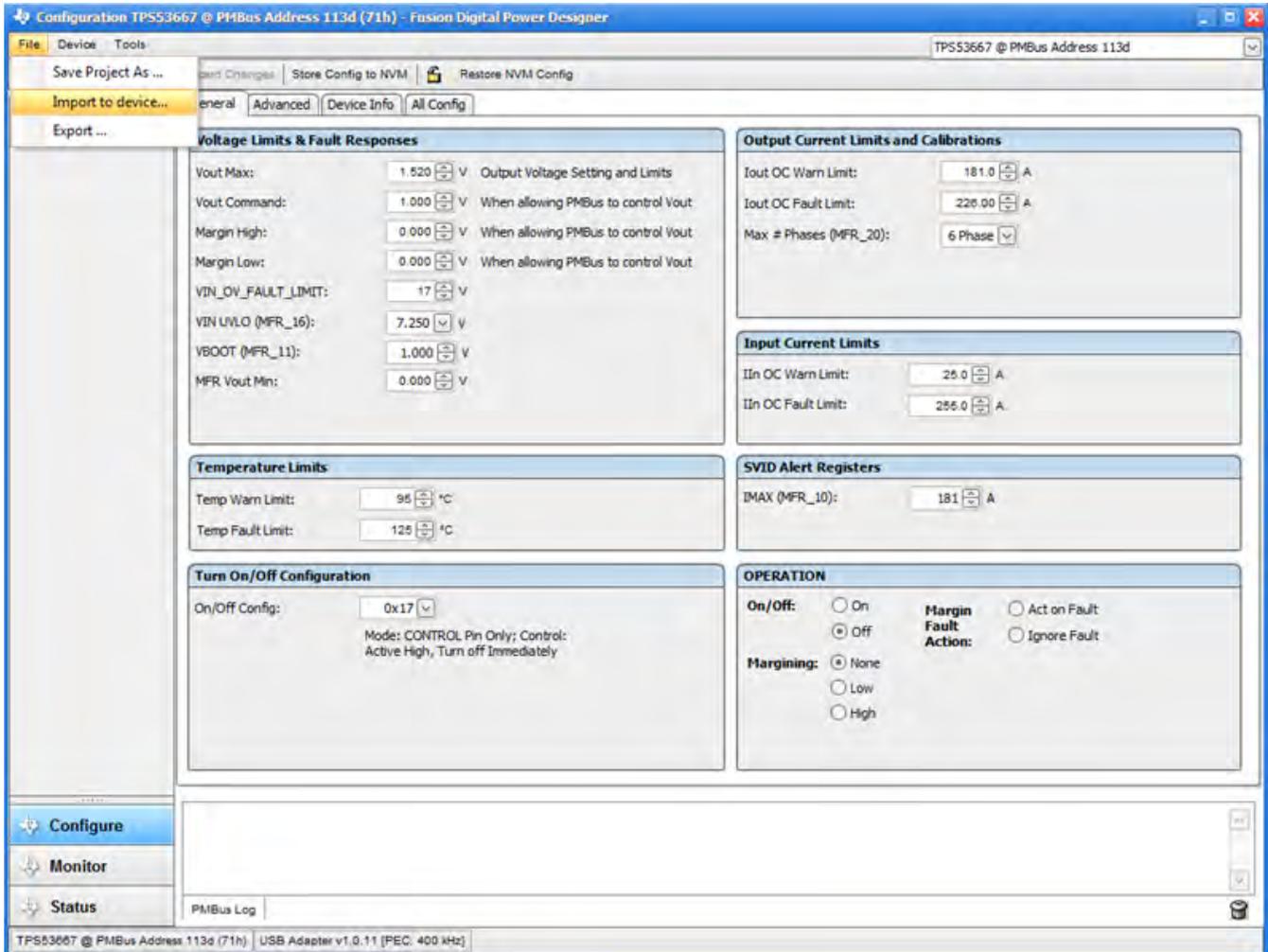


Figure 35. Import Configuration File

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated