

Using the UCC27282EVM-335

This user's guide describes the characteristics, operation, and use of the UCC27282 Evaluation Module (EVM). A complete schematic diagram, PCB layouts, and BOM are included in this document.

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1 Introduction

The UCC27282EVM-335 is designed to primarily evaluate the UCC27282 performance. This driver is a 100-V boot voltage, high-side, low-side driver with 3-A peak source and sink current for driving two N-Channel MOSFETs. The same board can be used to evaluate other pin-to-pin compatible parts in the supported package. The UCC27282 has low propagation delay and low propagation delay matching between the high- and low-side rising and falling edges of the driver outputs for reliable timing of the gate-drive signals. The UCC27282 inputs can tolerate signals as high as 16 V regardless of the V_{DD} voltage which enhances device robustness.

The UCC27282 driver includes an enable function which enables the driver outputs when pulled high, and disables the driver into a very low standby current mode when low. The UCC27282 also includes an interlock feature which sets both LO and HO driver outputs low when both LI and HI inputs are high at the same time. This prevents turning on the high-side and low-side MOSFETs at the same time enhancing robustness of the power train design.

2 Description

The EVM is developed in such a way that the UCC27282 driver performance can be evaluated and compared to data sheet parameters, or externally connected to power devices with provisions for source and sink gate-resistance flexibility. The UCC27282EVM-335 evaluation board uses surface-mount test points allowing connection to LI, HI, VDD, and HB inputs. A variety of other test points are available for probing the UCC27282. The input bias is configured such that the VHB-VHS high-side bias can be sourced from VCC, or an external additional bias can be added to provide VHB-VHS directly. The high- and low-side driver output returns are separated on HS and GND respectively to allow evaluation of the UCC27282 HS negative voltage capabilities. For detailed device information, see [UCC27282 Datasheet](#).

2.1 Features

The EVM supports the following features:

- EVM for the low-voltage features of the UCC27282 gate driver
- 6-V to 16-V V_{CC} power supply range
- TTL-compatible inputs
- PCB layout optimized for bias supply bypassing cap, gate-drive resistance selection
- Capacitive load, external gate drive resistor and diode for gate drive network evaluation
- Allows quick verification of most of the data sheet parameters
- Test points allow probing all the key pins of the UCC27282

2.2 I/O Description

Table 1 details the connection descriptions.

Table 1. Connection Descriptions

Pins	Description
VCC	V _{CC} positive input test point. Powers IC VDD pin, use 6-V to 16-V range.
VDD	V _{DD} positive input of UCC27282 IC
GND	Multiple test points. V _{CC} negative input, HI_IN, LI_IN, and ENA_IN negative inputs, and ground at UCC27282 IC
HI_IN	High-side input to EVM
HI	High-side input pin, HI
LI_IN	Low-side input to EVM
LI	Low-side input pin, LI
ENA_IN	Enable input to EVM. Connect to GND to disable driver.
VHB	HB pin voltage
HO LD	High-side output at capacitive load
HO	High-side output pin
HS	High-side driver return pin. Usually connected to high-side MOSFET source.
LO LD	Low-side output at capacitive load
LO	Low-side output pin

3 Electrical Specifications

Refer to the [UCC27282 Datasheet](#) for the full range of recommended operating specifications and design guidelines for driving loads.

CAUTION

The UCC27282EVM-335 is designed for low-voltage evaluation only, and is not certified for evaluation with voltages beyond the absolute maximums listed in the electrical specifications. Do **not** evaluate high-voltage parameters with this board.

4 Test Summary

4.1 Definitions

This procedure details how to configure the UCC27282EVM-335 evaluation board. Within this test procedure, the following naming conventions are applied. Refer to the UCC27282EVM-335 *Bench Setup Diagram and Configuration*, [Figure 1](#), for details.

DMM: Digital multimeter

EVM: Evaluation module

4.2 Equipment

4.2.1 Power Supply

DC power supply with voltage and current above 20 V and 1 A, for example: Agilent E3634A

4.2.2 Function Generator

Two-channel function generator over 10 MHz, for example: Tektronics AFG3252

4.2.3 DMM

DMM with voltage and current above 25 V and 1 A, for example: Fluke 187

4.2.4 Oscilloscope

Four channel oscilloscope with 500MHz or greater bandwidth, for example DPO 7054

4.3 Equipment Setup

4.3.1 DC Power Supply Settings

- DC power supply #1
 - Voltage setting: 12 V
 - Current limit: 0.05 A

4.3.2 Digital Multi-Meter Settings

- DMM #1
 - DC current measurement, auto-range. Expected current is within 1 mA to 15 mA.

4.3.3 Two-Channel Function Generator Settings

[Table 2](#) displays the two-channel function generator settings.

Table 2. Two-Channel Function Generator Settings

	Mode	Frequency	Width	Delay	High	Low	Output Impedance
Channel A	Pulse	100 kHz	2.5 μ s	0 us	5 V	0 V	High Z
Channel B			2.5 μ s	5 μ s			

The UCC27282 interlock function will result in HO and LO in the low state if HI and LI are high at the same time.

4.3.4 Oscilloscope Settings

Table 3 details the oscilloscope settings.

Table 3. Oscilloscope Settings

	Bandwidth	Coupling	Termination	Scale Settings	Inverting
Channel A	500 MHz or above	DC	1 M Ω or automatic	10x or automatic	OFF
Channel B					

4.3.5 Bench Setup Diagram

The bench setup diagram includes the function generator and oscilloscope connections.

Use the following connection procedure, refer to Figure 1.

- First, make sure the output of the function generator and power supplies are disabled before connection.
- Apply function generator channel-A on HI_IN-GND.
- Apply function generator channel-B on LI_IN-GND.
- Power supply #1: apply positive lead to current input of DMM #1 and current output of DMM #1 to test point VCC; apply negative lead to test point GND.
- Apply oscilloscope channel-1 probes on HO LD-HS, minimizing the loop area as much as possible. Note the scope ground is connected to HS test point.
- Apply oscilloscope channel-2 probes on LO LD-GND, minimizing the loop area as much as possible.

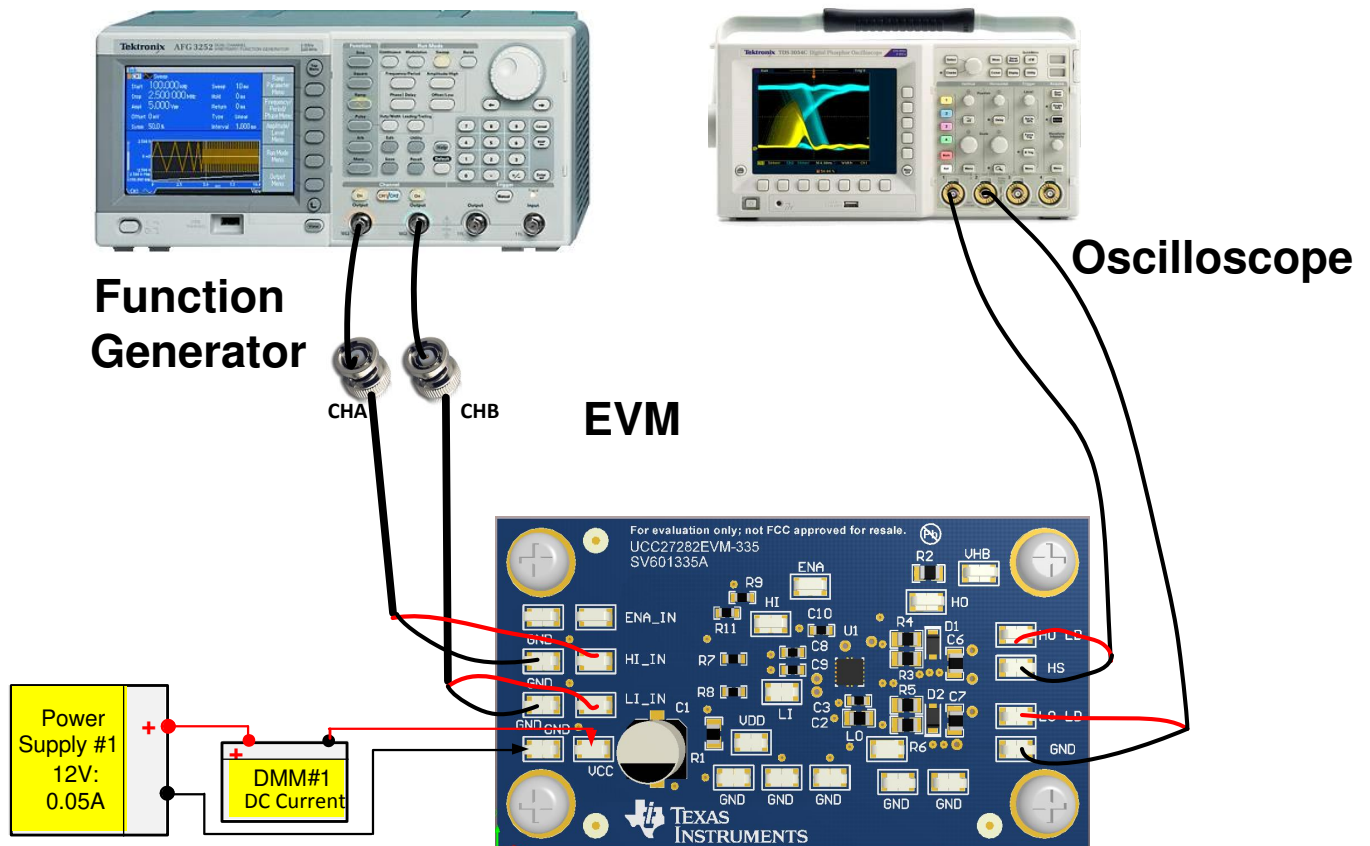


Figure 1. Bench Setup Diagram and Configuration

5 Power Up and Power Down Procedure

5.1 Power Up

1. Before beginning the power up test procedure, verify the connections with [Figure 1](#).
2. Enable supply #1, if the current on DMM1 is more than 0.25 mA and less than 0.71 mA, everything is set correctly.
3. Enable function generator outputs channel-A and channel-B.
4. The following conditions should be present:
 1. Stable pulse output on channel-1 and channel-2 in the oscilloscope, refer to [Figure 2](#)
 2. Frequency measurement should be 100 kHz, ± 5 kHz or equal to the programmed function generator frequency
 3. DMM #1 should display around 4.6 mA, ± 2 mA with the default load capacitance of 1.8nF. For more information about operating current, refer to [UCC2728x Datasheet](#).
5. Connect ENA_IN test point to GND test point with a Jumper. The pulse outputs on channel-1 and channel-2 will cease operation and the voltage level should be near ground.



Figure 2. Example Input and Output Waveforms (Green and Magenta are PWM Inputs, Yellow and Blue are Driver Outputs)

5.2 Power Down

Use the following steps to power down the EVM:

1. Disable function generator
2. Disable power supply #1
3. Disconnect cables and probes

6 Operation With External Bootstrap Diode

The UCC27282EVM-335 has an external bootstrap diode included, the series resistor (R10) is not populated. This allows the user to evaluate pin compatible drivers that do not have the internal bootstrap diode which is included with the UCC27282 3-A Peak High-Side and Low-Side Driver.

As a general guideline, when using the external bootstrap diode a resistance value of 2.2Ω to 10Ω is recommended. Install R10 1206 size resistor for evaluation of pin compatible drivers without the internal bootstrap diode.

7 Typical Performance Waveforms ($C_L = 1800\text{ pF}$)

7.1 Propagation Delays

The waveforms below illustrate the HI input and HO output on the top traces, and the LI input and LO output on the bottom traces in each plot.

To evaluate propagation delays and rising and falling details, it is recommended to have scope probe connections with short ground leads, see [Figure 3](#) and [Figure 4](#).

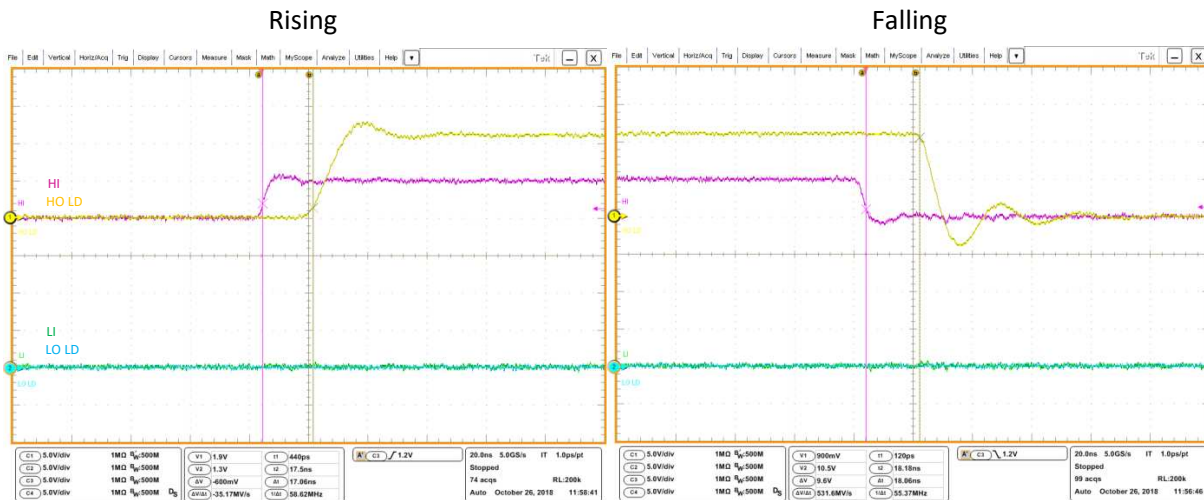


Figure 3. HI and HO Propagation Delay Waveforms (Green and Magenta are PWM Inputs, Yellow and Blue are Driver Outputs)

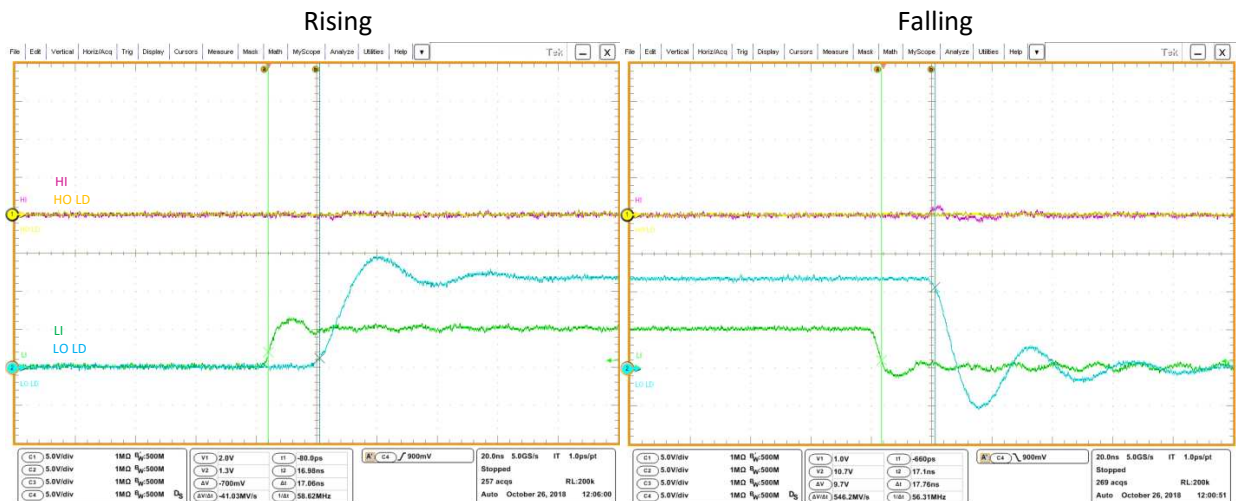


Figure 4. LI and LO Propagation Delay Waveforms (Green and Magenta are PWM Inputs, Yellow and Blue are Driver Outputs)

8 Schematic

Figure 5 shows the UCC27282EVM-335 schematic diagram.

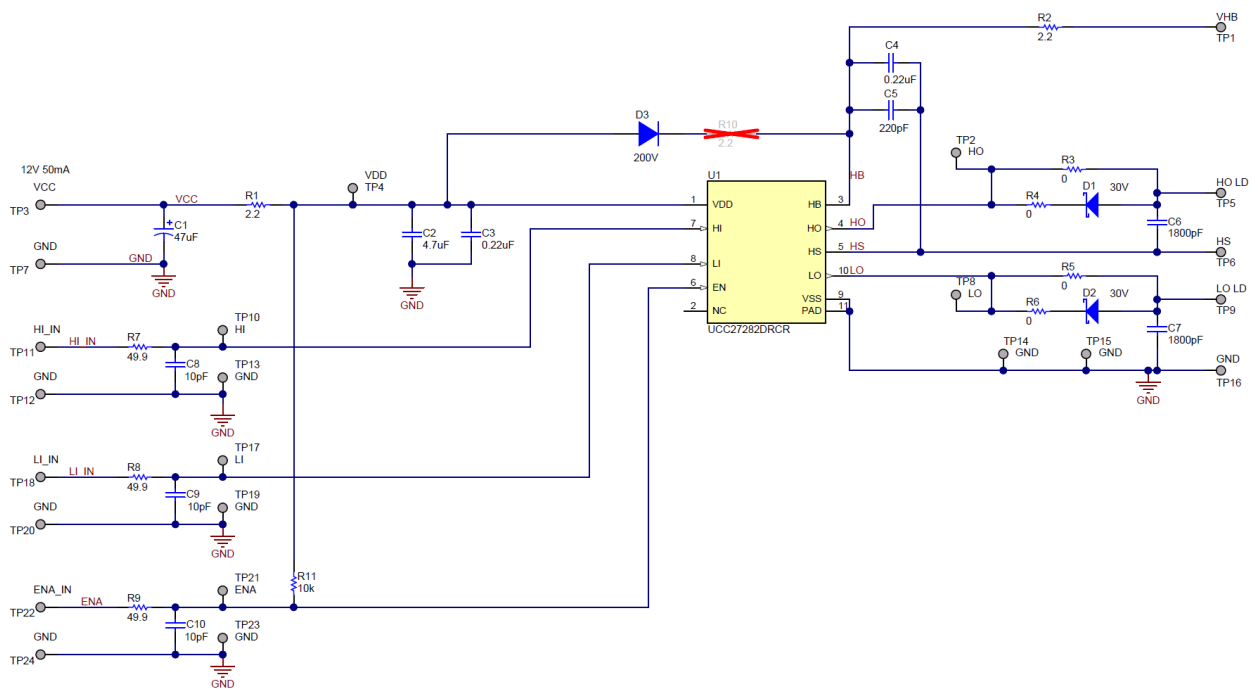


Figure 5. UCC27282EVM-335 Schematic

9 Layout Diagrams

The PCB layout information for UCC27282EVM-335 is shown in [Figure 6](#) through [Figure 9](#).

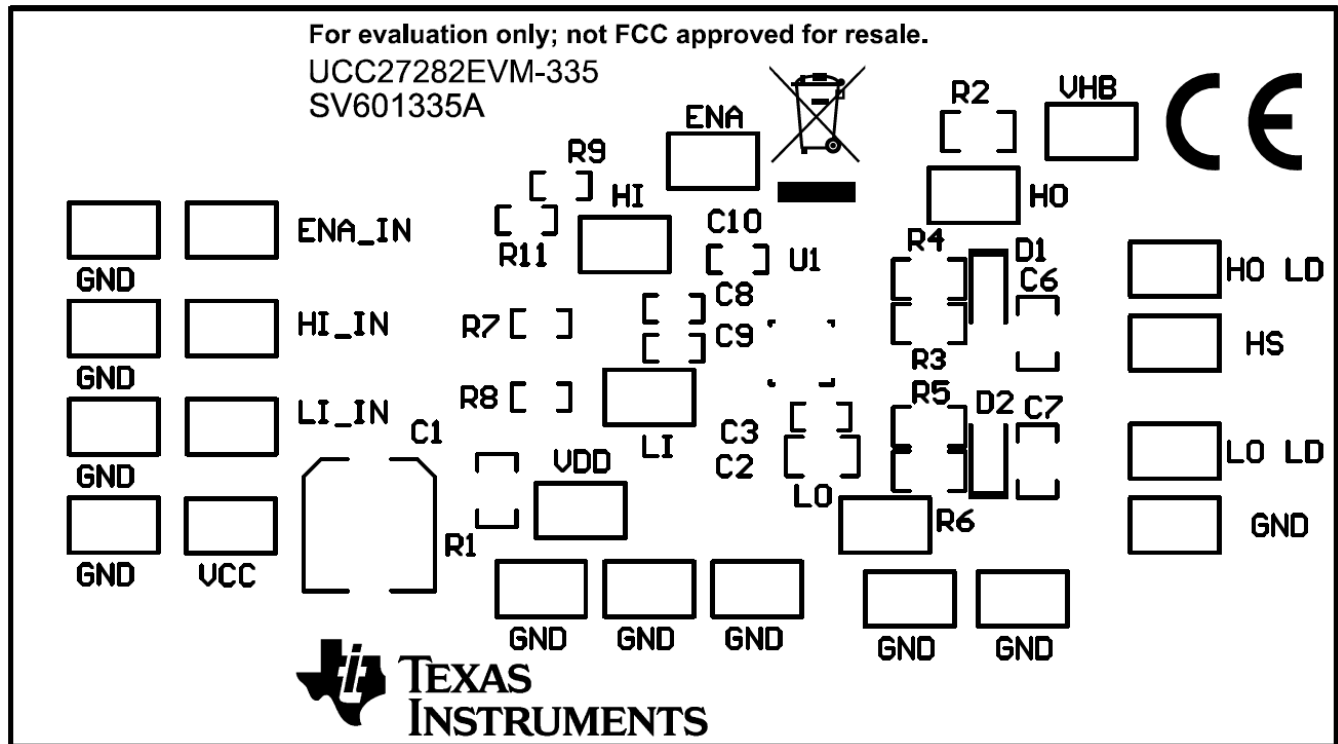


Figure 6. Top Overlay

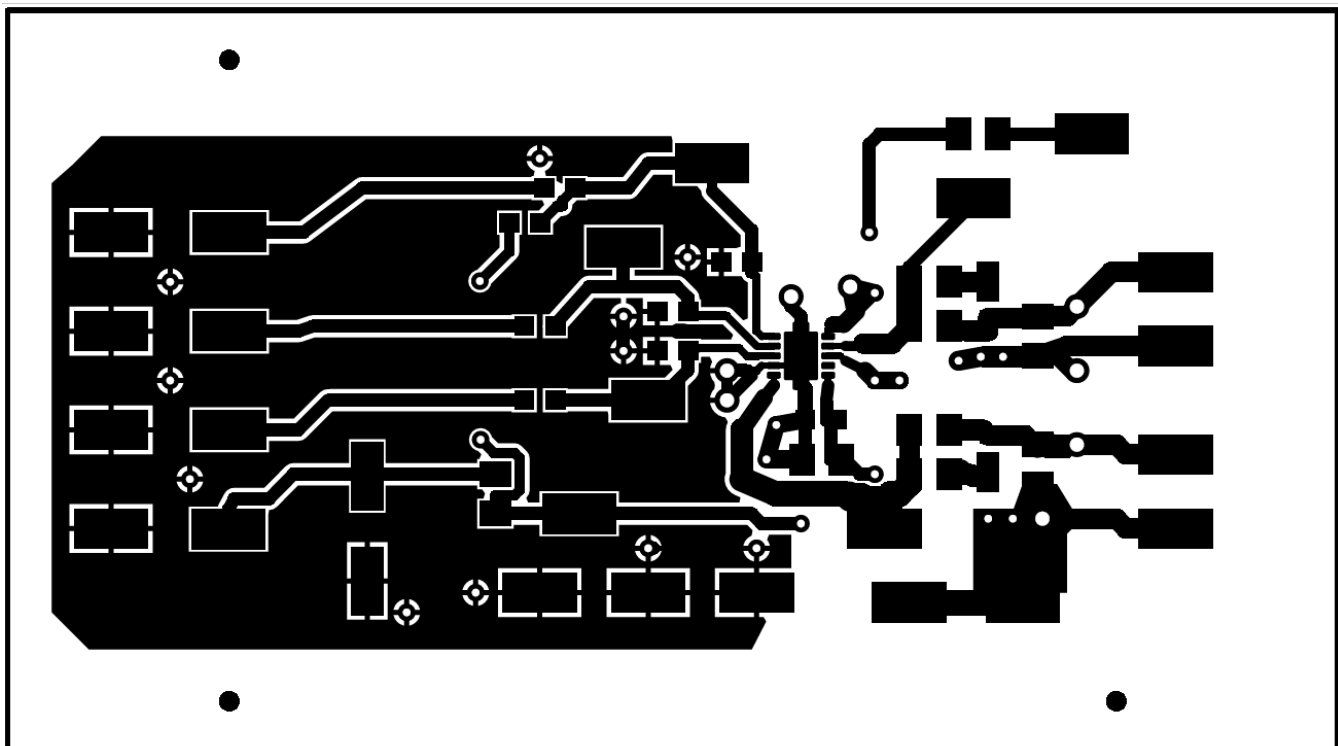


Figure 7. Top Layer

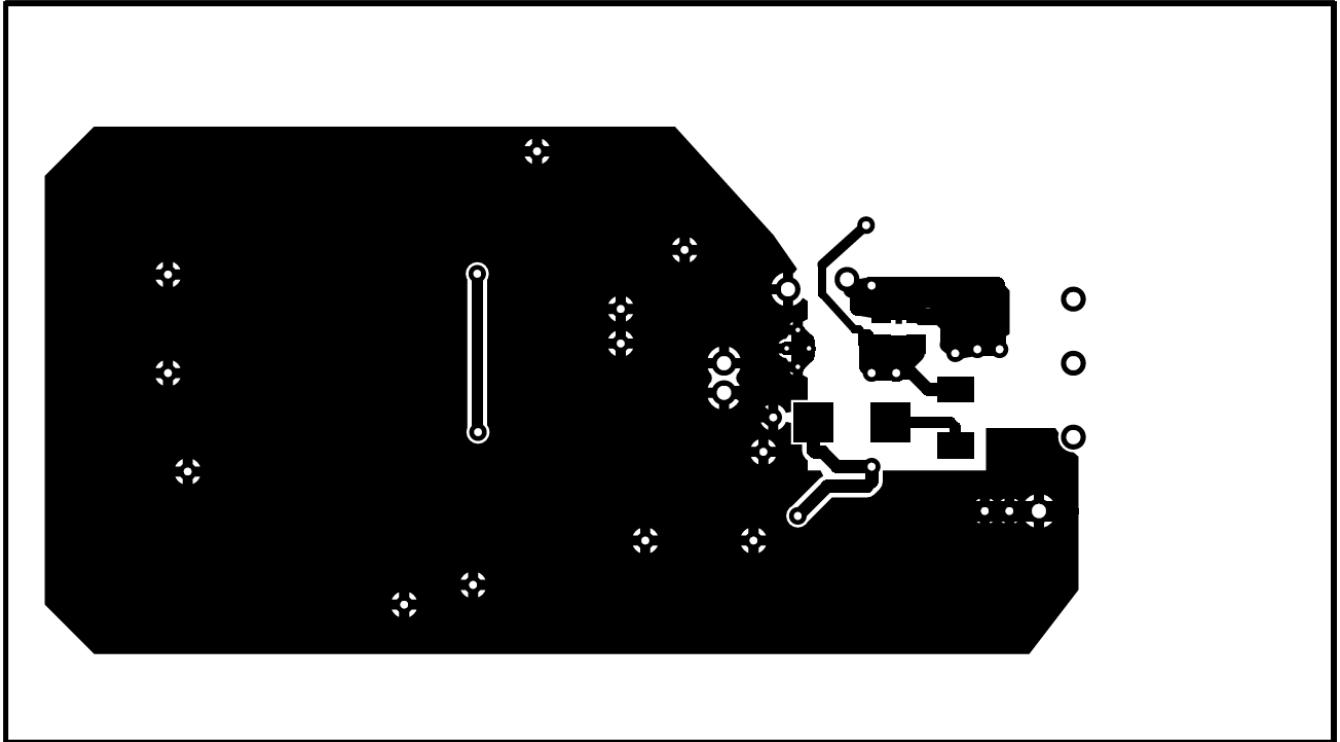


Figure 8. Bottom Layer

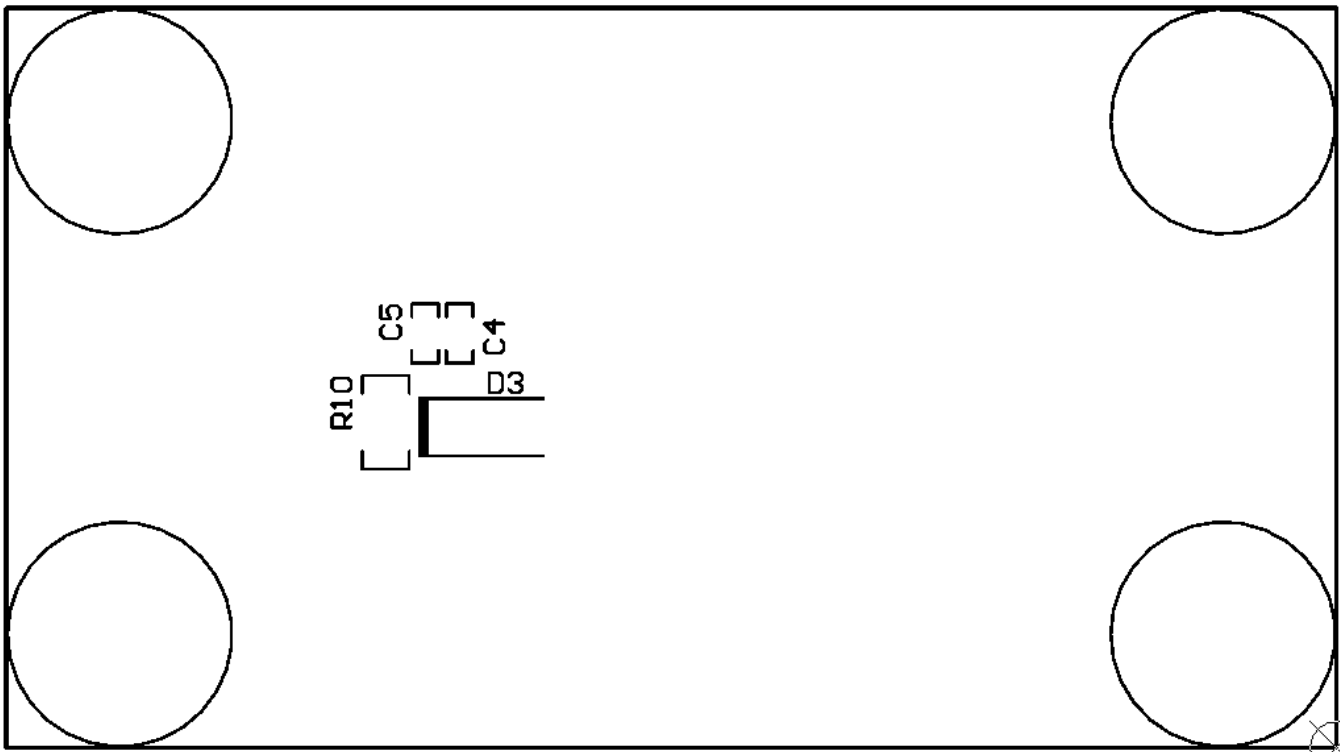


Figure 9. Bottom Overlay

10 List of Materials

Table 4 lists the UCC27282EVM-335 list of materials.

Table 4. UCC27282EVM-335 List of Materials

Item	Designator	QTY	Value	Part Number	Manufacturer	Description	Package Reference
1	C1	1	47 uF	UUD1H470MCL1GS	Nichicon	CAP, AL, 47 µF, 50 V, ±20%, 0.68 ohm, SMD	6.3x7.7
2	C2	1	4.7 uF	C2012X7R1E475K125AB	TDK	CAP, CERM, 4.7 µF, 25 V, ±10%, X7R, 0805	0805
3	C3, C4	2	0.22 uF	C1608X7R1H224K080AB	TDK	CAP, CERM, 0.22 µF, 50 V, ±10%, X7R, 0603	0603
4	C5	1	220pF	C0603C221J5GACTU	Kemet	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
5	C6, C7	2	1800 pF	08055C182KAT2A	AVX	CAP, CERM, 1800 pF, 50 V, ±10%, X7R, 0805	0805
6	C8, C9, C10	3	10 pF	C0603C100J5GACTU	Kemet	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603
7	D1, D2	2	30 V	MSS1P3L-M3/89A	Vishay-Semiconductor	Diode, Schottky, 30 V, 1 A, AEC-Q101, MicroSMP	MicroSMP
8	D3	1	200V	ES1D-13-F	Diodes Inc.	Diode, Ultrafast, 200 V, 1 A, SMA	SMA
9	H1, H2, H3, H4	4		SJ-5303 (CLEAR)	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon
10	R1, R2	2	2.2	CRCW08052R20JNEA	Vishay-Dale	RES, 2.2, 5%, 0.125 W, 0805	0805
11	R3, R4, R5, R6	4	0	ERJ-6GEY0R00V	Panasonic	RES, 0, 5%, 0.125 W, 0805	0805
12	R7, R8, R9	3	49.9	CRCW060349R9FKEA	Vishay-Dale	RES, 49.9, 1%, 0.1 W, 0603	0603
13	R11	1	10k	RC1608J103CS	Samsung Electro-Mechanics	RES, 10 k, 5%, 0.1 W, 0603	0603
14	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24	24		5019	Keystone	Test Point, Miniature, SMT	Test Point, Miniature, SMT
14	U1	1		UCC27282DRCR	Texas Instruments	120-V, 3-A Peak, 5-V UVLO, 3x3, High-Frequency, High-Side/Low-Side Driver, DRC0010J (VSON-10)	DRC0010J

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2018) to A Revision	Page
• Added UCC27282 datasheet link to updated Electrical Specifications.	3

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