User's Guide

TPSM84209 Power Module Evaluation Module User's Guide

ABSTRACT

The TPSM84209 evaluation module (EVM) is designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the TPSM84209 power module. This guide provides information on the correct usage of the EVM and an explanation of the numerous test points on the board.

Table of Contents

Trademarks

1 Description

This EVM features the TPSM84209 synchronous buck power module configured for operation with a 4.5-V to 28-V input voltage range. The output voltage can be set to one of five popular values by using a configuration jumper. The full 2.5-A output current rating of the device can be supplied by the EVM. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. A control test point is provided to control the ENABLE feature and component footprints are provided for UVLO resistors and additional input and output capacitors. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The *VIN Power* terminal block (J1) is used for connection to the host input supply and the *VOUT Power* terminal block (J2) is used for connection to the load. These terminal blocks can accept up to 16-AWG wire.

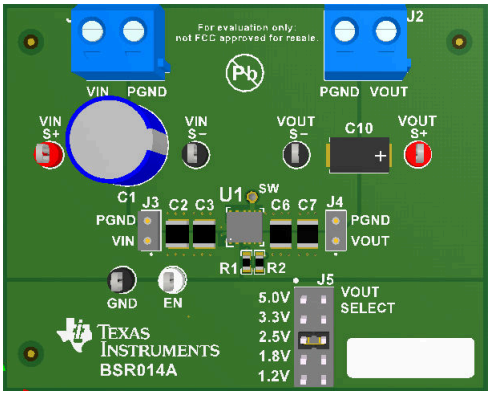


Figure 2-1. TPSM84209 EVM User Interface

The S+ and S- test points for both VIN and VOUT, located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.

The VIN Scope (J3) and VOUT Scope (J4) test points can be used to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. The scope probe tip must be inserted into the socket marked with a white dot, and the scope ground lead must be inserted into the other socket.

The Enable (EN) and ground (GND) test points located to the left of the device are made available to enable or disable the device. Leaving the EN test point floating enables the device when a valid input voltage is applied, while connecting EN to GND disables the device. Refer to the Test Points Descriptions section of this guide for more information on the individual control test points.

The VOUT SELECT jumper (J5) is provided for selecting the desired output voltage. Before applying power to the EVM, ensure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper setting.

3 Test Point Descriptions

Wire-loop test points and two scope probe test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point follows:

Table 3-1. Test Point Descriptions(1)

VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
VIN S–	Input voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
VOUT S+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
VOUT S–	Output voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
AGND	Analog ground test point.
VIN Scope (J3)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT Scope (J4)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
EN	Enable test point. Connect this test point to AGND to disable the device. Leave this test point open to enable the device.The UVLO resistor divider (R9 and R10) is connected at this point.

(1) Refer to the TPSM84209 datasheet for absolute maximum ratings associated with above features.

4 Performance Data

Figure 4-1 through Transient Performance demonstrate the TPSM84209EVM performance. For more data regarding the TPSM84209 please see the product data sheet.

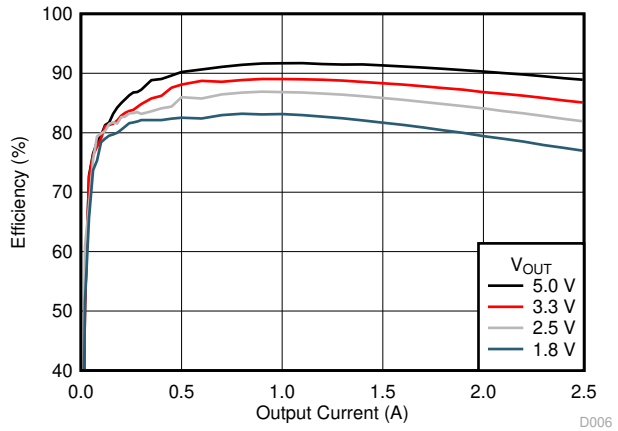


Figure 4-1. Efficiency (V_{IN} = 12 V)

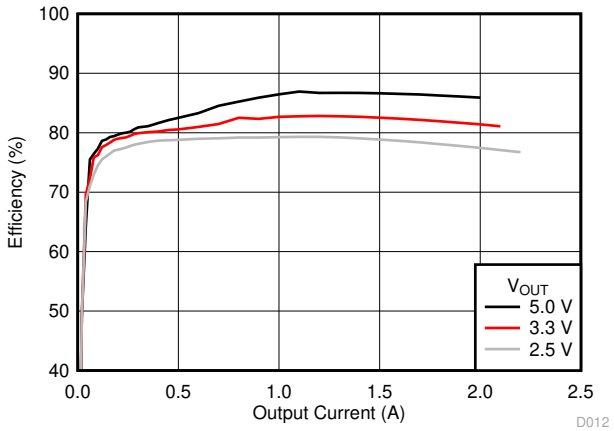


Figure 4-2. Efficiency (V_{IN} = 24 V)

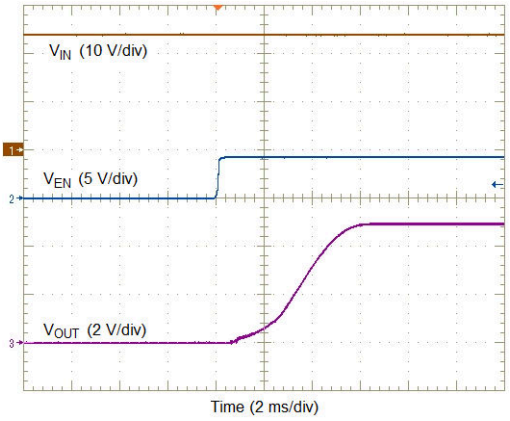


Figure 4-3. EN Start-Up Waveforms

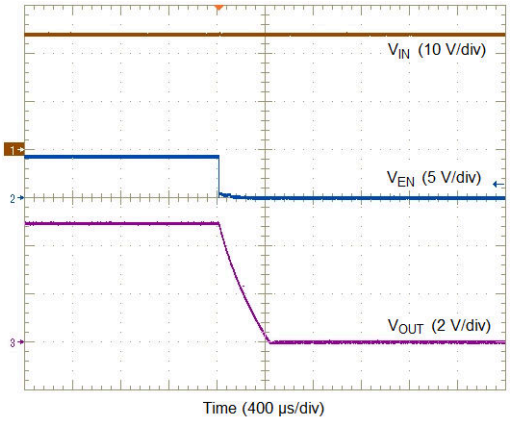
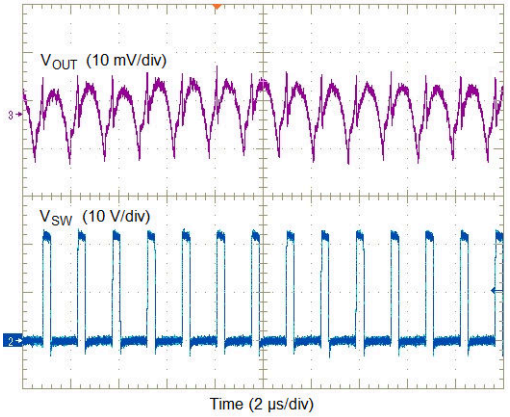
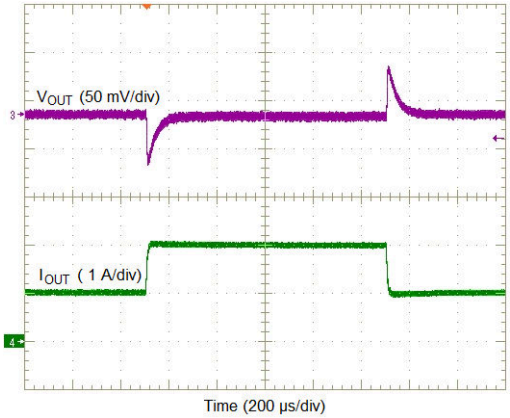


Figure 4-4. EN Shutdown Waveforms



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 4-5. Output Ripple and SW Node



V_{IN} = 12 V V_{OUT} = 1.8 V

Figure 4-6. Transient Performance

5 Bill of Materials (BOM)

See Table 5-1 for the TPSM84209 bill of materials.

Table 5-1. EVM Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C2, C3	2	10µF	CAP, CERM, 10 µF, 50 V,+/- 10%, X5R, 1210	1210	GRM32ER61H106KA12L	MuRata
C6, C6	2	47µF	CAP, CERM, 47 µF, 10 V,+/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
J1, J2	2		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J3, J4	2		Socket Strip, 2x1, 100mil, Black, Tin, TH	Socket Strip, 100mil, 2pin	310-43-102-41-001000	Mill-Max
J5	1		Header, 100mil, 5x2, Tin, TH	Header, 5x2, 100mil, Tin	PEC05DAAN	Sullins Connector Solutions
R1, R3	2	14.7k	RES, 14.7 k, 1%, 0.1 W, 0603	0603	CRCW060314K7FKEA	Vishay-Dale
R4	1	7.32k	RES, 7.32 k, 1%, 0.1 W, 0603	0603	CRCW06037K32FKEA	Vishay-Dale
R5	1	4.64k	RES, 4.64 k, 1%, 0.1 W, 0603	0603	CRCW06034K64FKEA	Vishay-Dale
R6	1	3.24k	RES, 3.24 k, 1%, 0.1 W, 0603	0603	CRCW06033K24FKEA	Vishay-Dale
R7	1	2.00k	RES, 2.00 k, 1%, 0.1 W, 0603	0603	CRCW06032K00FKEA	Vishay-Dale
R8	1	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
SH-J1,	1	1x2	Shunt, 2mm, Gold plated, Black	2mm Shunt, Closed Top	2SN-BK-G	Samtec
TP1, TP3	2		Test Point, Multipurpose, Red, TH	Multipurpose Testpoint Red	5010	Keystone
TP2	1		Test Point, Multipurpose, White, TH	Multipurpose Testpoint White	5012	Keystone
TP5, TP6, TP7	3		Test Point, Multipurpose, Black, TH	Multipurpose Testpoint Black	5011	Keystone
U1	1		4.5V to 28V Input, 1.2V to 6.0V Output, 2.5A	RKH0009A	TPSM84209RKH	Texas Instruments
C1	0		CAP, ALUM, TH	10x16mm		
C4	0		CAP, CERM, 1210	1210		
C5	0		CAP, CERM, 0603	0603		
C8, C9	0		CAP, CERM, 1210	1210		
C10	0		CAP, Tantalum Polymer, 7343-40 SMD	7343-40		
C11	0		CAP, CERM, 0603	0603		
R2, R9, R10	0		RES, 0.1 W, 0603	0603		

6 Schematic

Figure 6-1 is the schematic for the TPSM84209EVM.

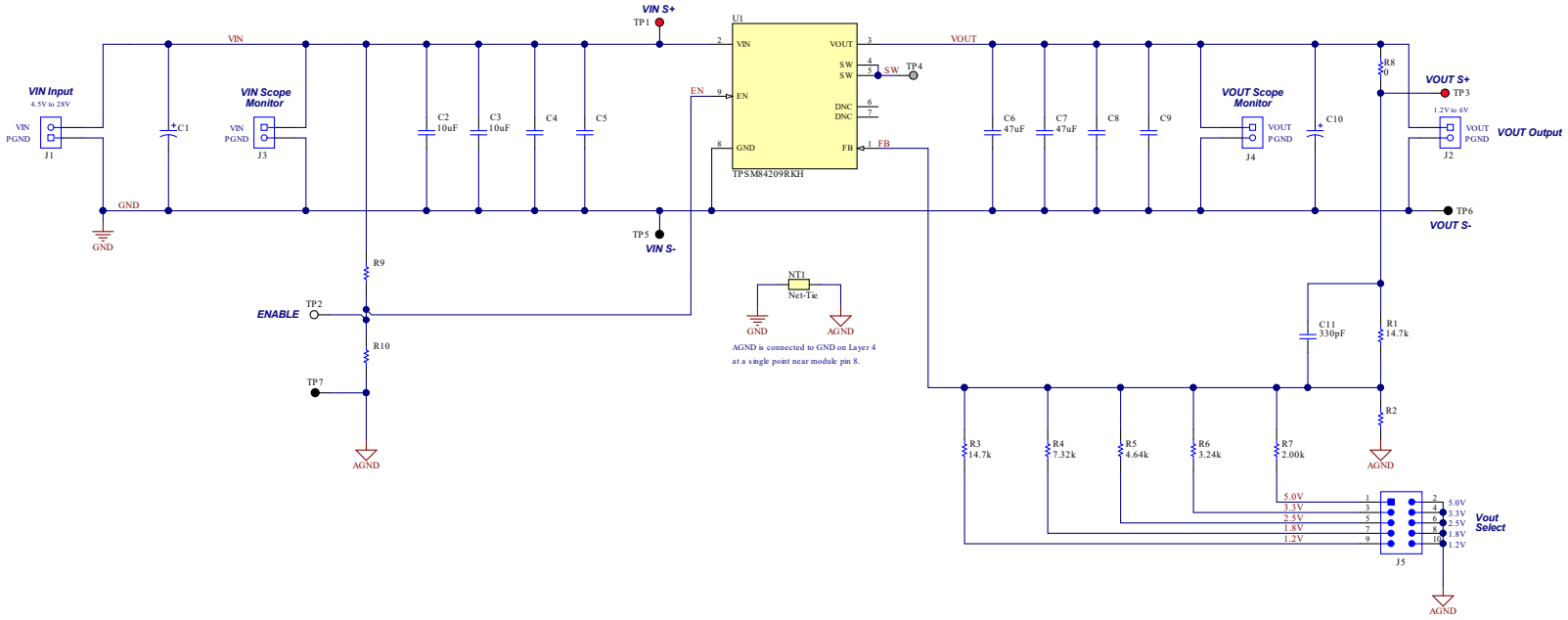


Figure 6-1. TPSM84209EVM Schematic

7 PCB Layout

Figure 7-1 through Figure 7-6 show the PCB layers of the TPSM84209EVM.

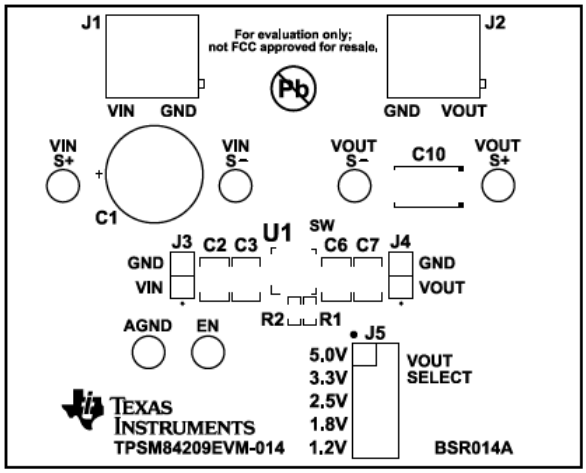


Figure 7-1. Topside Component Layout (Top View)

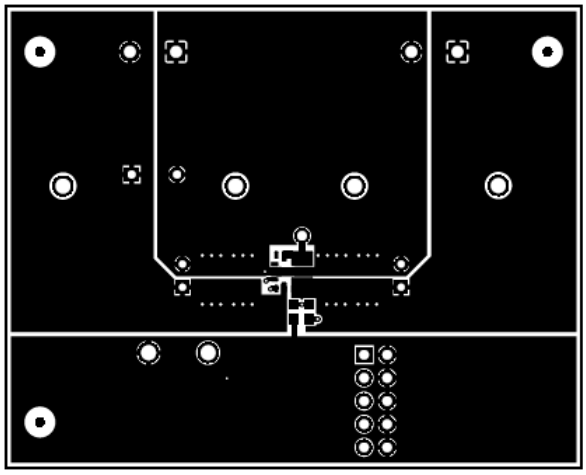


Figure 7-2. Topside Copper (Top View)

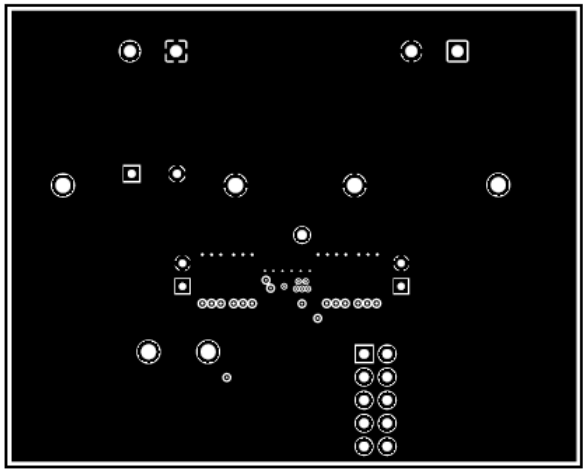


Figure 7-3. Layer 2 Copper (Top View)

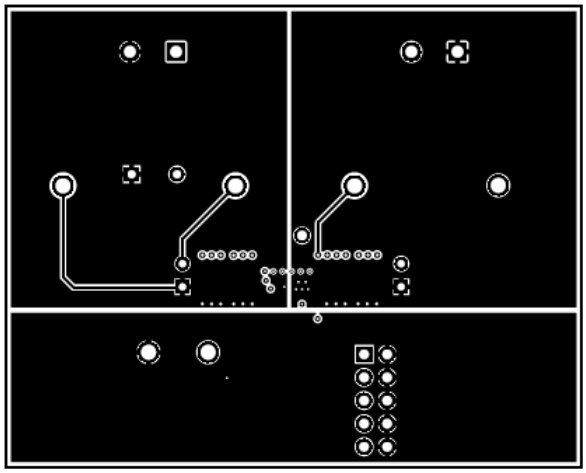


Figure 7-4. Layer 3 Copper (Top View)

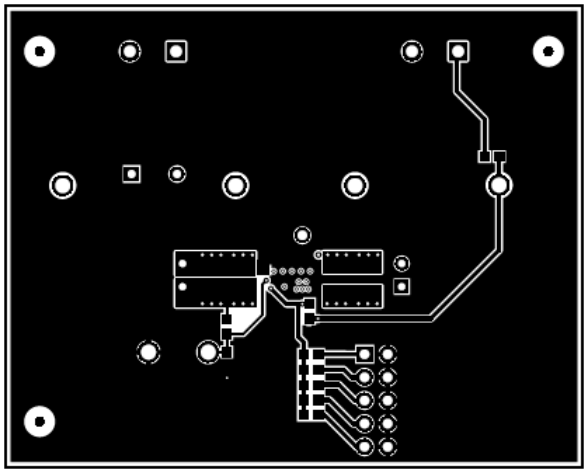


Figure 7-5. Bottom-Side Copper (Top View)

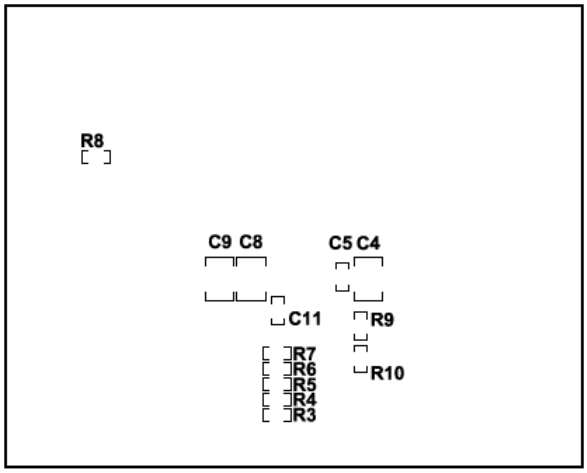


Figure 7-6. Bottom-Side Component Layout (Bottom View)

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2018) to Revision A (June 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

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