

TPS62866EVM-051 Evaluation Module

The TPS62866EVM-051 facilitates the evaluation of the TPS62866 6-A, step-down converter with DCS-Control™ in a tiny 1.05-mm by 1.78-mm WCSP package with 0.35-mm pitch. The EVM outputs a 0.9-V output voltage with 1% accuracy from input voltages between 2.4 V and 5.5 V. The TPS62866 is a highly efficient and tiny solution for point-of-load (POL) converters for space-constrained applications, such as artificial intelligence chips, camera modules, solid state drives (SSDs), and optical modules.

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1 Introduction

The TPS62866 is a synchronous, step-down converter in a 1.05- x 1.78- x 0.5-mm wafer chip-scale package (WCSP).

1.1 Performance Specification

Table 1 provides a summary of the TPS62866EVM-051 performance specifications.

Table 1. Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.4	5	5.5	V
Output voltage setpoint			0.9		V
Output current		0		6000	mA

1.2 Modifications

The EVM can support variance of the whole IC family. Additional input and output capacitors can be added.

2 Setup

This section describes how to properly use the TPS62866EVM-051.

2.1 Input/Output Connector Descriptions

J1, Pin 1 and 2 – VIN	Positive input connection from the input supply for the EVM
J1, Pin 3 and 4 – S+/S-	Input voltage sense connections. Measure the input voltage at this point.
J1, Pin 5 and 6 – GND	Input return connection from the input supply for the EVM
J2, Pin 1 and 2 – VOUT	Output voltage connection
J2, Pin 3 and 4 – S+/S-	Output voltage sense connections. Measure the output voltage at this point.
J2, Pin 5 and 6 – GND	Output return connection
J3, Pin 5 – VBUS	The VBUS pin of this header is used to bias the SCL and SDA nodes of I ² C interface via a resistor.
J3, Pin 6 – GND	The GND pin of this header is used to connect the grounds of the IC and the I ² C interface.
J3, Pin 9 – SCL	The pin of this header should be connected to the SCL of the I ² C interface.
J3, Pin 10 – SDA	The pin of this header should be connected to the SDA of the I ² C interface.
JP1 – VID/PG	VID/ $\overline{\text{PG}}$ pin jumper. Always place the jumper across VID/ $\overline{\text{PG}}$ and LOW pins before start-up. This sets the output voltage and device address. After startup, VOUT reflects the value set on V _{OUT} Register 1 if the jumper is placed across VID/ $\overline{\text{PG}}$ and LOW pins. VOUT follows the value set on V _{OUT} Register 2 if the jumper is placed across VID/ $\overline{\text{PG}}$ and HIGH pins.
JP2 – EN	EN pin input jumper. Place the jumper across ON and EN to turn on the IC. Place the jumper across OFF and EN to turn off the IC.

2.2 Setup

To operate the EVM, set jumpers JP1 and JP2 to the desired position per Section 2.1. Connect the input supply to J1 and connect the load to J2.

3 TPS62866EVM-051 Test Results

The TPS62866EVM-051 was used to take all the data in the TPS62866 data sheet ([SLVSE11](#)). See the device data sheet for the performance of this EVM.

4 Board Layout

This section provides the TPS62866EVM-051 board layout and illustrations in [Figure 1](#) through [Figure 7](#). The Gerbers are available on the EVM product page: [TPS62866EVM-051](#)

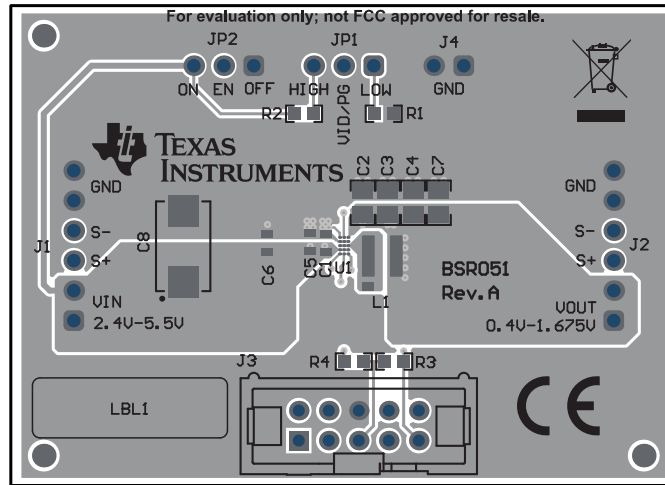


Figure 1. Top Assembly

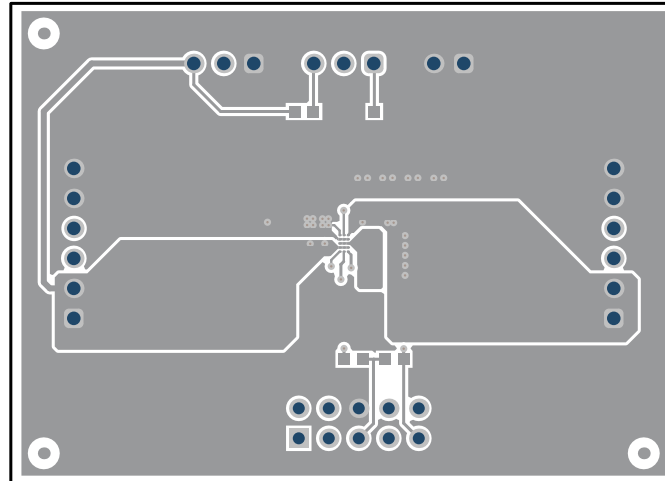


Figure 2. Top Layer

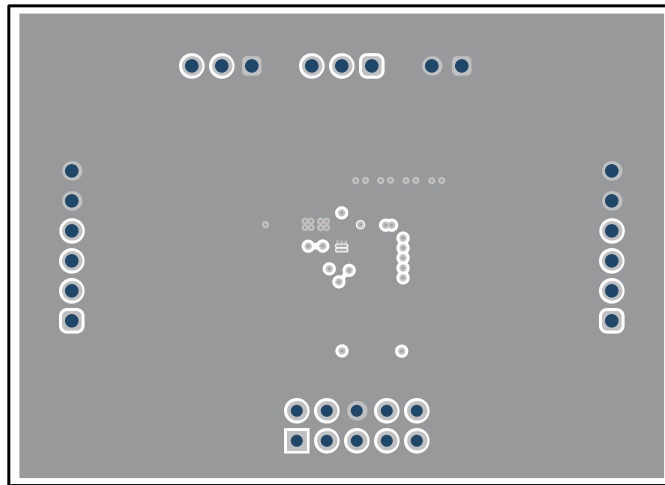


Figure 3. Signal Layer 1

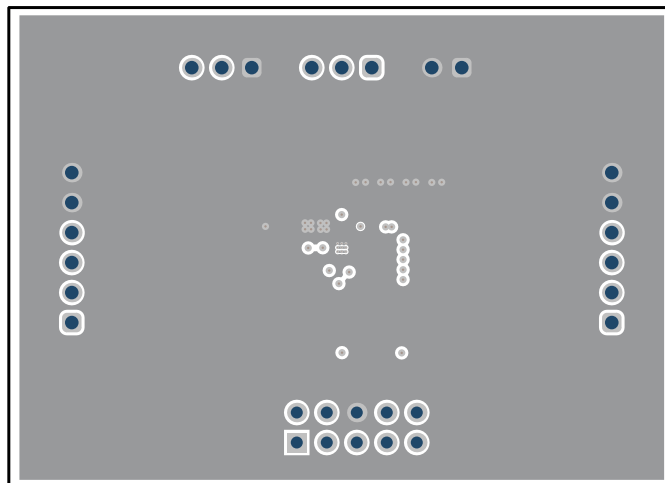


Figure 4. Signal Layer 2

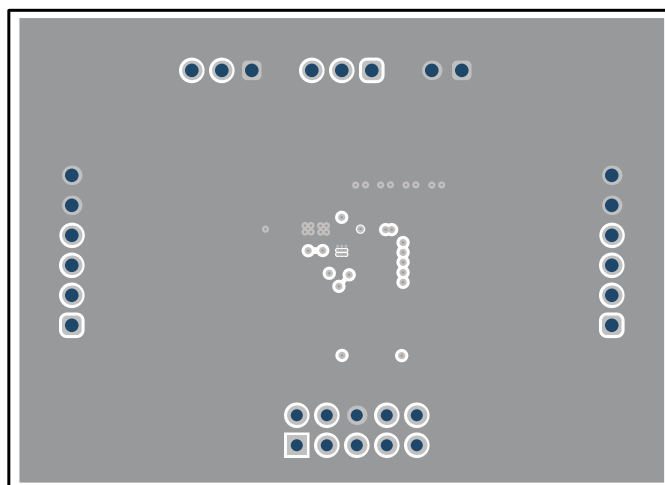


Figure 5. Signal Layer 3

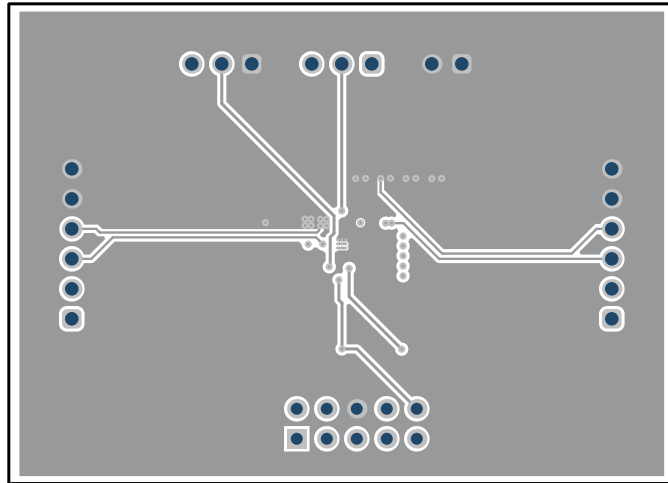


Figure 6. Signal Layer 4

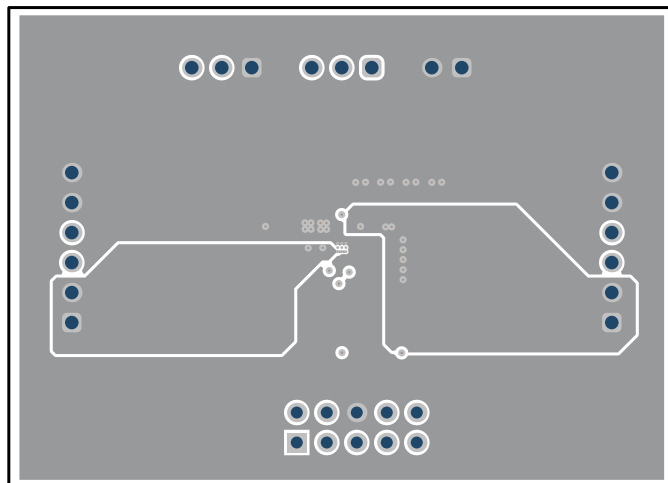


Figure 7. Bottom Layer



Figure 8. TPS62866EVM-051 Angled View



Figure 9. TPS62866EVM-051 Overhead View

5 Schematic and List of Materials

This section provides the TPS62866EVM-051 schematic and list of materials.

5.1 Schematic

Figure 10 illustrates the EVM schematic.

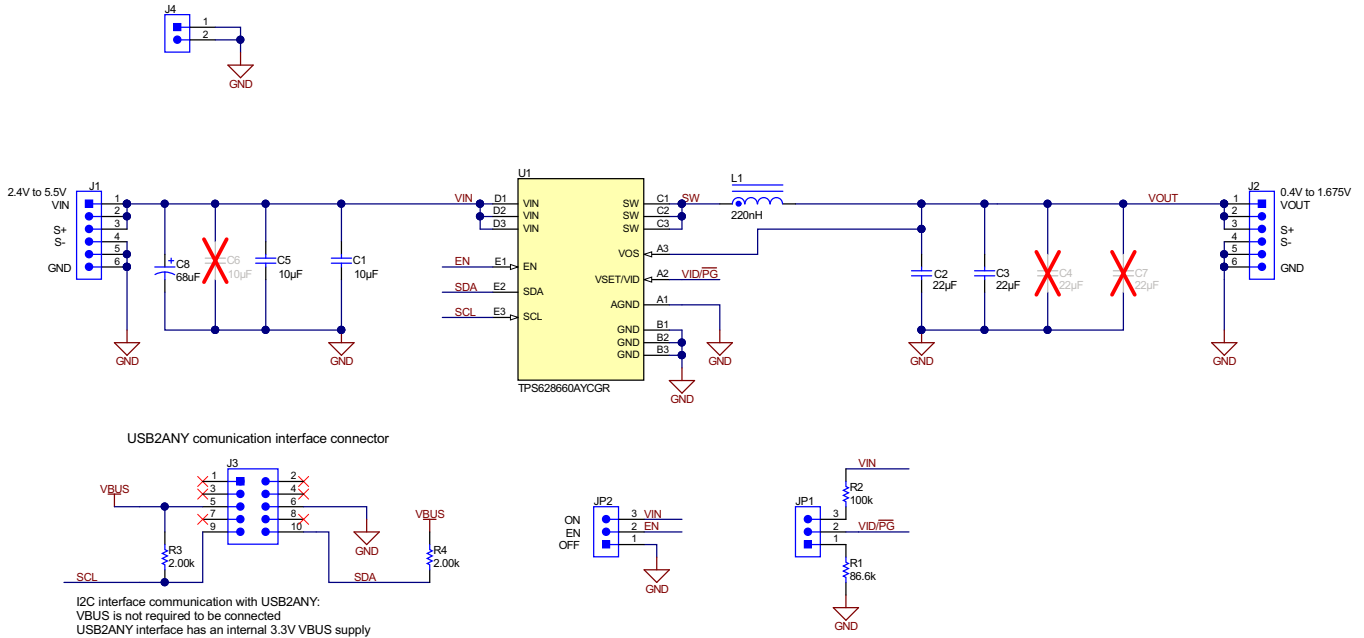


Figure 10. TPS62866EVM-051 Schematic

5.2 List of Materials

Table 2 lists a list of materials for this EVM.

Table 2. TPS62866EVM-051 List of Materials

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C1, C5	2	Capacitor, ceramic, 10 µF, 6.3 V, ±20%, X7R, 0603	CL10B106MQ8NRNC	Samsung Electro-Mechanics
C2, C3	2	Capacitor, ceramic, 22 µF, 6.3 V, ±20%, X7R, 0805	GRM21BZ70J226ME44L	Murata
C8	1	Capacitor, tantalum, 68 µF, 20 V, ±10%, 7343	T495D686K020ATE150	Kemet
L1	1	Inductor, 220 nH, 16.8 A, 5.8 mΩ, SMD, 4040	XAL4020-221MEB	Coilcraft
R1	1	Resistor, 86.6 kΩ, 1%, 0.1 W, 0603	Std	Std
R2	1	Resistor, 100 kΩ, 1%, 0.1 W, 0603	Std	Std
R3, R4	2	Resistor, 2.0 kΩ, 1%, 0.1 W, 0603	Std	Std
U1	1	6-A Step-Down Converter with I ² C Interface and Wide Output Voltage Range, YCG0015ACAC (DSBGA-15)	TPS628660AYCGT	Texas Instruments

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

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NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

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