User's Guide **BQ76952 Evaluation Module**

TEXAS INSTRUMENTS

Matt Sunna

ABSTRACT

The BQ76952EVM evaluation module (EVM) is a complete evaluation system for the BQ76952, a 3-cell to 16cell Li-Ion battery monitor integrated circuit. The EVM consists of a BQ76952 circuit module which is used for simple evaluation of the BQ76952 monitor function. The circuit module includes one BQ76952 integrated circuit (IC), sense resistor, thermistors, power FETs, and all other onboard components necessary to protect the cells from overcharge, over discharge, short circuit, overcurrent discharge, over temperature and under temperature in a 16-series cell Li-Ion or Li-Polymer battery pack. The circuit module connects directly across the cells in a battery, or can be connected with a power supply and the included cell simulator resistors. With the on-board interface or compatible external interface board and Microsoft[®] Windows[®] based PC graphical user interface (GUI) software, the user can view the device registers, evaluate voltage, current and temperature accuracy, perform calibration, adjust protection limits and enable FET control outputs.

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1 Features

- Complete evaluation system for the BQ76952 3-cell to 16-cell Li-Ion and Phosphate battery monitor
- Populated circuit module for 16-cell configuration for quick setup
- Power connections available on test points
- · Communication available with included USB interface adapter or available on 4-pin connector
- Resistor cell simulator for quick setup with only a power supply
- PC software available for configuration

1.1 Kit Contents

- BQ76952 circuit module
- USB cable

1.2 Ordering Information

For complete ordering information, refer to the product folder at www.ti.com.

Table 1-1. Ordering Information

| EVM Part Number | Chemistry | Configuration | Capacity |
|-----------------|-----------|---------------|----------|
| BQ76952EVM | Li-Ion | 16 cells | Any |
| | | | |

Note

Although capacity is shown as *Any*, practical limits of the physical construction of the module typically limits the operation of the EVM to a 1P or 2P battery construction. Refer to the physical construction section for board details.

1.3 BQ76952 Circuit Module Performance Specification Summary

This section summarizes the performance specifications of the BQ76952 circuit module in its default 16-cell series FET configuration.

Typical voltage depends on the number of cells configured. Typical current depends on the application. Board cooling may be required for continuous operation at or below maximum current.

Table 1-2. Performance Specification Summary

| Specification | Min | Тур | Max | Unit |
|---|-----|-----|-----|------|
| Input voltage BATT+ with respect to BATT- | 6 | - | 72 | V |
| Continuous charge or discharge current | 0 | - | 6 | А |
| Operating temperature range | 20 | 25 | 30 | °C |

1.4 Required Equipment

The following equipment is required to operate the BQ76952 EVM in a simple demonstration:

- DC power supply, 0–80 V at 2.5 A
- DC voltmeter
- · Computer with USB port and compatible Windows operating system and access to the internet
- Test leads to connect equipment
- Electronic load or assorted resistors

Additional equipment may be desired to operate the BQ76952 with a more extensive demonstration.

2 BQ76952 EVM Quick Start Guide

2.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the BQ76952 EVM. Observe all safety precautions.

| | Warning | The BQ76952EVM circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory. |
|----------|---------|---|
| Â | Warning | The bq76952EVM is not rated as a high voltage EVM, has smaller clearances than normally used on high voltage boards and does not have an isolation boundary. If you apply high voltage to this board, all terminals should be considered high voltage. Electric shock is possible when connecting the board to live wire. The board should be handled with care by a professional. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended. |
| \wedge | Caution | Do not leave the EVM powered when unattended. |

CAUTION

The default settings of the BQ76952 do not limit performance to the ratings of the EVM. Set all protections appropriately and limit current for safe operation.

CAUTION

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment. Do not operate beyond the current and voltage limits in the Sepcification Table.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the Battery- potential of the EVM.

CAUTION

Connections for rated current must be made at the terminal block. Test points are not rated for the board current.



2.2 Quick Start

The BQ76952 registers must be configured to enable most protections, select the monitored cells, and enable the protection FETs on the EVM. This quick start section does not describe current protection settings. Once all registers are configured, the values may be written to One Time Programmable memory (OTP) for use on the next reset of the device, but since that is a permanent change it is not part of this quick start procedure. This quick start assumes a new EVM without OTP configuration settings. If your board has a part with configuration stored in OTP refer to Section 3 and Section 4.

These steps describe quick connection of the BQ76952 EVM to demonstrate operation of the AFE portion of the EVM. For more detailed descriptions, refer to other sections of the user guide.

Refer to Figure 2-1 for the following steps.

- 1. Download the BQSTUDIO Software from the tool folder link www.ti.com/tool/BQSTUDIO or search from www.ti.com.
- 2. Install the BQStudio software (see Section 3.2).
- 3. Install the cell simulator shunts.
- 4. Position shunts to uC_SCL and uC_SDA.
- 5. Attach the on board communication adapter USB connector to the PC using USB cable.
- 6. Connect a 0-V DC power supply capable of 250 mA minimum between the "*BAT-*" and "*CELL16*" terminals and adjust to approximately 48 V.
- 7. Press and release the WAKE switch.
- 8. Start the BQStudio software. The GUI should open with a register display. Click on the *Scan* button to enable repeated update of the display. The power supply may be adjusted within range of the part to observe voltage changes in the GUI register display.
- 9. Select the Data Memory button in the BQStudio window.
- 10.Select the Settings button. Set the Enabled Protections A CUV bit
- 11. In the Commands panel click on the FET_EN button.
- 12.In the Registers view click on the Scan icon so that the registers update periodically. Observe that the CHG_FET and DSG_FET bits in the FET Status register are on and that the Stack voltage and the PACK pin voltage registers are approximately equal. Measure the PACK voltage on the board if desired.
- 13.Adjust the supply voltage to approximately 38 V. In the registers view observe that the DSG_FET bit goes off and the PACK voltage drops to approximately 0 V.
- 14.Make other adjustments as desired for evaluation. See other sections of this user guide for details of operation.
- 15. When complete with this quick start demonstration, exit the BQStudio software and turn off the power supply.

Refer to other sections of this user guide for additional details.





Figure 2-1. EVM Connection for Basic Operation



3 Battery Management Studio Software

The Battery Management Studio software is used for evaluation of the BQ769x2 monitor. It is also identified as BQStudio for a compact name. If an earlier version of the BQStudio software is already installed from another product evaluation, it should still be installed again to load the configuration files and tools specific to the current version of the BQ76952.

3.1 System Requirements

The BQStudio software requires a Windows 7, or later, operating system. Additional items are required and are described in the installation windows.

3.2 Installing BQStudio

Find the latest software version in the software section of the product folder http://www.ti.com/tool/BQSTUDIO or search from ti.com. There are multiple versions available and the BQSTUDIO-TEST version should be used with the BQ76952 EVM. Check periodically for software updates. Use the following steps to install the BQStudio software:

- 1. Uninstall older versions of BQStudio software. After uninstalling, delete the BatteryManagmentStudio program directory.
- 2. Copy the archive file to a directory of your choice, extract all files and run the *Battery Management Studio-xxxxxx-Setup.exe* application.
- 3. Follow the instructions and make selections as required on the setup windows selecting **Next**, as required. TI recommends installing the software in the default location.
- 4. On the last window select option check-boxes desired and **Finish** to complete the BQStudio software installation.

3.3 BQ769x2 bqz File Installation

The BQStudio software uses a bqz file to configure the displays for the BQ769x2 device family or specific family device. This is normally provided in the BQStudio installation. If provided separately, copy the .bqz file to the config directory in the installation, typically C:\ti\BatteryManagementStudio\config.

3.4 BQStudio Operation and Registers View

BQStudio is used to communicate to the BQ769x2 for evaluation. It includes several tools to aid in configuration, calibration and data display of the BQ769x2 during evaluation.

Although the software runs without connection to an interface board or powered device, it is recommended to have both connected and the device on when starting the software. Follow the directions in the Quick Start section. Figure 2-1 shows typical connections for operation with the BQStudio software.

Start the software from the desktop shortcut Battery Management Studio or the from the Start menu.

When started, the software looks for the communication interface and the device. If the device is not found, it opens a Target Selection Wizard. On the first window select the Monitor or All class and click the *Next* button. On the second window select the newest or appropriate BQ769x2 version in the list and click the **Finish** button. This selection will be remembered until the software is re-stared. If the device is not found, the user will be presented with a *Proceed*? window which must be acknowledged. If the software still can not find the device, a *Battery Management Studio* popup window appears indicating communication status. Acknowledge the message to proceed.

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Battery Management Studio Software



www.ti.com

| Target Selection Wizard | | 23 |
|--|-------------------------|---------------|
| Please select a target | | |
| Monitor_7692_0_11-bq76922.bqz Monitor_7693_0_11-bq76932.bqz Monitor_7694_0_11-bq76942.bqz Monitor_7695_0_11-bq76952.bqz | | |
| Auto Detected Device : None | | |
| If the type of device is not in the list above, you may download the latest version of bqStudio at <u>http://www</u> (new versions add support for newer devices) | <u>v.ti.com/tool/bq</u> | <u>studio</u> |
| <back next=""> Finish</back> | Canc | el |

Figure 3-1. Target Selection Wizard

If the software was started without a communication interface adapter, a Battery Management Studio popup window will indicate a free adapter is not available. Acknowledge the message to proceed. Errors will appear in the left bottom border of the Battery Management Studio screen. Correct the problem with the adapter and restart the software.

BQStudio contains a user guide for general operation of the software. Refer to the menu selection Help | Help Contents for information.

The BQStudio window appears as shown in Figure 3-2. The register area is blank since the device is not attached.

The center pane of BQStudio displays tool tips when the cursor is held over an item name. The tool tip provides some description of the item. The tool tip closes after approximately 30 seconds. To avoid the tool tip display move the cursor to the value or units column, or to the Dashboard pane.



| | | | | | | | | | | | | 1 . | | |
|---|-----------------|--|---|--|--|---|---|--|--|--|---|--|--|--------------------|
| Registers 🛛 | | | | | | | | | | | | Comman | ds 🖾 | - |
| Registers | | | | | | | | | P | 🔟 🗸 🕅 | 2 | Comman | nds | |
| | | | | | | | | | Parameter view | start Log Sc | an Kerresh | 2 DD4 | | |
| Registers Basic Para | eters Displayed | | | | | | | | | | | The second secon | ICE_NOMBER | |
| | | | | | | | | | | | | 🥏 FV | V_VERSION | |
| Name | Value | Units | Name | Value | Units | Name | Value | Units | Name | Value | Units | 🔮 F | W_BUILD | |
| Cel 1 Votage | | m∨ | Cell 9 Voltage | | mV | DFETOFF Temperature | | *C | Cel Temperature | | °C | A 10 | ALVERGION . | |
| Cell 2 Voltage | | m∨ | Cell 10 Votage | | mV | ALERT Temperature | | *C | FET Temperature | | °C | ¥ 14 | VERSION | |
| Cell 3 Voltage | | m∨ | Stack Voltage | | userV | TS1 Temperature | | •c | CC3 Current | | userA | 🗇 I | ROM_SIG | |
| Cel 4 Votage | | mV m)/ | PACK Pin Voltage | | userV | TS2 Temperature | | *C | CC1 Current | | userA | 🖉 STA | TIC CEG SIG | |
| Cell 6 Votage | | mV | CC2 O great | | userA | HDQ Temperature | | -r | Accum Time | | e | - | | |
| Cel 7 Votage | | m∨ | Int Temperature | | *C | DCHG Temperature | | *Č | Cell Balancing Active Cells | | _ | 2 C | DROM_SIG | |
| Cell 8 Voltage | | m∀ | CFETOFF Temperature | | •c | DDSG Temperature | | *C | Cell Balancing Present Time | | 8 | 🛷 EXIT | T_DEEPSLEEP | |
| | | | | | | | | | | | | × 0 | EEPSLEEP | |
| | | | | | | | | | | | | 🛷 Sł | HUTDOWN | |
| | | | | | | | | | | | | | RESET | |
| | | | | | | | | | | | | æ 1 | PDSGTEST | |
| | | | | | | | | | | | | 🛷 FU | ISE_TOGGLE | |
| | | | | | | | | | | | | 🛷 P | CHGTEST | |
| | | | | | | | | | | | | | CHGTEST | |
| | | | | | | | | | | | | | | |
| Bit Registers | | | | | | | | | | Bit High Bit L | ow RSVD | | DSGTEST | |
| Bit Registers None | Value | B#7 | Bit6 | BtS | | Bt4 | Bt3 | Bt | 2 Bt1 | Bit High Bit L Bit0 | ow RSVD | e FE | DSGTEST ET_ENABLE | |
| Bit Registers | Value | Bt7 RSVD_0 | Bts RSVD_0 | Bt5 RSVD_ |) | Bt4 RSVD_0 F | Bt3 SVD_0 | Bt | 2 Bt1 D_0 RSVD_0 | Bit High Bit L Bit0 RSVD | ow RSVD | P | DSGTEST ET_ENABLE F_ENABLE | |
| Bit Registers Name Control Status (high Control Status (low) | Volue | Bt7 RSVD_0 RSVD_0 | Bt6 RSVD_0 RSVD_0 | Bt5 RSVD_0 RSVD_1 |) | Bt4 RSVD_0 F RSVD_0 F | Bt3 SVD_0 SVD_0 | Bt RSVI DEEPS | 2 Bt1 D_0 RSVD_0 LEEP LD_TIMEOUT | Bit High Bit L Bito RSVD | ow RSVD | FE P | DISGTEST ET_ENABLE F_ENABLE DE RESET | |
| Bit Registers Name Control Status (high Control Status (low Safety Alert A | Velue | Bt7 RSVD_0 RSVD_0 SCD SCD | Bt6 RSVD_0 RSVD_0 OCD2 OCD2 | Bt5 RSVD_0 RSVD_0 OCD1 |) | Bt4 RSVD_0 F RSVD_0 F OCC F | Bt3 SVD_0 SVD_0 COV | Bt RSVI DEEPS CU | 2 Bt1 D_0 RSVD_0 LEEP LD_IMEOUT V RSVD_0 | BR High Bt L Bt0 RSVD, LD_0 RSVD, RSVD, | 0 RSVD | P FE | DSGTEST ET_ENABLE F_ENABLE PF_RESET | |
| Bit Registers Nome Control Status (high Control Status (ow Safety Alert A Safety Status A Safety Alert B | Volue | Bit7 RSVD_0 RSVD_0 SCD SCD OTE | Bt6 RSVD_0 RSVD_0 0 CD2 0 CD2 0 TINT | BIS RSVD_0 RSVD_0 OCD1 OCD1 OTD |) | Bt4 RSVD_0 F RSVD_0 F OCC OTC F | Bt3 SVD_0 SVD_0 COV COV COV | Bt RSVI DEEPS CU CU | 2 Bt1 0_0 RSVD_0 LEEP LD_TIMEOUT V RSVD_0 V RSVD_0 NT UTD | BR High BRL Bt0 RSVD LD_0 RSVD RSVD UTC | 0 RSVD | P P | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL | |
| Bit Registers Name Control Status (high Control Status (ow) Safety Alert A Safety Alert B Safety Alert B | Value | Bt7 RSVD_0 RSVD_0 SCD SCD OTF OTF | BH5 RSVD_0 RSVD_0 OCD2 OCD2 OCD2 OTNT OTNT | BIS RSVD_ OCD1 OCD1 OTD OTD |) | Bt4 RSVD_0 F OCC OCC OTC F OTC F | Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 | Bt RSVI DEEPS CU CU CU | 2 BH 5_0 RSVD_0 LEEP LD_TIMEOUT V RSVD_0 V RSVD_0 NT UTD | BR High BRL BHO RSVD LD_O RSVD RSVD UTC UTC | 0 | P P | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL CURITY_KEYS | |
| Bit Registers Name Control Status (high Control Status (ow) Safety Alert A Safety Alert B Safety Alert B Safety Alert B Safety Alert C | Volue | Bt7 RSVD_0 RSVD_0 SCD SCD OTF OTF OCD3 | Bt5 RSVD_0 0 0 0 <td>Bt5 RSVD_0 OCD1 OCD1 OTD OTD OCDL</td> <td>)</td> <td>B14 RSVD_0 F RSVD_0 F OCC OCC OTC F OTC F COVL</td> <td>Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 PTOS</td> <td>Bt RSVI DEEPS CU CU CU UTII RSVI</td> <td>2 BH 0.0 RSVD_0 LEEP LD_TMROUT V RSVD_0 V RSVD_0 NT UTD 0.0 RSVD_0</td> <td>BR High BILL BHO RSVD LD_O RSVD RSVD UTC UTC UTC</td> <td>0 RSVD</td> <td>P FE</td> <td>DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL CURITY_KEYS</td> <td></td> | Bt5 RSVD_0 OCD1 OCD1 OTD OTD OCDL |) | B14 RSVD_0 F RSVD_0 F OCC OCC OTC F OTC F COVL | Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 PTOS | Bt RSVI DEEPS CU CU CU UTII RSVI | 2 BH 0.0 RSVD_0 LEEP LD_TMROUT V RSVD_0 V RSVD_0 NT UTD 0.0 RSVD_0 | BR High BILL BHO RSVD LD_O RSVD RSVD UTC UTC UTC | 0 RSVD | P FE | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL CURITY_KEYS | |
| Bit Registers None Control Status (Nigh Control Status (Dow Safety Alert A Safety Status A Safety Status B Safety Status B Safety Alert C Safety Status C | Value | Bt7 RSVD_0 SCD SCD OTF OTF OCD3 OCD3 | Bi6 RSVD_0 RSVD_0 OCD2 OCD2 OTINT OTINT SCDL SCDL | BtS RSVD_I OCD1 OCD1 OTD OTD OTD OCDL |) | BH4 RSVD_0 F OCC 0 OTC F OTC F OTC F COVL F | Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 PTOS SVD_0 | Bt RSVI DEEPS CU CU CU UTII RSVI PT | 2 BH 0.0 RSVD 0 LEEP LD TIMEOUT V RSVD 0 V RSVD 0 VI RSVD 0 NT UTD 0.0 RSVD 0 0 HW0F | Bt High Bt L Btion LD_0 RSVD RSVD UTC UTC RSVD RSVD | 0 | FFE P P SEC Log Panel | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL CURITY_KEYS | Clear I |
| Bit Registers Name Control Status (High Control Status (High Control Status (Jow Safety Alert A Safety Alert A Safety Status B Safety Status C | Value | Bt7 RSVD_0 RSVD_0 SCD SCD OTF OTF OCD3 OCD3 OCD3 OCD3 | 86 RSVD_0 RSVD_0 0CD2 0CD2 0THNT 0THNT SCDL SCDL SCDT SCDT | BtS RSVD_1 OCD1 OCD1 OTD OTD OCDL OCDL RSVD_1 | | BH4 RSVD_0 F RSVD_0 F OCC 0 OCC 0 OTC F COVL F COVL F SOT 0 | Bt3 SVD_0 COV COV SVD_0 SVD_0 SVD_0 SVD_0 SVD_0 SVD_0 SOCD | Br RSVI DEEPS CU CU CU UTII RSVI PT SOO | 2 8H1 0.0 RSVD_0 LEEP LLD_TIMEOUT V RSVD_0 NF UTD 0.0 RSVD_9 0 HWDF cc SVU | BR High BLL Bto RSVD, LD_O RSVD, RSVD, UTC UTC RSVD, RSVD, SVV | 0 | FF P P SEC Log Panel | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL :URITY_KEYS | ClearL |
| Bit Registers Name Control Status (high Control Status (high Control Status A Sartety Status C Sartety Status C FF Alert A FF Status A | Value | Bt7 RSVD_C SCD SCD OTF OCD3 OCD3 OCD3 CUDEP CUDEP SCD4 | Bt6 RSVD_0 0 RSVD_0 0 CD2 0 CD2 0 CD2 0 TNIT 0 TNIT S CDL S CDL S CDL S CDF S OTF S OTF | BIS RSVD_I OCD1 OCD1 OTD OTD OCDL OCDL RSVD_I RSVD_I | | BH4 F PSXD_0 F OCC F OCC F OTC F COVL COVL COVL SOT SOT SOT | Bt3 SVD_0 COV COV SVD_0 SVD_0 SVD_0 PTOS SVD_0 SOCD SOCD | Bt RSVI DEEPS CU CU UTII UTII RSVI PT SOO SOO SOO 21) | 2 Bti 9.9 RSVD 0 LEEP LO,TMMEOUT V RSVD 0 W RSVD 0 HI UTD 9.0 RSVD 9 0.1 RSVD 9 0.1 RSVD 9 0.2 SVV 2. SVV | BRHigh BLL Bto RSVD, LD_O RSVD, RSVD, UTC UTC RSVD, RSVD, SUV SUV | 0 | FF P P SEC Log Panel Transaction | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS | ClearL |
| Bit Registers | Value | Bt7 RSVD_C RSVD_C SCD SCD OTF OCD3 OCD3 OCD3 CUDEP CUDEP SCDL SCDI | BHS P RSVD.9 P RSVD.9 OCD2 OCD2 OTINT OTINT SCOL SCOF SOFF SOFF PSVD.9 PSVD.9 | BIS RSVD_ OCD1 OCD1 OTD OTD OCDL OCDL RSVD_ RSVD_ RSVD_ RSVD_ | | BI4 RSVD_0 F RSVD_0 F OCC 0 OTC F OTC F COUL COUL COUL F SOT SOT VIMA VIMA | Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 SVD_0 SVD_0 SOCD SOCD SOCD JIMR | Bt RSVI DEEPS CU UTII UTIII RSVI PT SOO SOO 2LV | 2 8H 0.0 RSV0.0 VEPL L0.1MR60H V RSV0.0 HT UTD 0.0 RSV0.0 HT UTD 0.0 RSV0.0 CC SOV CC SOV A DFETE | BR High BR L BRO RSVD CD RSVD RSVD UTC UTC RSVD RSVD SUV SUV | 0 RSVD | FF P P SEC Log Panel Transaction Name | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS LOG Cmd Result | Clear Le Read A |
| Bit Registers None Control Status (Nigh Control Status (Nigh Control Status (Nigh Sarter) Alert A Sarter) Status A Sarter A Sarter A Sarter B Sarter B Sarter B Sarter B Sarter C C Control C | Value | BE7 RSVD_0 SCD OTF OTF OCD3 OCD3 OCD3 OCD3 CUDEP CUDEP SCDL SCDL RSVD_0 | B65 PISVD_0 PISVD_0 OCD2 OUD4 OTM1 OTM1 SCDL SCDL SOTF SOTF RSVD_0 HWMK | BIS RSVD_I OCD1 OCD1 OTD OTD OCDL OCDL RSVD_I RSVD_I RSVD_I RSVD_I VSSE | | BH PSVD_0 F OOC OOC OTC F OTC F COUL COUL COUL SOT SOT VMAA VMAA VMEA | Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 SVD_0 SOCD SOCD SOCD JIMR VIMR LFOF | Bit RSVI DEEPS CU CU UTII RSVI PT SOO SOO 21A 21A RSVI | 2 BH 1.4EP LD_TMRK00T V RSND_0 1.4EP LD_TMRK00T V RSND_0 1.4EV RSND | BR High BR L BRO RSVD LD_O RSVD RSVD UTC UTC RSVD SVV SVV SVV CFET CFET RSVD | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | FF | DSGTEST F_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS LURITY_KEYS Cmd Resub | Clear Le Read A |
| Bit Registers Nane Control Status (high Control Status (high Control Status (high Control Status (high Sately Alant A Sately Alant B Sately Alant B Sately Alant B Sately Alant B P P Alant A P P Status A P P Status A P P Status B P P Status B P P Status B P P Status C P P P Status C P P Stat | Value | Bt7 RSVD_0 SCD SCD OTF OCD3 OCD3 CUDEP CUDEP SCDL RSVD_0 CNDE | B65 FISVD_0 NSVD_0 OCD2 OTBH OTBH SCR | BtS RSVD_I RSVD_I OCD1 OCD1 OCDL OCDL OCDL RSVD_I RSVD_I RSVD_I RSVD_I VSSF |)))))) | BH RSVD_0 F OCC 0 OTC F OTC F COVL C COVL F SOT SOT VMAA VREF VREF | Bt3 SVD_0 SVD_0 COV SVD_0 SVD_0 PTOS SVD_0 SOCD SOCD SOCD SOCD SOCD JMAR LFOF FOF | Br RSVI DEEPS CU U U U U U U U U U U U U U U U U U U | 2 BH 0.0 FSN0.0 LEEP LD_INBCOUT V RSN0.0 V RSN0.0 VI UTD NT UTD 0.0 FSN0.0 0.0 FSN0.0 0.0 FSN0.0 0.0 FSN0.0 A DEFIT 0.0 FSN0.0 FSN0.0 PS | BR High BRL BROD RSVD RSVD UTC UTC RSVD RSVD RSVD SUV SUV SUV CFET CFET RSVD OTPI | 0 RSVD 0 0 0 0 0 0 0 0 F F 0 0 | FE P SEC Log Panel Transaction Name | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS Log Cmd Result | Clear Le |
| Bit Registers Name Control Status (high Control Status (high Control Status (high State) Status A State) Status A State) Status A State) Status A State) Status A State Status A State Status A State Status A State Status A PF Status A PF Status B PF Status B PF Status B PF Status B PF Status C PF Status C PF Status C PF Status C | Value | BK7 RSVD_C SCD OTF OTF OCD3 OCD3 CUDEP CUDEP SCDL SCDL SCDL RSVD_C CUDEP | B65 PISVD_0 PISVD_0 OCD2 OCD2 OTINT OTINT SCRL SCRL SOTF FISVD_0 HMMX HMMX HMMX HMMX | BtS RSVD_1 OCD1 OCD1 OTD OCDL OCDL RSVD_1 RSVD_1 RSVD_1 RSVD_1 VSSF VSSF RSVD_1 | | BH RSX0E.0 F OCC F OCC OC OTC F COUL COUL COUL SOT SOT VMAA VMAA VREF VREF VREF VREF RSVD.0 | Bt3 SVD_0 SVD_0 COV COV SVD_0 SVD_0 SVD_0 SOCD SOCD SOCD JIMR JIMR LFOF LFOF LFOF | Bit RSVI DEEPS CU UTII UTIII RSVI SOO 200 210 210 RSVI RSVI RSVI RSVI RSVI | 2 BH 0 PSN0_0 LEEP LD_MMEOUT V NOV_0 W NOV_0 W NOV_0 MT UTD MT UTD 0.0 FSN0_0 0.1 HMOF CC SOV CC SOV C0 RSN0_0 UFETF DFETF A DFETF 0.0 RSN0_0 BF3WE_0_0 BF3WE_0 | BR High BBL BRID RSVD RSVD RSVD RSVD UTC UTC RSVD SVV SVV SVV SVV SVV SVV SVV SVV SVV | 0 RSVD 0 0 0 0 0 0 0 0 F F 0 0 5 5 5 6 6 7 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 7 8 8 8 7 8 8 8 8 8 8 8 8 8 8 8 8 8 | FE | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL :URITY_KEYS nLog Cmd Result | Clear L Read A |
| Bit Register: Nane Control Status (High Control Status (High Control Status (High Control Status (High State), Alert A State), Alert A State), Alert A State), Alert A State), Alert A Fr Status A Fr Sta | Value | Bt7 RSVD_C SCD OTF OCD3 OCD3 CUDEP CUDEP SCDL SCDL RSVD_C RSVD_C RSVD_C | B65 FISVD_0 NSVD_0 OCD2 OCD2 OTM1 OTM1 OTM1 SOTE SOTE SOTE PISVD_0 HMMAX HMMAX FISVD_0 HMMAX FISVD_0 HMMAX FISVD_0 | 815 RSVD_ RSVD_ 0CD1 0CD1 0TD 0TD 0CDL 0CDL RSVD_ RSVD_ VSSF VSSF VSSF RSVD_ RSVD_ RSVD_ | | B14 RSVD_0 F OCC 0 OCC 0 OTC F OTC F OTC F COVL C SOT VMA VMA VMEF RSVD_0 F RSVD_0 F | B13 SVD_0 COV COV SVD_0 SVD_0 SVD_0 TOS SVD_0 SVD_0 SVD_0 SVD_0 SVD_0 SVD_0 SVD_0 | Bt RSM DEEPS CU CU UTIII PT SOO 200 210 210 210 210 210 210 210 210 210 | 2 BH 0.0 FSN0.0 LEEP LD_INECOU V RSN0.0 V RSN0.0 V RSN0.0 0.0 FSN0.0 0.0 FSN0.0 0.0 FSN0.0 A DEFIT 0.0 FSN0.0 FBN0.0 0.0 FSN0.0 | BEHON BIL BIO RSVD, RSVD, RSVD, UTC UTC UTC SUV SUV SUV CFET CFET RSVD, OTPT TOSIS | 0 RSVD 0 N 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | FE P P FI SEC Log Panel Tansaction Name | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS CURTY_KEYS | Clear L |
| Bit Registers Varie Control Status (trip) Control Status (trip) Stately Alort A Stately Alort A Stately Alort A Stately Alort A Stately Alort A Stately Alort A Stately Alort A P Status A | Value | BI7 RSV0_C SCD SCD OTF OCD3 CUDEP SCDL SCDL SCDL SCDL RSV0_C CMDF RSV0_C SLEEP SLEEP | B65 PISVD_0 PISVD_0 OCD2 OCD2 OTMT OTMT SCOL SCOL SCOL SCOL SCOL SCOL SOTF PISVD_0 HMMK HMMK PISVD_0 PISVD_0 PISVD_0 | BES RSVD_1 OCD1 OCD1 OCD1 OTD OTD OCD1 RSVD_1 RSVD_1 RSVD_2 RSVD_1 RSVD_3 VSSF VSSF RSVD_3 SD_CMM | | BH BSX0_0 F SX0_0 F OCC OC OCC COL OTC F COUL COL SOT SOT VMAA VMAA VMAA VREF VREF RSVD_0 F BSVD_0 F DF F | B13 SVD_0 SVD_0 COV COV SVD_0 | BH RSVI DEEPS CU CU UTIII RSVI SOO SOO SOO 21A RSVI RSVI RSVI RSVI RSVI RSVI | 2 BH 14EP ILD [MESOL 0 V ESOL 0 V ESOL 0 V ESOL 0 V TO VIT UTD VIT UTD VIT UTD 0.0 ESVL 0 0.0 ESVL 0 0. | BRHON BIL BIO RSVD, LD.0 RSVD, UTC UTC UTC UTC UTC UTC UTC UTC UTC UTC | 000 RSVD | FE | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS Log Cmd Result | Clear L |
| Bit Registers None Correl Status (right Correl Status (right) Correl Status (right) Co | Value | BK7 RSVD_C SCD SCD OTF OCD3 CUDEP CUDEP SCDL SCDL SCDL SCDL SCDL SCDL SCDL SCDL SCDL SCDL SCD CUDEP SCDL SCDL SCD SCD SCD SCD SCD SCD SCD SCD | B65 FISVD_9 PISVD_9 OCD2 OCD2 OTM1 OTM1 OTM1 SOTF SOTF PISVD_9 HMMEX PISVD_9 HMMEX PISVD_9 FISVD_9 FISVD_9 FISVD_9 FISVD_9 OTFW1 | 815 RSVD_0 RSVD_0 0CD1 0CD1 0TD 0CDL 0CDL 0CDL 0CDL 0CDL 0CDL 0CDL 0CDL 0CDL 0CDL 0CDL 0CD1 | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | BH RSVD_0 F OCC 0 OCC 0 OTC F OTC F COVL C COVL F SOT VMA VREF F RSVD_0 F BF VO | 813 SVD_0 COV COV COV SVD_0 SVD_0 PTOS SVD_0 SOCD SOCD SOCD JMAR LFOF LFOF LFOF SVD_0 SVD_0 SSD_0 SS SS POR SS SS | BH RSVI DEEPS CU UUUUUUU RSVI SOO SOO 2LL RSVI RSVI RSVI RSVI RSVI RSVI RSVI SLEEF | 2 BH 0.0 FSN0.0 LEEP LD_INBC/01 V RSN0.0 V RSN0.0 V RSN0.0 V RSN0.0 0.0 FSN0.0 0.0 FSN0.0 0.0 FSN0.0 A DFETF 0.0 FSN0.0 FF PRWF 0.0 FSN0.0 0.0 FSN0.0 FF SN0.0 0.0 FSN0.0 | BRHON BLD BBD RSVD RSVD RSVD RSVD RSVD SVD SVD SVD SVD SVD SVD SVD SVD SVD | ((() (| FFI | DSGTEST ET_ENABLE F_ENABLE PF_RESET * SEAL URITY_KEYS a Log Cmd Result | Clear L |

Figure 3-2. BQStudio Window without Device

Without a device, BQStudio operates with reduced functions. Tools can be browsed and data fields inspected, but data can not be entered.

On the left side of the window is the dashboard which shows the adapter, device and simple voltage and current displays. The dashboard also shows the communication protocol the EV2400 is using to interface to the device - this is set to I2C by default, but SPI and HDQ options are available as well which will be described in more detail with the device configuration. The dashboard updates periodically unless Auto Refresh is stopped by clicking on the banner. The right side of the window has the commands pane.

The center panel of the window initially shows the register tab. The register display shows device status registers and is read once when the device is detected. To update the register values select the *Refresh* button at the top of the Registers tab. To repeatedly read the registers select the *Scan* button. To repeatedly read and log the register values to a file select the *Start Log* button and follow the prompts to save a log file. When a log is running, select *Stop Log* to end the log and close the file. The *Parameter View* selection allows the choice of basic parameters which shows commonly used registers, or all parameters which shows more registers.

If a device is connected and powered after BQStudio is powered, dashboard may auto detect the device and update the device and register display. Figure 3-3 shows a register display with a connected device.



Battery Management Studio Software

| 🚳 Registers 🖛 D | ata Memory abc C | ommand Sequence 🛭 🥏 Cor | mmands [Calik | ration | 🕎 Watch 🜆 Data | Graph 🔤 Err | ors | | | | | | | | |
|------------------------------|------------------|---------------------------|----------------|--------|---------------------|-------------|--------|---------------------|------------|-------|-----------------------------|--------------|---------------------------------------|------------------|---------|
| DashBoard | ~ | 🔕 Registers 🐹 | | | | | | | | | | | | 🗳 Commands 🛛 | - |
| nto Refresh is ON - Click te | Turn OFF | Registers | | | | | | | | | P * S | | 9 2 | Commands | |
| id I2C Addr(Hex) 10 | Detect | | | | | | | | | | Funditieter flew | care cog 5 | an wencom | DEVICE NUMBER | |
| Studio Version: 1.3.101 | | Registers Basic Parameter | rs Displayed | | | | | | | | | | | EW VERSION | |
| 0 | | Nama | Vitikus | Linke | Nama | 100.00 | Linite | Mana | Make | Linto | hana | Makura | linke | | |
| | EV2400 | Cel 1 Votage | 3473 | mV | Cell 9 Voltage | 3502 | m\/ | DEETOEE Temperature | -273 | 2 °C | Cel Tesperature | 27.0 | 90 | V PW_DOILD | |
| | Version:0.32 | Cel 2 Votage | 3487 | mV | Cell 10 Votage | 3500 | mV | ALERT Temperature | -273 | 2 *C | FET Temperature | -273.2 | *0 | HW_VERSION | |
| | SPI Cfg | Cell 3 Voltage | 3482 | mV | Stack Voltage | 3483 | userV | TS1 Temperature | 27.0 | •c | CC3 Current | 0 | userA | 🐔 IROM SIG | |
| | | Cell 4 Votage | 3484 | m∀ | RACK Pin Votage | 82 | userV | TS2 Temperature | -273 | 2 °C | CC1 Current | .7 | userA | p mon_sto | |
| | | Cell 5 Votage | 3490 | mΥ | LD Pin Voltage | 76 | userV | TS3 Temperature | -273 | 2 °C | Accum Charge | 0 | user | 🤹 STATIC_CFG_SIG | |
| | | Cel 6 Votage | 3486 | mΥ | CC2 Current | -7 | userA | HDQ Temperature | -273 | 2 °C | Accum Time | 271 | s | A DROM SIG | |
| | I2C | Cell 7 Voltage | 3496 | m∀ | Int Temperature | 24.2 | *C | DCHG Temperature | -273 | 2 °C | Cell Balancing Active Cells | 0x0000 | - | prom_ad | |
| V | | Cell 8 Voltage | 3491 | m∨ | CFETOFF Temperature | -273.2 | •C | DDSG Temperature | -273 | 2 °C | Cell Balancing Present Time | 0 | 8 | EXIT_DEEPSLEEP | |
| <u>~</u> . | | | | | | | | | | | | | | DEEPSLEEP | |
| 200 | bq76942 | | | | | | | | | | | | | SHUTDOWN | |
| YP . | Addr: 0x10 | | | | | | | | | | | | | ✓ RESET | |
| M | 27.0 € | | | | | | | | | | | | | PDSGTEST | |
| | | | | | | | | | | | | | | FUSE_TOGGLE | |
| | | | | | | | | | | | | | | PCHGTEST | |
| 3483 userV | | | | | | | | | | | | | | CHGTEST | |
| | | Bit Registers | | | | | | | | | | Bit High Bit | Low RSVD | DSGTEST | |
| | | None | Value | B#7 | B#6 | BtS | | Bt4 | Bt3 | Ð | t2 Bt1 | Bit | ^ | FET_ENABLE | |
| | | Control Status (high) | 0x0000 | RSVD_0 |) RSVD_0 | RSVD_0 | | RSVD_0 | RSVD_0 | RSV | D_0 RSVD_0 | RSVD | _0 | PF_ENABLE | |
| | | Control Status (low) | | RSVD_0 | 0 RSVD_0 | RSVD_0 | | RSVD_0 | RSVD_0 | DEEP | SLEEP LD_TIMEOUT | LD_C | NN | PE PECET | |
| S -100 100 3 | | Safety Alert A | 0x00 | SCD | OCD2 | 0001 | | 0000 | cov | 0 | IV RSVD_0 | RSVD | _0 | * PF_RESET | |
| <u>-</u> -200 🔵 200 - | | Safety Status A | 0.00 | SCD | 0002 | 0004 | | 000 | COV | 0 | IV RSVD_0 | RSVD | 00 | 🛹 SEAL | |
| F 200 200 F | | Safety Alert B | 0:00 | OIF | OINI | 010 | | ore | RSVD_0 | 01 | | UIC | | | |
| -320 - 320 - | | Safety Status B | 0.00 | 000 | OIN | 010 | | 010 | KSVD_0 | 01 | | 010 | · · · · · · · · · · · · · · · · · · · | SECORITY_REA2 | |
| | | Safety Alert C | 0.00 | 0000 | SODE | 0000 | | COVE | PD/D 0 | 100 | 0 1000 | ROVD | 0 | | |
| -7 | | DE Alert A | 0:00 | CLIDER | SOTE | RSVD (| | SOT | SOCO | 50 | 00 SOV | SIA | | Log Panel | Clear L |
| -1 | | DE Status A | 0.00 | CUDEP | SOTE | RSVD_C | | 501 | 5000 | 50 | 00 SOV | 501 | _ | Transaction Log | |
| | | EPF Awt B | 0:00 | SCDL | RSVD 0 | RSVD_C | | VMA | VINR | 30 | A DEETE | CEET | ¥ | Name Cond Recut | Road A |
| | | PF Status B | 0:00 | SCPL | RSVD 0 | RSVD_C | | VMA | VINR | 2 | VI DEETE | CEET | F | reame und Kesult | nead A |
| | | EPF Alert C | 0.00 | RSVD | HANX | VSSE | | VREE | LEDE | RSV | D.0 RSVD.0 | RSVD | 0 | | |
| | | EPF Status C | 0:00 | CMDE | HAMX | VSSF | | VRFF | LECE | R | 4F DRMF | OTP | F | | |
| | | PE Alert D | 0:00 | RSVD 4 | 1 RSVD.0 | RSVD C | | RSVD 0 | RSVD 0 | PCU | D.0 RSVD.0 | TOS | F | | |
| | | PF Status D | 0:00 | BSVD (| BSVD.0 | RSVD 0 | | RSVD 0 | RSVD 0 | PS | D 0 RSVD 0 | TOS | F | | |
| | | Battery Status (high) | 0x818C | SLEEP | RSVD 0 | SD. CMP | | PF | SS | E | SE SECI | SEC | 0 | | |
| | | Battery Status (low) | | OTPH | OTEW | COM CH | к | WD | POR | SLEE | P EN PCHG MODE | CEGUP | DATE | | |
| | | Alarm Status (high) | 0x0000 | SSBC | SSA | PF | | MSK SFALERT M | SK PFALERT | NITS | TART INTCOMP | RSVD | 0 | | |
| | | C. State (right) | | | | | | | | | | | | | |

Figure 3-3. Register View with Device

The available tools for the device are shown at the top of the window and may be selected by clicking on the tool icon. Tools may also be selected from the "View" menu as shown in Figure 3-4. Opening a new tool may change the center tab of the window. These tools are described in following sections. Not all devices have all the tools described. Multiple tools can be active at one time, tools which use the center pane for display are shown as a tabs at the top of the center section. These tabs can be closed with the "X" as desired, but closing the tab may terminate the operation running in the tab.







3.5 Commands

The Commands tab is displayed on the right side of the BQStudio window. Buttons allow reading various information about the device and certain operations. Commands and returned data are shown in the Log Panel of the tab. The seal function is unusual in general evaluation and is not recommended during initial evaluation.

CAUTION

Sealing the device without remembering the key will reduce the function of the EVM.

3.6 Data Memory

The data memory tool is used to configure the device. The device has both volatile registers and One Time Programmable (OTP) memory. Most evaluation can be performed without writing OTP. Configuration files may be saved and loaded later to resume evaluation. At power up, the device is configured from the OTP. On a new EVM, the OTP is blank. Configuration can be entered in the volatile registers using the Data Memory tool. The Data Memory tool displays as a tab in the center pane of the BQStudio window. Figure 3-5 shows the initial data memory view with a device connected. Configuration settings are grouped into different functions accessed with buttons on the left side of the pane. The Calibration section is displayed on initial selection. Other functional sections can be displayed by clicking on the named button.

| 🖏 Registers 🗢 I | Data Memory 🖾 | | | - [|
|-----------------|-----------------------------------|---------------|------------------------------|-----------------------------|
| Data Memoi | У | Filter/Search | Program OTP Auto Export Expo | rt Import Write_All Read Al |
| Read/Write Data | Memory Contents | | | |
| Calibration | Name | | Value | Unit |
| Cambradierr | Configuration | | | |
| Settings | Power Config | | 0000 | hex |
| | REG12 Config | | 00 | hex |
| Protections | REG0 Config | | 00 | hex |
| | Temperature Enable | | 0002 | hex |
| | Temperature Mode | | 0000 | hex |
| | DA Configuration | | 01 | hex |
| | Vcell Mode | | 001f | hex |
| | CC3 Samples | | 80 | Num |
| | Protection | | | |
| | Enabled Protections A | | fc | hex |
| | Enabled Protections B | | 00 | hex |
| | Enabled Protections C | | 00 | hex |
| | CHG FET Protections A | | 98 | hex |
| | CHG FET Protections B | | d5 | hex |
| | CHG FET Protections C | | 12 | hex |
| | DSG FET Protections A | | e4 | hex |
| | DSG FET Protections B | | e6 | hex |
| | DSG FET Protections C | | 62 | hex |
| | Body Diode Threshold | | 50 | mA |
| | ⊿ Alert | | | |
| | Default Alert Mask | | 000d | hex |
| | Alert Mask A | | fc | hex |
| | Alert Mask B | | f7 | hex |
| | Alert Mask C | | 76 | hex |
| | ⊿ FET | | | |
| | FET Options | | 01 | hex |
| | Chg Pump Control | | 01 | hex |
| | | | | |

Figure 3-5. Data Memory View

3.6.1 Entering, Saving, and Loading Configuration

Most of the configuration of the BQ769x2 is accomplished through setting values in data memory. The data memory locations are accessed using the buttons in the Data Memory view. The *Parameter View* selection at the top of the pane allows the choice of basic parameters which shows commonly used parameters, or all parameters which shows more configuration parameters.Data values may be changed by selecting and entering a value. Parameter registers which are bit fields may be changed by selecting the bit in the pop up when the register or its value is selected. Data Memory must be written after bit changes, a button is provided under the bit

field. Figure 3-6 shows the bit field for the Enabled Protections A which is one of the most basic settings that must typically be changed with the EVM.

| Protection | | | | | | | | | |
|--------------------------------|-----------|-------|-------|-------|--|-------|-------|-------|-------|
| Protection Confi | iguration | | | | | | | | hex |
| Enabled Protect | tions A | | | | | | | | hex |
| Enak Enak | | | | | Enabled Protection | s A | | 1 | |
| СНО | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| CHG | MSB | SCD | OCD2 | OCD1 | 000 | COV | CUV | RSVD | RSVD |
| DSG | | | | | | | | | |
| DSG | | | | | Write to Data Memory | 1 | | | |
| DSG | Alons C | | | | | | | | HWA |

Figure 3-6. Data Memory Bit Field Change

Changes to configuration by memory changes take place immediately, however the FETs are enabled using the Enable_FETs command. Enabling a protection and enabling the protection action on a FET are not sufficient, the FETs must be enabled with the command.

Calibration data is also located in data memory. Calibration values may be loaded manually or calculated by a tool.

The *Export* tool in the Data Memory view allows saving the configuration data to a comma-separated-value file format which can be accessed by a spreadsheet program. Reading data before export with the *Read All* button will load the data from the part rather than values which may be only in the view. The *Import* tool allows loading such a saved file into the view so that it can be written to the device. The *Write All* tool writes all values in the view into registers in the device.

3.6.2 OTP Programming

CAUTION

OTP programming is a permanent change to the device. Be sure all configuration and calibration are set before programming settings into the device. Casual programming may leave the board inoperable. Writes to OTP are not incremental, all OTP is written at the same time.

Once the configuration and calibration has been determined and loaded in the registers, it may be programmed to the BQ76952 OTP memory using the *Program OTP* button at the top of the pane. Note that this is a permanent programming and is not reversible. There are 2 writes possible, if the device has been programmed once, a second memory is available. Additional memories are not available. OTP memory is programmed using the OTP memory view. Programming typically takes about 40 s. To program the OTP memory:

- 1. OTP write requires 12V at the board stack and room temperature. Calibrate the device if needed.
- 2. Be sure the desired settings are written to the data memory.
- 3. Select the Program OTP tool at the top of the Data Memory window. This opens a Program OTP pane.
- 4. Adjust the board voltage to 12.0 +/- 0.1 V for programming.
- 5. Select the Check OTP Programming Possible button. If not successful make the recommended adjustments if possible. If successful, the display is similar to Figure 3-7.
- 6. Select the Program Data Memory to OTP Memory button. If successful, the display is similar to the check.
- 7. Adjust the board voltage back to normal operating conditions, cycle power, and test as desired.



| S Program OTP 22 | - 0 |
|--|-----|
| Program Data Memory to OTP Memory | |
| Program Data Memory to One Time Programmable Memory in device. Programming OTP can not be reversed. C check OTP Programming Possible Device returned Success: OTP Check/Programming Successful II E Program Data Memory to OTP Memory Send reset after programming | |

Figure 3-7. Program OTP Pane with Success Display

3.7 Calibration

The calibration tool may not be available for all versions of devices. When the calibration tool is not available calibration of the device can be performed by entering values in the calibration section of the data memory.

The calibration writes to the volatile registers in the device which are available in the Data Memory view. When calibration values are complete they can be written to the OTP with other configuration settings. Calibration cannot be written to OTP separately from configuration settings.

The EVM and all new boards should be calibrated before operation. The calibration view is shown in Figure 3-8. Temperature is typically calibrated first. Board Offset should be calibrated with no current flow and should be calibrated before Current Gain. The EVM uses a $1-m\Omega$ sense resistor and calibration at low current will result in some granularity from the current resolution. This may result in an apparent error at higher currents. Calibration at higher currents will reduce this effect and should be done where it is important.

Voltages and temperatures may be calibrated individually or as a group. All values entered will be calibrated. If individual values are to be calibrated, leave all the other entries blank. As an example, measure the battery voltage, calculate the average cell value and enter the value in the box. Clicking the Calibrate Voltage button runs the calibration. Values left blank or entered as '0' are not calibrated. When successful, a green check appears next to the button as shown in Figure 3-9. If there is an error, a red X appears instead with a message as shown in Figure 3-10.

When calibrating the EVM voltage, remember the EVM uses 1% values for the cell simulator resistors. Measuring each cell voltage value is recommended rather than using a common value if individual cell voltage calibration is desired.

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| er units are not supported for calibration | on. Refer to the bq769xx User Guide for | more information. | | |
|---|--|--|--|-----------|
| oltage Calibration Enter actual voltage in millivolts betweer requiring voltage calibration. Items with | n anode and cathode for any cell nout data will be not be calibrated. | -Board Offset C Perform Board no current app | alibration Offset Calibration with lied. | I |
| Leave unused items empty. | | Calibrate Bo | ard Offset | |
| Click "Calibrate Voltage" button below to | perform voltage calibration | | | |
| or an items with valid voltages. | | -Current Gain C | alibration | |
| Cell Voltage 1 mV | Cell Voltage 2 mV | Applied Curren | t -2000 mA* | |
| Cell Voltage 3 mV | Cell Voltage 4 mV | Calibrate Cur | rent | |
| Cell Voltage 5 mV | Cell Voltage 6 mV | Temperature C | Calibration | |
| | | Sensor | Applied Temperature | Calibrate |
| Cell Voltage 7 mV | Cell Voltage 8 mV | Internal Sensor | 25.0 * | с |
| | | CFETOFF Pin | 25.0 * | с |
| Cell Voltage 9 mV | Cell Voltage 10 mV | DFETOFF Pin | 25.0 * | с 🗆 |
| Other Voltages | | ALERT Pin | 25.0 • | с |
| Stack Voltage 10mV* | Pack Voltage 10m/* | Sensor 1 | 25.0 * | с |
| | | Sensor 2 | 25.0 * | с |
| Load Detect Voltage 10m | V* | Sensor 3 | 25.0 | с |
| | | HDQ Pin | 25.0 * | с |
| Calibrate Vol | tage | DCHG Pin | 25.0 * | с 🗆 |
| | | DDSG Pin | 25.0 * | с |

Figure 3-8. Calibration View



| /oltage Calibration Enter actual voltage in mi requiring voltage calibrat Leave unused items empt | llivolts between tion. Items with ty. | anode and cathode for any cell out data will be not be calibrated. |
|--|---|---|
| of all items with valid volt | tages. | perform voltage cambration |
| Cell Voltage 1 3500 | mV | Cell Voltage 2 3500 mV |
| Cell Voltage 3 3500 | mV | Cell Voltage 4 3500 mV |
| Cell Voltage 5 3500 | mV | Cell Voltage 6 3500 mV |
| Cell Voltage 7 3500 | mV | Cell Voltage 8 3500 mV |
| Cell Voltage 9 3500 | mV | Cell Voltage 10 3500 m ³ |
| Other Voltages | | |
| Stack Voltage 3500 | 10mV* | Pack Voltage 3500 10m |
| Load Detect Voltage 350 |)0 10m\ | pt. |
| | Calibrate Volt | age |

Figure 3-9. Example Voltage Calibration Success

| Current Gain Calibration |
|--------------------------|
| Applied Current mA |
| Calibrate Current |

Figure 3-10. Example Current Calibration Failure

3.8 Command Sequences

Features are controlled by commands as described in the BQ769x2 data sheet. Data is available from registers, and the registers view shows data, but a user may want to send specific commands to the device. The Command sequences tool allows this operation and is shown in Figure 3-11. The *Device Send and Receive* section allows read or write to a single or consecutive locations. The *Command Sequence* section allows reads and writes to be intermixed in a sequence. Sequences may be stored to files or called from files. Files may be assigned to buttons in the *Command Sequence File Assignment Buttons* section. Results can be viewed in the *Transaction Log* and saved to a file if desired.



Battery Management Studio Software

| Registers 🗢 Data Me | emory 🔠 bq769x2 Comma | nd Sequence 🛛 | | | | • |
|--|--|--------------------|----------------|-----------|-----------------------|--|
| q769x2 Comma | and Sequence | | | | | |
| ommand Sequence | • | | | | | |
| Device Send and Recc P IZC A Start R Bytes b | alve rotocol in use 12C dddress (Hex) AA egister (Hex) 01 0 write (Hex) 00 | | | × w | ite Con Ass Cli | Imand Sequence File Assignment Buttons aga a sequence File Assignment Button is pressed. ck Run to send commands in dalog to device. Right click on any button to clear contents. Imaging Imaging |
| Command Sequence | Use controls on right to sav | re, edit, and run. | Clear | Save Load | Edit Run | Image: Source Processing Controls Image: Source Processing Controls Image: Clear Log Save Log |
| micscamp | Command | DOVICE Hadi | Rog Hour (noxy | congen | Cherrony | Data(not) |
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Figure 3-11. Command Sequence View



4 BQ76952 Circuit Module Use

The BQ76952 circuit module contains the BQ76952 IC and related circuitry to demonstrate the features of the IC. Surface mount FETs are provided for the high current path. A thermistor provides temperature sensing on the board. Other components provide support for the IC and connections to the board. Basic operation is described in the BQ76952 EVM Quick Start Guide section. For details of the circuit, refer to the BQ76952EVM Circuit Module Physical Construction section.

4.1 Cell Simulator

The EVM includes a resistive cell simulator made up of 200- Ω series resistors. The taps of the resistor network are connected to the cell inputs using shunts on the J14 and J23 headers. BAT- is always connected to the resistor divider network. Installing a shunt on the top cell location connects the top cell input to the resistor divider to provide simulated voltages for the other cell inputs. If the shunt is not installed on the top cell position of the header all lower inputs are pulled to VSS. Installing shunts for the lower cell positions will connect the input to the simulated voltage. There is no indication of the cell simulator connection, the user must be aware of the shunt installation.

4.2 Evaluating with Load Current

With the BQ769x2 configured and the FETs enabled discharge current can be demonstrated by attaching suitable resistors or a DC load at the PACK terminals as shown in Figure 4-1.



Figure 4-1. Evaluating with Load Current

4.3 Evaluating Charge and Discharge Currents

Bipolar power supplies will source or sink current to maintain the set voltage. When bipolar supplies are available, they may be used for both the battery and pack side of the board to allow charge and discharge currents without re-connecting the equipment. Be sure to set the supplies appropriately to prevent exceeding the ratings of the EVM.



Figure 4-2. Evaluating with Charge or Discharge Current

4.4 Evaluating with Simulated Current

The BQ76952 EVM Quick Start Guide describes connection for basic operation. Providing more than recognizable current in that configuration can require a power supply with a significant power rating. Applying a charge current can damage some power supplies. Figure 4-3 shows a method to force current through the control path without a high wattage power supply or special equipment. The *load* power supply should be set at a low voltage in a constant current mode. Polarity can be reversed on the *load* supply to simulate a charge current. The battery simulation supply must never be reversed.





Figure 4-3. Simulating Current Setup

4.5 Reducing the Cell Count

The BQ76952 must have the top and bottom cells used for proper operation. Cell count can be reduced by shorting the unused cell inputs from the next-to-top down. Cell count can be reduced for basic evaluation by shorting unused cells at the input terminal block. Follow the recommendations in the datasheet for which cells to short. This works for both operation with the cell simulator and cells, but can have some side effects in transient tests because it parallels the shorted resistors to the cell IC where the capacitor provides a signal path to the used input. See Figure 4-4 for an example of simple reduced cell configuration for 14 cells. For the best evaluation with reduced cells in a transient environment, short the VCx pins at the capacitor and remove the unused input resistor. When using the cell simulator, shorting the unused cell at the terminal block is still required to eliminate the simulated cell voltage. Shorting the cell inputs at the terminal block screw terminals is suggested since it should be apparent if the board is re-used for a different cell count. Table 4-1 shows configuration recommendations for reduced cell count.

| Table 4-1. Reddeling Gen Gount | | | | | | | | |
|---|----------------------------|--------------------------|---------------------------------|-------------------|--|--|--|--|
| Unused Cell (Numbered from Bottom Cell 1) | Short cell input terminals | Input resistor to remove | Replace capacitor with 0 ohm | IC inputs shorted | | | | |
| Cell 15 | CELL15 to CELL14 | R3 | C5 | VC15 to VC14 | | | | |
| Cell 14 | CELL14 to CELL13 | R4 | C6 | VC14 to VC13 | | | | |

Table 4-1. Reducing Cell Count





Figure 4-4. Example 14 Cell Simple Evaluation Configuration

When reducing the cell count with the top cell used, the resulting configuration of the BQ7718 secondary protector does not match its data sheet configuration. While the circuit will typically function on the EVM, when implementing a design the configuration of the data sheet is recommended.

4.6 Connecting Cells

The EVM is constructed with a single connection to the top and bottom of the cell stack. Cell voltage for these cells is sensed on the board.

While the EVM has a place to mount an activated fuse, the pattern is shorted to allow easy evaluation without the concern of activating the fuse. When connecting cells use a fuse in the current path and any other signal path appropriate for your application.

The cell simulator provides resistors between the cell inputs. When the cell simulator shunts are installed, these resistors will load the cells and divide the voltage to any unconnected inputs as cells are connected. If desired, the cell simulator shunts can be installed during cell connection and removed after cell connection. The shunts must be removed after connection of cells or the cells will be discharged by the constant drain of the cell simulator resistors.

BAT- is the reference voltage for the IC and should be connected first. After BAT- cells may be connected in any order. Cell connection from the bottom up minimizes the voltage step size applied to the board. Recommended connection sequence for the EVM when connecting cells is bottom up:

- 1. Connect BAT-
- 2. Connect cells bottom up; CELL1, CELL2, CELL3 ...
- 3. Be sure the cell simulator shunts are removed

Figure 4-5 shows an example connecting cells with an EVM configuration reduced to 15 cells.





Figure 4-5. Example Connection with 15 Cells

4.7 Connecting to a Host

After initial operation of the monitor with the BQStudio software, it may be desirable to operate the board connected to and controlled by a microcontroller board. J17 could be used to connect I2C signals to the microcontroller board with GND and REG1 for a power supply from J2. The user should note that the J2 GND is connected to the BQ76952 VSS and BAT- while the J17 reference is PACK-. With the connection shown in Figure 4-6 the MCU runs from the battery voltage inside the protection FETs. If the MCU board provides pull ups for the I2C lines, remove the PU shunts from J15 and J18. Alternately, the microcontroller board GND could be referenced to the PACK- at J17. In this case the REG1 power supply would be modulated by the battery current. Since the sense resistor is small, this is not normally a concern, but the user should be aware of the difference. Do not connect the same reference to both the J2 GND and the J17 PACK- since this will short the sense resistor through the external equipment and may lead to damage or unexpected results.

CAUTION

Do not connect the MCU board to both the J2 GND and J17 PACK- terminals, this will short the sense resistor and could result in damage to equipment or unexpected results.

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Figure 4-6. Host Connection Concept

4.8 Hardware Configuration

4.8.1 Configuration Jumpers

Certain features on the BQ76952EVM may be configured by jumpers or shunts on headers. See Section 5.4 for details of the header pins. Not all configurations are compatible with all register settings, the user should set pins appropriately for the register settings planned. For example pins must not be pulled above REG18 when used as thermistor inputs. Pull up to REG1 is not acceptable when registers configure a pin as a thermistor input.

CAUTION

Multi-function pins must be connected to compatible signal levels before programming registers to avoid device damage.

The cell simulator headers and I2C configuration are discussed with board connection diagrams.

J6 and J11 select the connection of the DFETOFF and CFETOFF pins. Pins may be pulled low or high to REG1.

J7 selects the connection of TS2. It may be taken to a terminal block for connection of an external wake or thermistor. It may also be pulled to VSS. The 10k R29 simulates a nominal temperature.

J20 and J21 select the connection of ALERT. It may be connected to the on-board interface for HDQ or pulled up to REG1.

4.8.2 Unused Components

The EVM contains a number of component patterns which may be useful for evaluation. Unpopulated headers at the MCU may provide future signal access. Parallel FET configuration is possible by changing the component population in the FET area. See the FET schematic in Figure 5-11.



4.9 Configuration Register Programming

Configuration register programming should be done once hardware configuration is set with jumpers. Configuration registers are set in the Data Memory screen and are different from the status registers displayed in the Registers screen. See the BQ76952 data sheet and supporting documentation for register information. When a configuration file is available it may be imported to set all operational selections at once. However, a configuration file loaded with Data Memory Import can load as little as 1 parameter, so the user should be familiar with the contents of imported files. With a new device or after loading a configuration file, individual register changes may be made. Configuration register programming will typically involve the following general principles selected in various register names:

- 1. Selection of the function for multi-function pins
- 2. Selection of the protection features to be enabled
- 3. Selection of the protection thresholds for the enabled features
- 4. Setting the FET control options
- 5. Exporting (saving) the configuration register file for future use

When no additional changes are anticipated to the configuration and extended validation is planned, the user may write the configuration to OTP. OTP is written using the "Program OTP" button on the Data memory window of BQStudio. Once programmed the device will load the register values from OTP after reset. Additional register changes may be made, but the user should realize the part features have been permanently changed. OTP settings may be incompatible with additional hardware configuration changes and could result in damage. The user should check settings or replace the IC or EVM as required.

CAUTION

Hardware changes after OTP programming may result in damage to the IC or board after reset if incompatible configuration is selected.

Changing the Communcation Mode

The BQ76952 device and EVM support SPI and HDQ protocols in addition to I2C. Changing the communication protocol can be done with the following steps.

- 1. Select the communication type on the Data Memory screen under Settings->Comm Type.
- If using SPI or HDQ, enable REG0 and REG1 (the MCU on the EVM is operating at 3.3V logic levels). In Data Memory set *REG0 Config* to 0x1 and set *REG1 Config* to 0xD (REG1 enabled at 3.3V).
- 3. If using SPI mode: In Data Memory configure *SPI Configuration* to 0x60. This sets the MISO output to the REG1 voltage level.
- 4. If using HDQ mode: In Data Memory configure HDQ Pin Config to desired settings. Setting this register to 0x28 configures the HDQ pin to drive to the REG1 voltage level when it is an output. (Similarly, HDQ can also be configured to use the Alert pin using the Alert Pin Config register.)
- 5. After communication settings are complete, click the **SWAP_COMM_MODE** command button in the Commands window. At this point BQStudio will lose communication with the device if the communication mode has changed.
- 6. Reconfigure the communication jumpers on the EVM (J7, J10, J12, J15, J17) based on the communication mode selected. By default, these jumpers are configured for I2C communication.
- 7. Restart BQStudio. BQStudio should now automatically detect the device and the updated communication protocol.



5 BQ76952EVM Circuit Module Physical Construction

This section contains the PCB layout, bill of materials, and schematic of the BQ76952EVM circuit module.

The BQ76952EVM consists of one circuit module assembly, BMS029.

5.1 Board Layout

The BQ76952EVM circuit module is a 4.0-inch × 5.0-inch 4-layer circuit card assembly. It is designed for easy assembly with cell connections on the left edge to a terminal block. Pack terminals are on the top edge using a terminal block. Wide trace areas are used reducing voltage drops on the high current paths. Optional connections for hardware feature pins are on a separate terminal block on the top edge of the board. An on-board interface adapter with USB connector is located in the right lower corner. Configuration headers are toward the right side of the board. Pushbutton switches for wake up and reset of the BQ76952 are located near the bottom edge of the board. The EVM layout and construction allows easy understanding of the connections and access to the test points for evaluation, but the connector area and programming features result in a large board.

The board layout includes spark gaps with the reference designator prefix "E". These spark gaps are fabricated with the board and no component is installed.

See additional information in the configuration and operation sections of this document. Figure 5-1 to Figure 5-8 show the board layout.



Figure 5-1. Top Silk Screen





Figure 5-2. Top Assembly





Figure 5-3. Top Layer





Figure 5-4. Layer 2





Figure 5-5. Layer 3





Figure 5-6. Bottom Layer





Figure 5-7. Bottom Silk Screen





Figure 5-8. Bottom Assembly

5.2 Bill of Materials

The bill of materials for the circuit module is shown in Table 5-1. Substitute parts may be used in the manufacturing of the assembly.

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|----------|---------|---|-------------------|---------------------|------------------|
| !PCB1 | 1 | | Printed Circuit Board | | BMS029 | Any |
| C1, C71 | 2 | 1uF | CAP, CERM, 1 uF, 100 V, +/- 10%, X7R, 1206 | 1206 | C3216X7R2A105K160AA | TDK |
| C2 | 1 | 100pF | CAP, CERM, 100 pF, 100 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603 | 603 | GCM1885C2A101JA16D | MuRata |
| C3 | 1 | 0.47uF | CAP, CERM, 0.47 uF, 25 V, +/- 10%, X7R, AEC- Q200 Grade 1, 0805 | 805 | GCM219R71E474KA55D | MuRata |
| C4, C5, C6, C7, C8, C9, C10, C11, C14, C16, C17, C18, C19, C21, C22, C23, C24 | 17 | 0.22uF | CAP, CERM, 0.22 uF, 50 V, +/- 10%, X7R, 0603 | 603 | C1608X7R1H224K080AB | TDK |
| C12, C15 | 2 | 1uF | CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0805 | 805 | EMK212B7105KG-T | Taiyo Yuden |
| C13 | 1 | 0.022uF | CAP, CERM, 0.022 uF, 16 V, +/- 10%, X7R, 0603 | 603 | C0603C223K4RACTU | Kemet |
| C20 | 1 | 0.01uF | CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603 | 603 | 8.85012E+11 | Wurth Elektronik |
| C25 | 1 | 2.2uF | CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0805 | 805 | EMK212B7225KG-T | Taiyo Yuden |
| C27 | 1 | 100pF | CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603 | 603 | C0603C101J5GACTU | Kemet |
| C28, C31, C32, C33, C35, C39, C40, C41, C43, C44, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57 | 22 | 0.1uF | CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603 | 603 | 8.85012E+11 | Wurth Elektronik |
| C37, C38, C42, C45 | 4 | 0.1uF | CAP, CERM, 0.1 uF, 100 V,+/- 10%, X7R, AEC- Q200 Grade 1, 0603 | 603 | GCJ188R72A104KA01D | MuRata |
| C58, C59, C60, C62, C65, C66, C68 | 7 | 0.1uF | CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402 | 402 | 8.85012E+11 | Wurth Elektronik |



| | | Table 5-1. BQ/ | 6952 Circuit Module Bill Of | Materials (continued |) | |
|---------------------------------|----------|----------------|--|---|-----------------|--------------------------------|
| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
| C61, C67, C69 | 3 | 0.47uF | CAP, CERM, 0.47 uF, 6.3 V, +/- 10%, X5R, 0402 | 402 | 04026D474KAT2A | AVX |
| C63, C64 | 2 | 10uF | CAP, CERM, 10 µF, 16 V,+/- 10%, X5R, 0805 | 805 | CL21A106KOQNNNG | Samsung Electro- Mechanics |
| C70 | 1 | 2200pF | CAP, CERM, 2200 pF, 10 V, +/- 10%, X7R, 0402 | 402 | 8.85012E+11 | Wurth Elektronik |
| D1, D2, D9 | 3 | 100V | Diode, Schottky, 100 V, 0.15 A, SOD-123 | SOD-123 | BAT46W-7-F | Diodes Inc. |
| D3 | 1 | Red | LED, Red, SMD | LED_0603 | 150060RS75000 | Wurth Elektronik |
| D4, D5, D6 | 3 | 16V | Diode, Zener, 16 V, 500 mW, SOD-123 | SOD-123 | MMSZ5246B-7-F | Diodes Inc. |
| D7 | 1 | 100V | Diode, Ultrafast, 100 V, 0.15 A, SOD-123 | SOD-123 | 1N4148W-7-F | Diodes Inc. |
| D8 | 1 | 10V | Diode, Zener, 10 V, 500 mW, SOD-123 | SOD-123 | MMSZ4697T1G | ON Semiconductor |
| D13 | 1 | 40V | Diode, Schottky, 40 V, 0.2 A, SOT-323 | SOT-323 | BAS40W-7-F | Diodes Inc. |
| D14, D15, D16 | 3 | Green | LED, Green, SMD | LED_0603 | 150060VS75000 | Wurth Elektronik |
| H1, H2, H3, H4 | 4 | | Bumpon, Hemisphere, 0.44 X 0.20, Clear | Transparent Bumpon | SJ-5303 (CLEAR) | 3М |
| J1, J4 | 2 | | TERM BLOCK 3.5MM VERT 6POS PCB | HDR6 | OSTTE060161 | On Shore Technology |
| J2, J22 | 2 | | Header, 2.54mm, 5x1, Tin, TH | Header, 2.54mm, 5x1, TH | PEC05SAAN | Sullins Connector Solutions |
| J3 | 1 | | TERM BLOCK 3.5MM VERT 5POS PCB | HDR5 | OSTTE050161 | On Shore Technology |
| J5 | 1 | | Header, 100mil, 6x1, Tin, TH | TH, 6-Leads, Body 608x100mil, Pitch 100mil | PEC06SAAN | Sullins Connector Solutions |
| J6, J7, J11, J13, J16, J19 | 6 | | Header, 2.54mm, 3x1, Gold, SMT | Header, 2.54mm, 3x1, SMT | 87898-0304 | Molex |
| 19 | 1 | | TERM BLOCK 3.5MM VERT 4POS PCB | HDR4 | OSTTE040161 | On Shore Technology |
| J10, J12, J15, J18, J20, J21 | 6 | | Header, 100mil, 2x1, Tin, TH | Header, 2 PIN, 100mil, Tin | PEC02SAAN | Sullins Connector Solutions |
| J14 | 1 | | Header, 100mil, 6x2, Tin, TH | Header, 6x2, 100mil, Tin | PEC06DAAN | Sullins Connector Solutions |
| J17 | 1 | | Header (friction lock), 100mil, 4x1, R/A, TH | 4x1 R/A Header | 22/05/3041 | Molex |

Table 5-1. BQ76952 Circuit Module Bill of Materials (continued)



|--|

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---|----------|-------|---|--------------------------------------|-------------------|--------------------------------|
| J23 | 1 | | Header, 2.54mm, 10x2, Tin, TH | Header, 10x2, 2.54mm, TH | PEC10DAAN | Sullins Connector Solutions |
| J26 | 1 | | Receptacle, Micro-USB Type B, 0.65 mm, 5x1, R/A, Bottom Mount SMT | Receptacle, 0.65mm, 5x1, R/A, SMT | 47346-1001 | Molex |
| J27 | 1 | | Header, 2.54 mm, 2x1, Gold, TH | Header, 2.54mm, 2x1, TH | 61300211121 | Wurth Elektronik |
| J29 | 1 | | Header, 2.54mm, 4x1, Tin, TH | Header, 2.54mm, 4x1, TH | 22284043 | Molex |
| Q1 | 1 | 150 V | Transistor, NPN, 150 V, 1 A, AEC-Q101, SOT-89 | SOT-89 | FCX495TA | Diodes Inc. |
| Q4, Q11, Q13 | 3 | 150 V | Transistor, PNP, 150 V, 0.5 A, SOT-23 | SOT-23 | MMBT5401LT1G | ON Semiconductor |
| Q5, Q6 | 2 | -150V | MOSFET, P-CH, -150 V, -0.53 A, SOT-23 | SOT-23 | SI2325DS-T1-E3 | Vishay-Siliconix |
| Q8, Q9 | 2 | 150V | MOSFET, N-CH, 150 V, 56 A, PG-TDSON-8 | PG-TDSON-8 | BSC160N15NS5ATMA1 | Infineon Technologies |
| Q10 | 1 | 60V | MOSFET, N-CH, 60 V, 0.31 A, SOT-323 | SOT-323 | 2N7002KW | Fairchild Semiconductor |
| Q12 | 1 | 150V | MOSFET, N-CH, 150 V, 3 A, PowerPAK SO-8 | PowerPAK SO-8 | SI7898DP-E3 | Vishay-Siliconix |
| R1, R27, R28, R31, R41, R67, R81 | 7 | 100 | RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW0603100RJNEA | Vishay-Dale |
| R2, R3, R4, R7, R8, R11, R12, R13, R14, R16, R17, R18, R19, R21, R22, R23, R24 | 17 | 20 | RES, 20.0, 1%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | CRCW120620R0FKEA | Vishay-Dale |
| R5, R9 | 2 | 220 | RES, 220, 5%, 1 W, AEC- Q200 Grade 0, 2512 | 2512 | CRCW2512220RJNEG | Vishay-Dale |
| R20, R25, R29, R57, R89, R92, R94, R97, R99, R109, R110, R111 | 12 | 10k | RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060310K0JNEA | Vishay-Dale |
| R26, R91 | 2 | 100k | RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW0603100KJNEA | Vishay-Dale |
| R30 | 1 | 0.001 | RES, 0.001, 1%, 1 W, 1210 | 1210 | PMR25HZPFV1L00 | Rohm |



| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer | |
|--|----------|--------|---|-------------------|------------------|--------------|--|
| R32, R34, R36, R37, R47, R49, R53, R54, R69, R72, R75, R78, R83, R84, R85, R86 | 16 | 1.0k | RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW06031K00JNEA | Vishay-Dale | |
| R38, R58, R66, R79 | 4 | 20k | RES, 20 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060320K0JNEA | Vishay-Dale | |
| R39, R40 | 2 | 4.7k | RES, 4.7 k, 5%, 1 W, AEC-Q200 Grade 0, 2512 | 2512 | CRCW25124K70JNEG | Vishay-Dale | |
| R42, R43, R50, R51, R52 | 5 | 10Meg | RES, 10 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060310M0JNEA | Vishay-Dale | |
| R44 | 1 | 95.3k | RES, 95.3 k, 1%, 0.1 W, 0603 | 603 | RC0603FR-0795K3L | Yageo | |
| R45, R48 | 2 | 7.5k | RES, 7.5 k, 5%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | CRCW12067K50JNEA | Vishay-Dale | |
| R56, R112, R113 | 3 | 0 | RES, 0, 5%, 0.1 W, AEC- Q200 Grade 0, 0603 | 603 | CRCW06030000Z0EA | Vishay-Dale | |
| R59, R61, R62, R63, R82 | 5 | 5.1k | RES, 5.1 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW06035K10JNEA | Vishay-Dale | |
| R60 | 1 | 62k | RES, 62 k, 5%, 0.1 W, 0603 | 603 | RC0603JR-0762KL | Yageo | |
| R64, R68, R73, R74, R76, R77 | 6 | 5.1k | RES, 5.1 k, 5%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | CRCW12065K10JNEA | Vishay-Dale | |
| R65 | 1 | 7.5k | RES, 7.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW06037K50JNEA | Vishay-Dale | |
| R80 | 1 | 27k | RES, 27 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060327K0JNEA | Vishay-Dale | |
| R87, R88, R90, R93, R95, R96, R98, R100, R101, R102, R103, R104, R105, R106, R107, R108 | 16 | 200 | RES, 200, 1%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | CRCW1206200RFKEA | Vishay-Dale | |
| R114, R115 | 2 | 33 | RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW040233R0JNED | Vishay-Dale | |
| R116 | 1 | 2.0k | RES, 2.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04022K00JNED | Vishay-Dale | |
| R117, R123 | 2 | 10k | RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW040210K0JNED | Vishay-Dale | |
| R118, R119 | 2 | 1.0Meg | RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 402 | CRCW04021M00JNED | Vishay-Dale | |

Table 5-1. BQ76952 Circuit Module Bill of Materials (continued)



| | | Table 5-1. BQ | 6952 CIrcuit Module Bill of | Materials (continued | ı) | |
|---|----------|---------------|--|-------------------------|----------------------|---------------------|
| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
| R120, R121, R122 | 3 | 330 | RES, 330, 1%, 0.1 W, AEC-Q200 Grade 0, 0402 | 402 | ERJ-2RKF3300X | Panasonic |
| RT1, RT2 | 2 | 10k | Thermistor NTC, 10.0k ohm, 1%, Disc, 5x8.4 mm | Disc, 5x8.4 mm | 103AT-2 | SEMITEC Corporation |
| S1, S2 | 2 | | Switch, Tactile, SPST-NO, SMT | Switch, 6.2X5X6.2 mm | KST221JLFS | C&K Components |
| S3 | 1 | | Switch, SPST-NO, Off- Mom, 0.05A, 12VDC, SMD | 3.9x2.9mm | PTS820 J20M SMTR LFS | C&K Components |
| SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20, SH-J21 | 21 | 1x2 | Shunt, 100mil, Gold plated, Black | Shunt | SNT-100-BK-G | Samtec |
| TP14, TP15, TP16, TP17 | 4 | | Test Point, Compact, Black, TH | Black Compact Testpoint | 5006 | Keystone |
| U1 | 1 | | Multicell Battery Monitor and Protection Family, PFB0048A (TQFP-48) | PFB0048A | bq76952PFBT | Texas Instruments |
| U2, U3, U4, U5 | 4 | | Family 2-5S Overvoltage Protector with Internal Delay Timer, DPJ0008A (WSON-8) | DPJ0008A | BQ771807DPJR | Texas Instruments |
| U6, U7, U8, U9 | 4 | | Single-Channel ESD in 0402 Package With 10pF Capacitance and 6V Breakdown, DPY0002A (X1SON-2) | DPY0002A | TPD1E10B06DPYR | Texas Instruments |
| U10 | 1 | | Dual-Bit Dual Supply Transceiver with Configurable Voltage Translation and 3-State Outputs, DCT0008A, LARGE T&R | DCT0008A | SN74LVC2T45DCTR | Texas Instruments |
| U11 | 1 | | 25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br) | PN0080A | MSP430F5529IPN | Texas Instruments |

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| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|---------------------------------------|----------|--------|--|------------------------------|--------------------|--------------------------------|
| U12, U13, U15, U16 | 4 | | Single-Channel ESD in 0402 Package With 10pF Capacitance and 6V Breakdown, DPY0002A (X1SON-2) | DPY0002A | TPD1E10B06DPYT | Texas Instruments |
| U14 | 1 | | Single Output LDO, 150 mA, Fixed 3.3 V Output, 2.7 to 10 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br) | DBV0005A | TPS76333DBVR | Texas Instruments |
| Y1 | 1 | | Resonator, 4 MHz, 39 pF, AEC-Q200 Grade 1, SMD | 4.5x1.2x2 mm | CSTCR4M00G55B-R0 | MuRata |
| C26 | 0 | 0.01uF | CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603 | 603 | 8.85012E+11 | Wurth Elektronik |
| C29, C30, C34, C36 | 0 | 0.1uF | CAP, CERM, 0.1 uF, 100 V,+/- 10%, X7R, AEC- Q200 Grade 1, 0603 | 603 | GCJ188R72A104KA01D | MuRata |
| D10, D11, D12 | 0 | 100V | Diode, Schottky, 100 V, 0.15 A, SOD-123 | SOD-123 | BAT46W-7-F | Diodes Inc. |
| F1 | 0 | | Fuse, 30 A, 62 VDC, SMD | 9.5x2x5mm | SFK-3030 | Dexerials Corporation |
| FID1, FID2, FID3, FID4, FID5, FID6 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A |
| J8 | 0 | | Terminal Block, 3.5mm Pitch, 2x1, TH | 7.0x8.2x6.5mm | ED555/2DS | On-Shore Technology |
| J24 | 0 | | Header, 2.54 mm, 7x1, Gold, TH | Header, 2.54 mm, 7x1, TH | PBC07SAAN | Sullins Connector Solutions |
| J25 | 0 | | Header, 2.54 mm, 11x1, Gold, TH | Header, 2.54 mm, 11x1, TH | PBC11SAAN | Sullins Connector Solutions |
| J28 | 0 | | Header, 2.54mm, 5x1, Tin, TH | Header, 2.54mm, 5x1, TH | PEC05SAAN | Sullins Connector Solutions |
| Q2 | 0 | -150V | MOSFET, P-CH, -150 V, -0.53 A, SOT-23 | SOT-23 | SI2325DS-T1-E3 | Vishay-Siliconix |
| Q3 | 0 | 150V | MOSFET, N-CH, 150 V, 13 A, PG-TSDSON-8 | PG-TSDSON-8 | BSZ900N15NS3 G | Infineon Technologies |
| Q7 | 0 | 150V | MOSFET, N-CH, 150 V, 56 A, PG-TDSON-8 | PG-TDSON-8 | BSC160N15NS5ATMA1 | Infineon Technologies |

Table 5-1. BQ76952 Circuit Module Bill of Materials (continued)



BQ76952EVM Circuit Module Physical Construction

| Designator | Quantity | Value | Description | Package Reference | Part Number | Manufacturer |
|------------|----------|-------|---|---------------------------------|------------------|-----------------|
| R6, R10 | 0 | 220 | RES, 220, 5%, 1 W, AEC- Q200 Grade 0, 2512 | 2512 | CRCW2512220RJNEG | Vishay-Dale |
| R15 | 0 | 0 | RES, 0, 5%, 0.1 W, AEC- Q200 Grade 0, 0603 | 603 | CRCW06030000Z0EA | Vishay-Dale |
| R33 | 0 | 4.7k | RES, 4.7 k, 5%, 1 W, AEC-Q200 Grade 0, 2512 | 2512 | CRCW25124K70JNEG | Vishay-Dale |
| R35 | 0 | 10Meg | RES, 10 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060310M0JNEA | Vishay-Dale |
| R46 | 0 | 0 | RES, 0, 5%, 2 W, 2512 WIDE | 2512 WIDE | RCL12250000Z0EG | Vishay Draloric |
| R55 | 0 | 51 | RES, 51, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | 603 | CRCW060351R0JNEA | Vishay-Dale |
| R70, R71 | 0 | 5.1k | RES, 5.1 k, 5%, 0.25 W, AEC-Q200 Grade 0, 1206 | 1206 | CRCW12065K10JNEA | Vishay-Dale |
| TP1 | 0 | | Test Point, Multipurpose, Red, TH | Red Multipurpose Testpoint | 5010 | Keystone |
| TP9 | 0 | | Test Point, Multipurpose, Black, TH | Black Multipurpose Testpoint | 5011 | Keystone |
| TP43, TP44 | 0 | Red | Test Point, Compact, Red, TH | Red Compact Testpoint | 5005 | Keystone |

Table 5-1. BQ76952 Circuit Module Bill of Materials (continued)



5.3 REACH Compliance

In compliance with the Article 33 provision of the EU REACH regulation we are notifying you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are:

| Component Manufacturer | Component part number | SVHC Substance | SVHC CAS (when available) | | | |
|------------------------|----------------------------|---|---------------------------|--|--|--|
| Murata | Resonator CSTCR4M00G55B-R0 | Lead Titanium Zirconium Oxide [(Pbx Tiy Zrz) 03] | 12626-81-2 | | | |

Table 5-2. REACH Components



5.4 Schematic

Figure 5-9 through Figure 5-12 illustrate the schematics.







Figure 5-9. Schematic Diagram Monitor



BQ76952EVM Circuit Module Physical Construction



Figure 5-10. Schematic Diagram Pin Configuration







Figure 5-11. Schematic Diagram FETs



BQ76952EVM Circuit Module Physical Construction

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Figure 5-12. Schematic Diagram Interface

C70 2200pl

GND



6 Related Documents from Texas Instruments

- Texas Instruments, BQ76952 3S-16S Battery Monitor and Protector data sheet
- Texas Instruments, BQ76952 Technical Reference Manual
- Texas Instruments, Easy Configuration of BQ76942, BQ76952 Battery Monitors
- Texas Instruments, BQ76942, BQ76952 Software Development Guide
- Texas Instruments, BQ7718 Overvoltage Protection for 2 to 5-Series Cell Li-Ion Batt w/ Int Delay Timer data sheet

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3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
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