# User's Guide TPS546D24A 2-Phase SWIFT<sup>™</sup> Step-Down Converter Evaluation Module User's Guide

# TEXAS INSTRUMENTS

#### ABSTRACT

The TPS546D24AEVM-2PH evaluation module (EVM) is a two-phase buck converter with two TPS546D24A devices. The TPS546D24A device is a stackable synchronous buck with PMBus interface that can operate from a nominal 2.95-V to 16-V supply. The device allows programming and monitoring via the interface.

Two TPS546D24A devices are configured as two-phase buck converter in factory default, output current is evenly distributed in the two devices; both the negative and positive output terminals are connected together.

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# **1** Description

The TPS546D24AEVM-2PH is a two-phase buck design using two stacked TPS546D24A devices. It designed for a nominal 12-V bus and to produce a regulated 0.8-V output at up to 80 A of load current. The TPS546D24AEVM-2PH is designed to demonstrate stacking operation of the TPS546D24A in a two-phase, low-output voltage application while providing a number of test points to evaluate the performance of the devices. The TPS546D24AEVM-2PH can be modified to single-phase buck converters by changing the components assembled. See Section 4.3 for more information on single-phase configuration.

# 1.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS546D24AEVM-2PH. Observe all safety precautions.

Warning	The TPS546D24AEVM-2PH circuit module may become hot during operation due to dissipation of heat. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.
Caution	Do not leave the EVM powered when unattended.

#### WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This may result in exposed voltages, hot surfaces, or sharp edges. Do not reach under the board during operation.

### CAUTION

The circuit module may be damaged by over temperature. To avoid damage, monitor the temperature during evaluation and provide cooling, as needed, for your system environment.

### CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, check your equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to your equipment.

### CAUTION

The communication interface is not isolated on the EVM. Be sure no ground potential exists between the computer and the EVM. Also be aware that the computer is referenced to the battery- potential of the EVM.

# 1.2 Typical Applications

The TPS546D24A device is designed for the following applications:

- High-density power solutions
- Wireless infrastructure
- Switcher
- Router network
- Server

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- Storage
- Smart power systems



# 1.3 Features

This EVM has the following features:

- Regulated 0.8-V output up to 80-A<sub>DC</sub> steady-state output current
- The output voltage is marginable and trimmable using the PMBus interface
  - Programmable UVLO, soft-start, and enable via the PMBus interface
  - Programmable overcurrent warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable overvoltage and undervoltage warning and fault limits and programmable response to faults via the PMBus interface
  - Programmable turn-on and turn-off delays
- Convenient test points for probing critical waveforms

# **2 Electrical Performance Specifications**

Table 2-1 lists the electrical performance specifications in room temperature (20 to  $25^{\circ}$ C). Characteristics are given for an input voltage of VIN = 12 V, unless otherwise specified.

Table 2-1	TPS546D24AE	VM-2PH Electrica	I Performance S	Specifications
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Parameter	Test Conditions	MIN	TYP	MAX	Unit
Input Characteristics					
Input voltage range, V <sub>IN</sub>		5	12	16	V
Full load input current	I <sub>OUT</sub> = 80 A		6.4		A
Full load input current	V <sub>IN</sub> = 5 V, I <sub>OUT</sub> = 80 A		15.6		A
No load input current	I <sub>OUT</sub> = 0 A, switching enabled		130		mA
Enable switching threshold	Set by default resistor divider, JP2_P1 and JP2_P2 pins 3 and 4 shorted		5.26		V
Disable switching threshold	Set by default resistor divider, JP2_P1 and JP2_P2 pins 3 and 4 shorted		4.75		V
Output Characteristics					
Output voltage, V <sub>OUT</sub>			0.8		V
Output load current, I <sub>OUT</sub>		0		80	A
	Line Regulation: V <sub>IN</sub> = 5 V to 16 V		0.1%		
	Load Regulation: I <sub>OUT</sub> = 0 A to 80 A		0.1%		
Output voltage ripple	I <sub>OUT</sub> = 80 A		5		mVpp
Output voltage undershoot	I <sub>OUT</sub> = 20-A to 60-A step at 1 A/μs		70		mV
Output voltage overshoot	I <sub>OUT</sub> = 60-A to 20-A step at 100 A/µs		70		mV
	Phase current limit setting of U1_P1 programmed by MSEL2		52		A
	Phase current limit setting of U1_P2 programmed by MSEL2		52		A
Systems Characteristics					
Switching frequency	Programmed by MSEL1		550		kHz
Full load efficiency, V <sub>OUT</sub> <sup>(1)</sup>	I <sub>OUT</sub> = 80 A		84.8%		
Operating case temperature	I <sub>OUT</sub> = 80 A, 10 minute soak		80		°C
Loop bandwidth	40.4		30.3		kHz
Phase margin	- I <sub>OUT</sub> = 40 A		93.5		٥
PMBus Interface and Pin-Strapping					
U1_P1 PMBus address	Programmed by NVM and ADRSEL		36		Decimal
U1_P1 Voltage reference	Default setting of VOUT_COMMAND programmed by VSEL		800		mV
U1_P1 Soft-start time (TON_RISE)	Default setting of TON_RISE programmed by MSEL2		3		ms

(1) The efficiency is measured using the test points listed in Table 6-2 to minimize the effect of DC drops caused by onboard copper traces.



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# **3 Schematic**

Figure 3-1 through Figure 3-3 illustrate the TPS546D24AEVM-2PH schematics.



Figure 3-1. TPS546D24AEVM-2PH Schematic Page 1





Figure 3-2. TPS546D24AEVM-2PH Schematic Page 2 (U1\_P1 Master)



Figure 3-3. TPS546D24AEVM-2PH Schematic Page 3 (U1\_P2 Slave)



# 4 Test Setup

# 4.1 Test and Configuration Software

To change any of the default configuration parameters on the EVM through PMBus, obtain the *TI Fusion Digital Power Designer* software.

# 4.1.1 Description

The *TI Fusion Digital Power Designer* is the graphical user interface (GUI) used to configure and monitor the Texas Instruments TPS546D24A power converter installed on this evaluation module. The application uses the PMBus protocol to communicate with the controller over serial bus by way of a TI USB adapter described in Section 4.2.6.

# 4.1.2 Features

Some of the tasks you can perform with the GUI include:

- Turn on or off the power supply output, either through the hardware control line or the PMBus operation command.
- Monitor real-time data. Items such as input voltage, output voltage, output current, die temperature, and warnings and faults that are continuously monitored and displayed by the GUI.
- Configure common operating characteristics such as V<sub>OUT</sub> trim and margin, UVLO, soft-start time, warning and fault thresholds, fault response, and On/Off modes.

# 4.2 Test Equipment

### 4.2.1 Voltage Source

The input voltage source  $V_{IN}$  should be a 0-V to 20-V variable DC source capable of supplying a minimum of 16 ADC to support 80-A load with 5-V input. Connect input VIN and GND to T1 and T2. If the output voltage of the EVM is increased, the power supply may need to be capable of supplying more current.

# 4.2.2 Multimeters

TI recommends using two separate multimeters: one meter to measure  $V_{IN}$  and the other to measure  $V_{OUT}$ .

# 4.2.3 Output Load:

A variable electronic load is recommended for the test setup. To test the full load current this EVM supports, the load should be capable of sinking at least 80 A.

# 4.2.4 Oscilloscope

When using an oscilloscope to measure the switching node voltage or voltage ripple, measure using a *Tip-and-Barrel* method as Figure 4-1 shows, or better.

# 4.2.5 Fan:

During prolonged operation at high loads, it may be necessary to provide forced air cooling with a small fan aimed at the EVM. Maintain the surface temperature of the devices on the EVM below their rated temperature.

### 4.2.6 USB-to-GPIO Interface Adapter:

A communications adapter is required between the EVM and the host computer. This EVM is designed to use TI's USB-to-GPIO Adapter. Purchase this adapter at http://www.ti.com/tool/usb-to-gpio.

# 4.2.7 Recommended Wire Gauge

- Input VIN and GND to T1 and T2 (GND) (12-V input) The recommended wire size is AWG #12, with the total length of wire less than 2 feet (1 foot input, 1 foot return).
- Output T3 and GND T5 (0.8-V output) The minimum recommended wire size is AWG #10, with the total length of wire less than 2 feet (1 foot output, 1 foot return). A thicker wire gauge may be required to minimize the voltage drop the wires.



### 4.3 Tip and Barrel Measurement

Figure 4-1 illustrates the tip and barrel measurement for switching node waveform on TP2\_P1 with TP4\_P1 or TP2\_P2 with TP4\_P2.



Figure 4-1. Tip and Barrel Measurement

#### 4.4 List of Test Points, Jumpers, and Connectors

Table 4-1 lists the test point functions.

#### Table 4-1. Test Point Functions

Test Point	Туре	Name	Description
TP1_P1	T-H Loop	PVIN_P1	PVIN pin voltage of U1_P1 device measurement point
TP1_P2	T-H Loop	PVIN_P2	PVIN pin voltage of U1_P2 device measurement point
TP2_P1	T-H Loop	SW_P1	Switching node of output rail phase 1 measurement point, reference to TP4_P1
TP2_P2	T-H Loop	SW_P2	Switching node of output rail phase 2 measurement point, reference to TP4_P2
TP3_P1	T-H Loop	GND_P1	GND pin voltage of U1_P1 device measurement point
TP3_P2	T-H Loop	GND_P2	GND pin voltage of U1_P2 device measurement point
TP4_P1	T-H Loop	GND_P1	GND reference for switch node measurement of U1_P1
TP4_P2	T-H Loop	GND_P2	GND reference for switch node measurement of U1_P2
TP5_P1	T-H Loop	PG_S_P1	PGOOD signal of phase 1
TP5_P2	T-H Loop	PG_S_P2	PGOOD signal of phase 2
TP6	T-H Loop	AUX_5V	External 5V measurement point for VDD5
TP7	T-H Loop	DATA	DATA signal on J2 header
TP8	T-H Loop	SMBALRT	SMBALERT signal on J2 header
TP9	T-H Loop	CNTL	CNTL signal on J2 header
TP10	T-H Loop	CLK	CLK signal on J2 header
TP11	T-H Loop	GND	GND reference
TP12	T-H Loop	PVIN	VIN+ measurement point
TP13	T-H Loop	VOUT_P1	U1_P1 output voltage measurement point for efficiency, reference to TP16
TP14	T-H Loop	Remote SNS+	OUTPUT remote sense + voltage point
TP15	T-H Loop	GND	VIN- measurement point
TP16	T-H Loop	GND_P1	U1_P1 output voltage referencing GND for efficiency measurement
TP17	T-H Loop	CH_A	OUTPUT for small signal loop gain measurements (B/A setup)
TP18	T-H Loop	CH_B	INPUT for small signal loop gain measurements (B/A setup)
TP19	T-H Loop	Ext_AVIN	AVIN measurement point
TP20	T-H Loop	GND	GND reference
TP21	T-H Loop	VSHARE	VSHARE measurement point. Sensitive signal.
TP22	T-H Loop	VOUT	VOUT + measurement point
TP23	T-H Loop	GND	GND reference
TP24	T-H Loop	GND	GND reference
TP25	T-H Loop	GND	VOUT - measurement point
TP26	T-H Loop	VOUT_P2	U1_P2 output voltage measurement point for efficiency, reference to TP30
TP27	T-H Loop	SYNC	Synchronization connection between U1_P1 and U1_P2. External SYNC input.

Test Point	Туре	Name	Description
TP28	T-H Loop	Remote SNS-	OUTPUT remote sense - voltage point
TP29	T-H Loop	BC_DAT	Data for back-channel communications between stacked devices
TP30	T-H Loop	GND_P2	U1_P2 output voltage referencing GND for efficiency measurement
TP31	T-H Loop	BC_CLK	Clock for back-channel communications between stacked devices
TP32	T-H Loop	GND	GND reference
TP33	T-H Loop	VOSNS_P2	VOSNS measurement point for U1_P2
TP34_P1, TP34_P2	T-H Loop	MSEL2_P1, MSEL2_P2	MSEL2 measurement point for U1_P1 and U1_P2
TP35_P1, TP35_P2	T-H Loop	VSEL_P1, VSEL_P2	VSEL measurement point for U1_P1 and U1_P2

#### Table 4-1. Test Point Functions (continued)

#### Table 4-2 lists the EVM jumpers.

Jumper	Туре	Name	Description
JP1_P1, JP1_P2	Header, 100 mil, 2 × 1	EXT_5.1V_P1, EXT_5.1V_P2	Short to connect VDD5 of U1_P1 or U1_P2 to the 5.1 V from U2
JP2_P1, JP2_P2	Header, 100 mil, 3 × 2	CNTL_SEL1, CNTL_SEL2	U1_P1 and U1_P2 EN/UVLO pin selections
JP3	Header, 100 mil, 2 × 1	EN to GND	Short to disable the auxiliary 5 V
JP4	Header, 100 mil, 2 × 1	AVIN-PVIN	Short to connect to connect AVIN input to PVIN
JP5	Header, 100 mil, 2 × 1	AVIN-LDO	Short to connect to connect AVIN input to U2 input
JP6	Header, 100 mil, 2 × 1	PMBus3.3V-AVIN	Short to connect USB-to-GPIO 3.3V to AVIN
JP7_P1, JP7_P2	Header, 100 mil, 3 × 1	AVIN-U1_P1, AVIN-U1_P2	U1_P1 and U1_P2 AVIN input source selections
JP8	Header, 100 mil, 2 × 1	Micro_USB-PVIN	Short to connect PVIN to Micro USB connector

#### Table 4-3 lists the options for the EN/UVLO pin selections on JP2\_P1 and JP2\_P2.

#### Table 4-3. JP2\_P1 and JP2\_P2 Selections

Shunt Position	Selection
pin 1 to 2 shorted	PMBus adaptor control signal
pin 3 to 4 shorted	Resistor divider to PVIN
pin 5 to 6 shorted	EN/UVLO short to ground

#### Table 4-4 lists the options for the EN/UVLO pin selections on JP2\_P1 and JP2\_P2.

#### Table 4-4. JP7\_P1 and JP7\_P2 Selections

Shunt Position	Selection
pin 1 to 2 shorted	AVIN pin connected to AVIN input through 10- $\Omega$ resistor. Use this selection when testing with a split rail input.
pin 2 to 3 shorted	AVIN pin connected to PVIN through 10-Ω resistor

#### Table 4-5 lists the EVM connector functions.

#### Table 4-5. Connector Functions

Connector	Туре	Name	Description
J1	Header, 100 mil, 6 × 2	N/A	Do not use
J2	Header, 100 mil, 5 × 2	PMBus connector	PMBus socket for TI FUSION adaptor
J3	Header, 100 mil, 6 × 2	N/A	Do not use
J4	Micro USB	Micro USB	Micro USB connector to power EVM from a 5 V USB source



		(continuou)	
Connector	Туре	Name	Description
T1	Terminal block, 2 × 1	PVIN	VIN+ connector
T2	Terminal block, 2 × 1	GND	VIN– connector
Т3	Terminal 90A Lug	VOUT	VOUT+ connector
T4	Terminal block, 2 × 1	Ext_AVIN	External AVIN connector
T5	Terminal 90A Lug	GND	VOUT– connector

# Table 4-5. Connector Functions (continued)



# 4.5 Evaluating Single Phase Operation

The default configuration of the EVM is for 2-phase operation. For a single-phase operation, modify the EVM as follows:

- 1. Short MSEL2 of U1\_P1 to GND to program single-phase operation by populating R18\_P1 with a 0-Ω resistor.
- If U1\_P2 is left populated, disconnect VSHARE of the slave device from the master by depopulating R15\_P1 (this is a 0-Ω resistor and can be used for MSEL2 pin of U1\_P1 in the previous step).
- 3. If U1\_P2 is left populated, disable U1\_P2 by moving the JP2\_P2 jumper to position 5-6 (GND).

#### Note

This will leave the AVIN (pin 26) of U1\_P2 powered, if no-load leakage current or light-light efficiency measurement is important, the U1\_P2 AVIN pin should also be disconnected from the input supply. Disconnect the slave U1\_P2 AVIN from  $V_{IN}$  by removing the jumper from JP7\_P2.

# 4.6 Evaluating Split Rail Input

The default configuration of the EVM is for single rail input. Split rail input enables operation with 3.3V PVIN. For split rail operation configure the jumpers on the EVM as follows:

- 1. Open JP4 to disconnect AVIN from PVIN.
- 2. Move the jumper JP7\_P1 and JP7\_P2 to position 1-2 to disconnect the AVIN pin from the PVIN pins.
- 3. Apply the AVIN input to T4. 4-V or greater AVIN is required to bring the VDD5 voltage high enough to enable conversion.
- 4. If operation with 3.3-V PVIN is needed and the CNTL Jumpers (JP2\_P1 and JP2\_P2) are in position 3-4, the resistor divider at the EN/UVLO will need to be changed. Alternately move the CNTL Jumpers to position 1-2 and use the control signal to enable conversion or use the ON\_OFF\_CONFIG and OPERATION commands to enable conversion.

# 4.7 Configuring EVM to Overdrive VDD5

The EVM has an external LDO (U2) that can be used to overdrive VDD5. The output of this LDO is set for 5.1 V by default. This LDO is useful to minimize the power dissipation in the TPS546D24A IC when using a single rail input. Overdriving VDD5 moves the loss from the internal LDO of the TPS546D24A to the external LDO (U2). To use this LDO, configure the jumpers on the EVM as follows:

- 1. Short JP4 and JP5 to connect the input of the LDO to the input supply.
- 2. Open JP3 to enable the LDO.
- 3. Short JP1\_P1 and JP1\_P2 to connect the LDO output to the VDD5 pin.
- 4. Ensure the VDD5 output of the TPS546D24A is set below the external LDO's output voltage.



# 5 EVM Configuration Using the Fusion GUI

The TPS546D24A IC leaves the factory pre-configured. The factory default settings for the parameters can be found in the datasheet. If configuring the EVM to settings other than the factory defaults, use the software described in Section 4.1. It is necessary to have the input voltage applied to the EVM prior to launching the software so that the TPS546D24A may respond to the GUI and the GUI can recognize the device. The default configuration for the EVM to stop converting is set by the EN/UVLO resistor divider to a nominal input voltage of 4.75 V; therefore if it is necessary to avoid any converter activity during configuration, an input voltage less than 4.75 V should be applied. TI recommends an input voltage of 3.3 V.

### **5.1 Configuration Procedure**

- 1. Adjust the input supply to provide 3.3 VDC, current limited to 1 A.
- 2. Apply the input voltage to the EVM. See Section 4.2 for connections and test setup.
- 3. Launch the Fusion GUI software. See the screen shots in Section 10 for more information.
- 4. Configure the EVM operating parameters as desired.

By default the pinstrap resistors configure U1\_P1 as the loop master and U1\_P2 as the loop slave.



# **6 Test Procedure**

# 6.1 Line and Load Regulation and Efficiency Measurement Procedure

- 1. Set up the EVM as Section 4.2 and Section 6.2 describe.
- 2. Set the electronic load to draw 0  $A_{DC}$ .
- 3. Increase  $V_{IN}$  from 0 V to 12 V using voltage meter to measure input voltage.
- 4. Use the other voltage meter to measure output voltage  $V_{\mbox{OUT}}.$
- 5. Vary the load from 0 to 80 A<sub>DC</sub>. V<sub>OUT</sub> should remain in regulation as defined in Table 2-1.
- 6. Vary  $V_{IN}$  from 5 V to 16 V.  $V_{OUT}$  should remain in regulation as defined in Table 2-1.
- 7. Decrease the load to 0 A.
- 8. Decrease  $V_{\text{IN}}$  to 0 V.



### 6.2 Efficiency Measurement Test Points

To evaluate the efficiency of the power train (device and inductor), it is important to measure the voltages at the correct location. This is necessary because otherwise the measurements will include losses that are not related to the power train itself. Losses incurred by the voltage drop in the copper traces and in the input and output connectors are not related to the efficiency of the power train, which should not be included in efficiency measurements.

Input current can be measured at any point in the input wires, and output current can be measured anywhere in the output wires of the output being measured.

Table 6-1 shows the measurement points for input voltage and output voltage. VIN and VOUT are measured to calculate the efficiency. Using these measurement points will result in efficiency measurements that excluded losses due to the wires and connectors.

Test Point	Node Name	Description	Comment		
TP12	PVIN	Input voltage measurement point for VIN+	The pair of test points are connected to the PVIN/PGND pins of U1_P1. The voltage drop		
TP15	PGND	Input voltage measurement point for VIN– (GND)	between input terminal to the device pins is included for efficiency measurement.		
TP22	VOUT	Output voltage measurement point for VOUT+	The pair of test points are connected near the output terminals. The voltage drop from the		
TP25	GND	Output voltage measurement point for VOUT– (GND)	output point of the inductor to the output terminals is included for efficiency measurement		

#### Table 6-1. Test Points for Efficiency Measurements

For more accurate efficiency measurements of the power train, the voltage drop between the power train and the terminals should also be removed from the measurement. Using the test points in Table 6-2 will reduce these losses. To average the voltages at each test point so that only one meter is needed for PVIN and VOUT, add some resistance between the each test point and the meter. For the measurements taken in this user's guide, a 1.5-k $\Omega$  resistor was added in series with each test point. Using these test points reduced the measured power loss at 80 A load by approximately 0.5 W. This power is lost in the copper traces of the PCB.

Test Point	Node Name	Description	Comment
TP1_P1	PVIN_P1	Input voltage measurement point for VIN+	This pair of test points are connected to DVIN and DCND poor the pine of U1, D1
TP4_P1	GND_P1	Input voltage measurement point for VIN– (PGND)	
TP1_P2	PVIN_P2	Input voltage measurement point for VIN+	This pair of test points are connected to PVIN and PCND pear the pine of L11, P2
TP4_P2	GND_P2	Input voltage measurement point for VIN– (PGND)	
TP13	VOUT_P1	Output voltage measurement point for VOUT+	This pair of test points are connected to VOLIT and GND poor the output inductor for LL1_P1
TP16	GND_P1	Output voltage measurement point for VOUT– (GND)	
TP26	VOUT_P2	Output voltage measurement point for VOUT+	This pair of test points are connected to VOLIT and CND poor the output industor for LLL D2
TP30	GND_P2	Output voltage measurement point for VOUT– (GND)	

#### Table 6-2. Test Points for Better Efficiency Measurements



### 6.3 Control Loop Gain and Phase Measurement Procedure

The TPS546D24AEVM-2PH includes a 49.9- $\Omega$  series resistor in the feedback loop for V<sub>OUT</sub>. The resistor is accessible at the test points TP17 and TP18 for loop response analysis. These test points should be used during loop response measurements as the perturbation injecting points for the loop. See the description in Table 6-3.

#### Table 6-3. List of Test Points for Loop Response Measurements

Test Point	Node Name	Description	Comment
TP18	CH_B	Input to feedback divider of V <sub>OUT</sub>	The amplitude of the perturbation at this node should be limited to less than 30 mV
TP17	CH_A	Resulting output of V <sub>OUT</sub>	Bode can be measured by a network analyzer with a CH_B/CH_A configuration

Measure the loop response with the following procedure:

- 1. Set up the EVM as described in Section 4.2.
- 2. For V<sub>OUT</sub>, connect the isolation transformer of the network analyzer from TP18 to TP17.
- 3. Connect the input signal measurement probe to TP18. Connect the output signal measurement probe to TP17.
- 4. Connect the ground leads of both probe channels to TP20.
- 5. On the network analyzer, measure the Bode as TP18/TP17 (In/Out).



# 7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-4 present typical performance curves for the TPS546D24AEVM-2PH. The input voltage is 12 V and the oscilloscope measurements use 20 MHz bandwidth limiting unless otherwise noted.

### 7.1 Efficiency



### 7.2 Load and Line Regulation (Measured Between TP22 and TP25)





### 7.3 Transient Response

Figure 7-5 shows the transient response waveform with a 20 A to 60 A transient at 1 A/ $\mu$ s



Timescale = 100  $\mu$ s/div, CH4 = I<sub>OUT</sub> STEP at 10 A/div, CH3 = V<sub>OUT</sub> at 50 mV/division

Figure 7-5. Transient Response

# 7.4 Control Loop Bode Plot

Figure 7-6 is the control loop bode plot.



Figure 7-6. Bode Plot at 0.8-V Output at 12  $V_{\text{IN}},$  20-A Load



# 7.5 Output Ripple

Figure 7-7 and Figure 7-8 show the output ripple waveforms at 0-A and 80-A load.



Timescale = 1  $\mu$ s/div, CH1 = SW1 at 5 V/div, CH2 = SW2 at 5 V/div, CH3 = V<sub>OUT</sub> at 10 mV/div





Timescale = 1  $\mu$ s/div, CH1 = SW1 at 5 V/div, CH2 = SW2 at 5 V/div, CH3 = V<sub>OUT</sub> at 10 mV/div

#### Figure 7-8. Output Ripple With 80-A Load



# 7.6 Power MOSFET Drain-Source Voltage

Figure 7-9 and Figure 7-10 show the low-side and high-side MOSFET drain-source voltage (V<sub>DS</sub>) at 80-A load. The voltage is measured with 1-GHz bandwidth and at the solder mask openings near the U1\_P1 IC using a 1-GHz differential probe.



Timescale = 40 ns/div, CH1 = Low-side  $V_{DS}$  at 5 V/div

### Figure 7-9. Low-side MOSFET $V_{DS}$



Timescale = 40 ns/div, CH1 = High-side V<sub>DS</sub> at 5 V/div

# Figure 7-10. High-side MOSFET $V_{DS}$

# 7.7 Control On

Figure 7-11 and Figure 7-12 illustrate the start-up from control on waveforms at 0-A and 80-A output.





Timescale = 1 ms/div, CH3 = V<sub>OUT</sub> at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-11. Start-Up From Control, 0-A Load



Timescale = 1 ms/div, CH3 = V<sub>OUT</sub> at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

Figure 7-12. Start-Up From Control, 80-A CC Load



# 7.8 Control Off

Figure 7-13 and Figure 7-14 illustrate the control off waveforms at 0-A and 20-A outputs, respectively.



Timescale = 1 ms/div, CH3 = V<sub>OUT</sub> at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div



### Figure 7-13. Shutdown From Control, 0-A Load

Timescale = 1 ms/div, CH3 = V<sub>OUT</sub> at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

#### Figure 7-14. Shutdown From Control, 20-A CC Load



### 7.9 Control On With Pre-biased Output

Figure 7-15 illustrates the control on waveforms with a pre-biased output voltage.



Timescale = 1 ms/div, CH3 = V<sub>OUT</sub> at 500mV/div, CH4 = EN/UVLO at 2 V/div, CH5 = PGOOD at 5 V/div

#### Figure 7-15. Start-Up From Control With Pre-biased Output

### 7.10 Current Sharing Between Two Phases

Figure 7-16 illustrates the current sharing between two phases.



Timescale = 1 µs/div, CH1 = SW1 at 10 V/div, CH2 = SW2 at 10 V/div, CH3 = IL1 at 10 A/div, CH4 = IL2 at 10 A/div

#### Figure 7-16. Inductor Current and Switch Node Waveform, 40-A Load

# 7.11 Thermal Image

Figure 7-17 shows the TPS546D24AEVM-2PH thermal image.



V<sub>IN</sub> = 12 V, I<sub>OUT</sub> = 80 A





# 8 EVM Assembly Drawing and PCB Layout

Figure 8-1 through Figure 8-8 show the design of the TPS546D24AEVM-2PH printed circuit board.



Figure 8-3. TPS546D24AEVM-2PH Top Copper (Top Figure 8-4. TPS546D24AEVM-2PH Internal Layer 1 View)

(Top View)





Figure 8-5. TPS546D24AEVM-2PH Internal Layer 2 (Top View)



Figure 8-7. TPS546D24AEVM-2PH Internal Layer 4 (Top View)



Figure 8-6. TPS546D24AEVM-2PH Internal Layer 3 (Top View)



Figure 8-8. TPS546D24AEVM-2PH Internal Layer 5 (Top View)





Figure 8-9. TPS546D24AEVM-2PH Internal Layer 6 Figure 8-10. TPS546D24AEVM-2PH Internal Bottom (Top View)



Layer (Top View)

# 9 Bill of Materials

Table 9-1 lists the BOM for the TPS546D24AEVM-2PH.

#### Table 9-1. TPS546D24AEVM-2PH Bill of Materials

Designator <sup>(1)</sup>	Quantity	Value	Description	Package	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BSR104	Any
C1_P1, C1_P2, C11_P1, C11_P2	4	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C2_P1, C2_P2, C33, C34	4	100uF	CAP, AL, 100 uF, 35 V, +/- 20%, 0.15 ohm, SMD	SMT Radial G	EEE-FC1V101P	Panasonic
C3_P1, C3_P2, C4_P1, C4_P2, C5_P1, C5_P2, C6_P1, C6_P2	8	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X6S, 1210	1210	GRM32EC81E226KE15L	MuRata
C7_P1, C7_P2, C8_P1, C8_P2, C9_P1, C9_P2	6	6800pF	CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H682KA88D	MuRata
C12_P1, C12_P2	2	1000pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	0603	06031C102JAT2A	AVX
C13_P1, C13_P2, C20_P1, C20_P2	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C15_P1, C15_P2	2	4.7uF	CAP, CERM, 4.7 uF, 10 V, +/- 10%, X5R, 0603	0603	C0603C475K8PACTU	Kemet
C17_P1	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C19_P1, C19_P2	2	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C21_P1, C21_P2	2	33pF	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C330J5GACTU	Kemet
C22	1	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	C0805C105K5RACTU	Kemet
C23	1	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0805	0805	C2012X7R1A106M125AC	ТДК
C24	1	0.01uF	CAP, CERM, 0.01 µF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R72A103KA37J	MuRata
C25, C26, C31, C32, C35, C36, C37, C38, C41, C42, C43, C44, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C67, C68	26	47uF	CAP, CERM, 47 uF, 10 V, +/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
C47, C48, C63, C64	4	470uF	CAP, Tantalum Polymer, 470 uF, 6.3 V, +/- 20%, 0.01 ohm, 7343-40 SMD	7343-40	6TPF470MAH	Panasonic
D1, D2	2	30V	Diode, Schottky, 30 V, 2 A, AEC-Q101, SOD-123FL	SOD-123FL	MBR230LSFT1G	ON Semiconductor
D1_P1, D1_P2	2	45V	Diode, Schottky, 45 V, 0.75 A, SOD-523	SOD-523	BAS 52-02V H6327	Infineon Technologies
H1, H2	2		Machine Screw Pan Philips 10-32		PMSSS 102 0050 PH	B&F Fastener Supply
H3, H4, H5, H6	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
H7, H8	2		Machine Screw Nut, Hex, 3/8', Stn, Steel, 10-32		HNSS 102	B&F Fastener Supply
H9, H10	2		Washer, Split Lock, #10		1477	Keystone
J2	1		Header (shrouded), 100mil, 5x2, Gold, TH	5x2 Shrouded header	5103308-1	TE Connectivity
J4	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	MICRO USB CONN, R/A	1981568-1	TE Connectivity
JP1_P1, JP1_P2	2		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
JP2_P1, JP2_P2	2		Header, 100mil, 3x2, Gold, TH	Sullins 100mil, 2x3, 230 mil above insulator	PBC03DAAN	Sullins Connector Solutions
JP3, JP4, JP5	3		Header, 100mil, 2x1, Tin, TH	Header, 2x1, 100mil, TH	5-146278-2	TE Connectivity

Designator <sup>(1)</sup>	Quantity	Value	Description	Package	Part Number	Manufacturer
JP7_P1, JP7_P2	2		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
L1, L2	2	150nH	Inductor, Shielded, Ferrite, 150 nH, 55 A, 0.00015 ohm, SMD	SMD 13.46x8.0x12.95mm	SLC1480-151MLB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
LED1	1	Green	LED, Green, SMD	LED_0603	150060GS75000	Wurth Elektronik
R2_P1, R2_P2, R3_P1, R3_P2	4	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R4_P1, R4_P2, R15_P1, R15_P2, R16_P1, R16_P2, R17_P1, R17_P2, R18_P2, R22_P1, R22_P2, R23_P1, R23_P2, R25_P1, R25_P2, R27_P1, R27_P2, R32, R33	19	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R5_P1, R5_P2, R34, R35, R36, R38	6	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R6_P1, R6_P2	2	1.0	RES, 1.0, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW12061R00JNEA	Vishay-Dale
R8_P2, R26_P1, R26_P2	3	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R9_P1, R9_P2	2	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo
R14_P1, R14_P2	2	7.50k	RES, 7.50 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF7501V	Panasonic
R19_P1	1	14.7k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1472V	Panasonic
R21_P1	1	12.1k	RES, 12.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
R28	1	1.00k	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00FKEA	Vishay-Dale
R29	1	47.5k	RES, 47.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060347K5FKEA	Vishay-Dale
R30	1	15.0k	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060315K0FKEA	Vishay-Dale
R31	1	560k	RES, 560 k, 1%, 0.1 W, 0603	0603	RC0603FR-07560KL	Yageo
SH-JP1, SH-JP2, SH-JP3, SH-JP4, SH- JP5, SH-JP6	6	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
SMB1_P1, SMB1_P2, SMB2	3		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
T1, T2	2		Therminal Block, 5 mm, 2-pole, Tin, TH	TH, 2-Leads, Body 10x10mm, Pitch 5mm	282856-2	TE Connectivity
T3, T5	2		Terminal 90A Lug	CB70-14-CY	CB70-14-CY	Panduit
T4	1		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
TP1_P1, TP1_P2, TP6, TP12, TP13, TP19, TP22, TP26	8		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP2_P1, TP2_P2, TP5_P1, TP5_P2, TP7, TP8, TP9, TP10, TP14, TP17, TP18, TP21, TP27, TP28, TP29, TP31	16		Test Point, Multipurpose, White, TH	White Multipurpose Testpoint	5012	Keystone
TP3_P1, TP3_P2, TP4_P1, TP4_P2, TP11, TP15, TP16, TP20, TP23, TP24, TP25, TP30, TP32	13		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
U1_P1, U1_P2	2		2.95-16V 40A PMBUS Stackable Synchronous Buck Converter, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS546D24ARVFR	Texas Instruments
U2	1		800-mA Ultra-Low-Noise, High-PSRR LDO, DNT0012B (WSON-12)	DNT0012B	LP38798SD-ADJ/NOPB	Texas Instruments

#### Table 9-1. TPS546D24AEVM-2PH Bill of Materials (continued)



Table 9-1. TPS546D24AEVM-2PH Bill of Materials	(continued)
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Designator <sup>(1)</sup>	Quantity	Value	Description	Package	Part Number	Manufacturer
C10_P1, C10_P2, C14_P1, C14_P2	0	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C16_P1, C16_P2	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet
C17_P2	0	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C18_P1, C18_P2	0	2.2uF	CAP, CERM, 2.2 uF, 16 V, +/- 10%, X7R, 0603	0603	EMK107BB7225KA-T	Taiyo Yuden
C27, C28, C29, C30, C39, C40, C45, C46, C61, C62, C65, C66, C69, C70, C71, C72	0	47uF	CAP, CERM, 47 uF, 10 V, +/- 10%, X7R, 1210	1210	GRM32ER71A476KE15L	MuRata
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J1, J3	0		Receptacle, 2.54mm, 6x2, Gold, TH	Receptacle, 2.54mm, 6x2, TH	SSQ-106-03-G-D	Samtec
JP6, JP8	0		Header, 100mil, 2x1, Tin, TH	Header, 2x1, 100mil, TH	5-146278-2	TE Connectivity
R1_P1, R1_P2, R18_P1, R24_P1, R24_P2, R37, R39	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R8_P1	0	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R10_P1, R10_P2, R11_P1, R11_P2, R12_P1, R12_P2, R20_P1, R20_P2	0	10.5k	RES, 10.5 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K5FKEA	Vishay-Dale
R13_P1, R13_P2	0	53.6k	RES, 53.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060353K6FKEA	Vishay-Dale
R19_P2	0	14.7k	RES, 14.7 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF1472V	Panasonic
R21_P2	0	12.1k	RES, 12.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060312K1FKEA	Vishay-Dale
ТР33	0		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP34_P1, TP34_P2, TP35_P1, TP35_P2	0		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone

(1) Unless otherwise noted, all parts may be substituted with equivalents.



# 10 Using the Fusion GUI

# 10.1 Opening the Fusion GUI

The Fusion GUI should include *IC\_DEVICE\_ID* in the scanning mode to find TPS546D24A. The EVM needs power to be recognized by the Fusion GUI. See Section 5 for the recommended procedure.

TE	TEXAS INSTRUMENTS						
Fusion Di Version 7.1.2	gital P 28 [2019	0W91 9-12-06	Dəsig. I	nər			
No Devices Fo No compatible PMBus power is supplied to y	und! devices were /our device.	e found. Plea	se check tha	t the serial cable	end of your USB adapte	r is attached to your device and	
Scanning Mode:	DeviceI	DAndCode	AndICDe	viceID			
USB Adapter Firr	nware Versi	ion: 1.0.1	13				
Bus Speed:	Packet Er	rror Checki	ing:		ALERT Pullup:	2.2 kΩ 🗸	
🔾 100 kHz	💿 Enable	ed		<ul> <li>Serial</li> </ul>	CLOCK Pullup:	2.2 kΩ 🗸	
• 400 kHz	🔿 Disabl	led			DATA Pullup:	2.2 kΩ 🛛 🗸	
Signals SMBALERT#: Control Lines: (click to set)	ACK: High #1 High Low	#2 ○ High ● Low	Refrest #3 O High O Low	#4 O High O Low	₩5 ○ High ● Low	Refresh All	
G	nange Device	Scanning Op	tions	Retry	Offline Mode Exit P	rogram I2C GUI	

Figure 10-1. Select Device Scanning Mode



# **10.2 General Settings**

Figure 10-2 shows the General Settings that can be used to configure the following:

- · Vout settings, power good limits and margin voltages
- OC Fault, OC Warn and Fault response
- OT Fault, OT Warn (Die Temperature) and Fault response
- Vin on and off UVLO
- On/Off Config
- · Soft Start (Output rise time), other Turn On Timing and Turn Off Timing
- Switching frequency
- Compensation

After clicking *Write to Hardware* to make changes to one or more configurable parameters, the changes can be committed to nonvolatile memory by clicking *Store Config to NVM*. This action prompts a pop-up, and if confirmed, the changes are committed to nonvolatile memory to store all the modifications in non-volatile memory.

Both the loop master device and the loop slave device are tied to same bus interface. In a two-phase stacking system, the master device will receive and respond to all PMBus communication and slave devices do not need to be connected to the PMBus. If the master receives commands which require updates to the PMBus registers of the slave, the master will relay these commands to the slaves. All commands on this tab are for PHASE = 0xFF.

🖗 Configuration TP5546D24A @ PMBus Addr 36d (24h) / 12C Addr 72d (48h)							
File Device Tools	File Device Tools						
🖞 Write to Hardware 🛛 🗙 Discard Changes Store Config to NVM Restore NVM Config 💑 Error Chedking							
Configure	General Setting SMBALERT# Mask Device Info Phase Commands Pin Strapping All Co	nfig					
	Voltage Settings	Rail On/Off Settings					
	Vout Max: 1.500000 ↔ V	On/Off Config: 0x17 (CONTROL Pin Only)					
	Over Fault: 0.317404 V 14.0 V Response: Respo V	Turn On Delay: 0.0 🕁 ms					
	Over Warn: 0.870538 ♥ 9.0 ♥ %	Rise Time: 3.00 🕆 ms Fall Time: 0.50 🗘 ms					
	Margin High: 0.839394 🗸 V 5.1 🗸 %	Max Turn On: 00 ms					
	Vout: 0.798828 V Synchronize margins/limits/ PG to Vout	✓ No limit					
	Margin Low: 0.758263 🗢 V -5.1 🤤 %						
	Under Warn: 0.727058 🗢 V -9.0 👻 %	Turn On Fault Response: Respons					
	Under Fault: 0.678692 ☆ ∨ -15.0 ☆ % Response: Respo ∨	Vin On: 2.75 😴 V					
	Vout Min: 0.500000 🗸 V	Vin Off: 2.50 ⊕ ∨					
	Vout Scale Loop: 0.500 V						
	Vout Mode: Relative; 🗹						
	Vout Trim: 0.000000 👻 V						
	Lurrent & Temperature Settings	USER_DATA_01 (Compensation) USER_DATA_05 (Power Stage)					
	Iout Cal Offset: 0.0000 🗘 A	SEL_GMV 50 VDDS regulator volcage 4.7V V					
	Iout Cal Gain: 1.000 🗢	SEL_GMI 100 V µS					
	Iout OC Warn Limit: 80.0 🕁 A	SEL_RVV 40 V K2 550 V kHz					
	Iout OC Fault Limit: 104.0 🕁 A	SEL_CPV 18.75 V PF					
	Iout OC Fault Response: Response=	SEL_RVI 40 V KΩ					
	Temp Warn Limit: 125 🖉 °C	SEL_CPI 9.6 V PF					
	Temp Fault Limit: 150 🕁 °C						
	OT Fault Response: Response=	CZI 239.76					
		CZV 750 V					
- in Canfinner							
Connyure							
🤄 Monitor							
🤣 Status	PMBus Log	 					
Fusion Digital Power Designer v7	.1.28.Beta TPS546D24A @ PMBus Address 36d (24h) * Not Saved						

#### Figure 10-2. General Settings



Some commands require the

# 10.3 Changing ON\_OFF\_CONFIG

Changing the *On/Off Config* prompts a pop-up window with details of the options shown in Figure 10-3. This pop-up gives multiple options on what turns on and off power conversion. By default the TPS546D24A is configured to *CONTROL Pin Only*. This is the EN/UVLO pin.

🗋 Write to Hardware 🛛 🗡	Discard Changes Store Config to NVM Restore NVM Config									
Configure	General Setting SMBALERT# Mask    Device Info    Phase Commands    Pin Strapping    All Config									
	Voltage Settings	Rail On/Off Settings								
	Vout Max:         1.500000 ⊕ ∨           Over Fault:         0.917404 ⊕ ∨         14.8 ⊕ % Response:         Respon ∨	On/Off Config: 0x17 ☑ (CONTROL Pin Only) — Turn On Timing — On / Off Control — — — — — — — — — — — — — — — — — — —								
	Over Warn:       0.870588 2 V       9.0 2 3%         Margin High:       0.839334 2 V       5.1 2 %         Wout:       0.798828 2 V       5.1 2 %         Wout:       0.798828 2 V       5.1 2 %         Margin Low:       0.758285 2 V       -5.1 2 %         Under Warn:       0.727058 2 V       -9.0 2 %         Under Fault:       0.678832 2 V       -15.0 2 %         Vout Min:       0.50000 2 V         Vout Scale Loop:       0.500 V         Vout Mode:       Relative; V	Turn On Delay:       Always Converting       ns         Rise Time:       Unit powers up any time power is present, regardless of state of the CONTROL pin or OPENATION command.       ns         Max Turn On:       No lim       CONTROL Pin Only       ns         Turn On Fault Response:       Re       OPENATION command from serial bus. Power is converted when the CONTROL pin is active.         Vin On:       OPENATION Only       The device ignores the CONTROL pin. Power is converted when the only off portion of the OPENATION only         Vin Off:       OPENATION Command is on.       Both CONTROL Pin & OPENATION the OPENATION only         The device ignores the CONTROL pin. Power is converted when the only off the OPENATION only       The device ignores the CONTROL pin. Power is converted when the only off portion of the OPENATION only         Øbth CONTROL Pin & OPENATION the CONTROL Pin State active and the only off portion of the OPENATION command is on.       Both CONTROL Pin State active and the only off portion of the OPENATION command								
	Vout Trim: 0.00000 ⊕ ∨ Current & Temperature Settings Iout Cal Offset: 0.0000 ⊕ A	USER_DATA_01 (Compensation SEL_GMV 50 V So V Start the unit)								
	Iout Cal Gain:         1.000 ⊕           Iout OC Warn Limit:         80.0 ⊕           Iout OC Fault Limit:         104.0 ⊕           Iout OC Fault Response:         Response= (∨)           Temp Warn Limit:         125 ⊕         *c	SEL_GMI       100       Control Pin Turn Off Configuration         SEL_RWV       40       Soft Off         Use the turn off delay configured by       TOFF_DELAY and fall time configured by         TOFF_FALL       TOFF_FALL         SEL_CPI       9.6								
	Temp Fault Limit: 150 🗁 *C OT Fault Response: Response= 🗸	CZI_MULT     80        CZI     239.76        CZV     750								
Configure										

Figure 10-3. Configure – ON\_OFF\_CONFIG



### 10.4 Pop-up for Some Commands While Conversion is Enabled

Some commands will cause a pop-up like the one shown in Figure 10-4 when trying to change them while conversion is enabled. The settings in the GUI which will cause this pop-up include *FREQUENCY\_SWITCH*, *USER\_DATA\_01 (Compensation)*, *Vout Mode* and *Vout Scale Loop*. To change these settings to a new value, click on *Stop Power Conversion* then *Close and continue*. The GUI will automatically disable conversion, write the new value, and enable conversion again.

👆 Stop Power Conversi	ion on TP5546D24A @ PMBus Address 36d	_ 🗆 🔀				
One or more of the configuration changes you made requires that power conversion be stopped before writing a new value to the device. • FREQUENCY_SWITCH: modified value = 650 kHz [0x028A]; device value = 550 kHz [0x0226] @ Click on "Stop Power Conversion" if you would like GUI to stop power conversion on rails. @ Click on "Abort" will abort write operation. Power conversion will be restored its original state if changed. @ Click on "Close and continue" will close this window, and continue with write operation. Upon completion, power conversion will be restored to its original state if changed.						
Timestamp	Message					
Force ON_OFF_CONF	IG to use OPERATION command to turn rail(s) off Copy to Clipboard Stop Power Conversion Abort Close and	continue				

Figure 10-4. Pop-up When Trying to Change FREQUENCY\_SWITCH With Conversion Enabled



### 10.5 SMBALERT# Mask

The sources of SMBALERT which can be masked are found and configured on the SMBALERT # Mask tab (Figure 10-5).

🏘 Configuration TP55	546D24A @ PMBus Addr 36d (24h) / I2C Add	r 72d (48h)		_ 0 🛛				
File Device Tools								
Write to Hardware	Discard Changes Store Config to NVM Restore	NVM Config   💑 Error Checking						
Configure	General Setting SMBALERT# Mask De	General Setting SMBALERT# Mask Device Info    Phase Commands    Pin Strapping    All Config						
	VOUT Mask	STATUS_IOUT_Mask	STATU5_INPUT_Mask					
	7 Vout OV Fault	7 DUT OC Fault	7 Vin OVF					
	6 🗌 Vout OV Warning	6 Not supported	6 V Not-supported					
	5 Vout UV Warning	5 OI IOUT OC Warning	5 🗹 <del>Vin UVW</del>					
	4 Vout UV Fault	4 V Not-supported	4 Not supported					
	3 MAX/MIN Warn	3 V Not supported	3 Unit off: Insufficient Vin					
	2 TON_MAX Fault	2 Not supported	2 Not supported					
	Not supported							
	STATUS_TEMPERATURE_Mask	STATUS_CML_Mask	STATUS_OTHER_Mask 7					
	7 OT Fault	7 D Invalid Command	7 Not supported					
	6 🔲 OT Warning	6 🔲 Invalid Data	6 Not supported					
	5 Not supported	5 🔲 PEC Fault	5 Not supported	=				
	4 Not supported	4 🗌 Memory Fault	4 Not supported					
	3 Not supported	3 Processor Fault	3 Not supported					
	2 Not supported	2 Not supported	2 Not supported					
	1 Not supported	1 Other Comms Fault	1 Not supported					
	0 Not supported	O Other Memory/Logic Fault						
	STATUS_MFR_SPECIFIC_Mask							
	7 POR							
	6 SELF_CHECK							
	5 Not supported							
	4 Not supported							
	3 🔲 RESET							
	2 🔲 BCX							
	1 V 5YNC							
	0 Not supported							
	Key: Fault Bit that Contributes to SMBAL	ERT# Warning Bit that Contributes to SMBAL	ERT# Bit Masked from SMBALERT# Bit Not Supported	<u> </u>				
🌵 Configure				^				
🍥 Monitor								
🚸 Status	PMBus Log							
Fusion Digital Power Desi	gner v7.1.28.Beta TPS546D24A @ PMBus Addres	s 36d (24h) * Not Saved						

Figure 10-5. Configure – SMBALERT # Mask

# 10.6 Device Info

The device information, Write Protection options, the configuration of *Vout Scale Loop*, *Vout Transition Rate*, and *lout Cal Offset* are found on the *Device Info* tab (see Figure 10-6).

🚸 Configuration TP5546D2	24A @ PMBus Addr 36d (24h) / I2C Addr 72d (48h)		_ 🗆 🔀						
File Device Tools									
🖞 Write to Hardware 🗙 Discard Changes Store Config to NVM Restore NVM Config 🖁 🖧 Error Checking									
Configure	General Setting SMBALERT# Mask Device Info Phase Commands Pin Strapping All Config								
	Device Constants	Write Protect							
	IC Device ID:       0x5449546D2441 (TP5546D24A)         IC Device REV:       0x4000         PMBus Revision:       1.3,1.3 - Part I: 1.3, Part II: 1.3         Capability:       Maximum Supported Bus Speed:       1000 kHz         Packet Error Checking (PEC) Supported:       Yes         SMBALERT# Supported:       Yes         Whether the device has an SMBALERT# pin and supports the SMBALERT# pin and	Disable all writes except to the WRITE_PROTECT command     Disable all writes except to the WRITE_PROTECT, and OPERATION commands     Disable all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND commands     Disable all writes are all and							
	Format: Linear/DIREC								
	Identification	Calibration							
	MFR_MODEL: 0x000000	Vout Scale Loop: 0.500 V							
	MFR_REVISION: 0x000000	Vout Transition Rate: 1.0000 💬 mV/µs							
Configure			<						
🤣 Status	PMBus Log		<u> </u>						
Fusion Digital Power Designer vi	7.1.28.Beta   TPS546D24A @ PMBus Address 36d (24h)   * Not Saved								

Figure 10-6. Configure – Device Info



### 10.7 Phase Commands

Use the *Phase Command* tab (see Figure 10-7) to calibrate the *IOUT/Temp* of each phase.

👆 Configuration TP5546D2	Configuration TP5546D24A @ PMBus Addr 36d (24h) / I2C Addr 72d (48h)							
File Device Tools								
write to Haroware \ Uscaro Lhanges Store Lonng to NVM_Restore NVM Config   Error Checking								
Configure	Useneral Second    Smithubek I # mask    Device Info    Phase Commands    Pin Strapping    All Config							
	Calibration - Iout/Temp							
	Phase 0 Phase 1							
	Iout Cal Offset:	0.0000 💭 A	0.0000 🄶 A					
	Iout Cal Gain:	1.000	1.000					
	Iout OC Warn Limit:	40.0 💭 A	40.0 🔶 A					
	Iout OC Fault Limit:	52.0 💭 A	52.0 📩 A					
	Temp Warn Limit:	125 💭 °⊂	125 📩 °C					
	Temp Fault Limit:	150 💭 ℃	150 📩 °C					
🚸 Configure								<u>^</u>
Monitor								
Status	PMBus Log							
Fusion Digital Power Designer v	7.1.28.Beta TPS546D24A @ PMI	Bus Address 36d (24h) * Not S	aved					

### Figure 10-7. Phase Commands



# 10.8 All Config

Use the *All Config* tab (Figure 10-8) to configure all of the configurable parameters, which also shows other details like Hex encoding.

🚸 Configuration TP5546	D24A @ PMBus Addr 36d (24h) / I2C Addr 72	d (48h)						
File Device Tools								
1 Write to Hardware	Discard Changes Store Config to NVM Restore NV	M Config 🛛 💑	Error Checking					
Configure	General Setting SMBALERT# Mask Device	Info    Phase C	iommands    Pin Strap	ping All Confi	9			
Sort Parameters By:	Command	Code	¥alue/Edit	Hex/Edit	Command	Code	Value/Edit	Hex/Edit
Command Name	▼ Calibration				▼ Manufacturer Info			
Command Code	IOUT_CAL_GAIN phase ALL	0×38	1.000 😴	0×C880	CAPABILITY	0×19	0xD0 🖂	0xD0
Group by Category	IOUT_CAL_OFFSET phase ALL	0×39	A 💭 0000.0	0×E000	MFR_MODEL	0×9A		0×00 🗸
	VOUT_SCALE_LOOP	0x29	0.500 🗸	0xC840	MFR_REVISION	0×9B		0x00 🗸
	VOUT_TRIM	0x22	V 🔪 0.00000.0	0×0000	MFR_SERIAL	0×9E		0x00 🗸
	Configuration				PMBUS_REVISION	0×98	0x33 🛩	0x33
	FREQUENCY_SWITCH	0x33	550 🗹 kHz	0x0226	▼ On/Off Configuration			
	IC_DEVICE_ID	0×AD	0x54495 🔽	0x54 ∨	ON_OFF_CONFIG phase ALL	0×02	0x17 🔽	0x17
	IC_DEVICE_REV	0×AE	0×4000 🗸	0x4000 🗸	OPERATION	0×01	0x04 🗸	0x04
	INTERLEAVE	0x37	Group ID 🔽	0x0020	TOFF_DELAY	0x64	0.0 🐳 ms	0xF800
	MISC_OPTIONS [MFR 29]	0×ED	PEC: Fals 🔽	0×0000	TOFF_FALL	0×65	0.50 🌩 ms	0×F002
	PGOOD_CONFIG [MFR 19]	0×E3	PGood O 🗸	0x009F	TON_DELAY	0×60	0.0 💭 ms	0xF800
	PIN_DETECT_OVERRIDE [MFR 30]	0×EE	Stack Co 🗸	0×1F2F	TON_MAX_FAULT_LIMIT	0×62	0 🗸 ms	0×F800
	SMBALERT_MASK_CML	0×1B	00000000 🗸	0x00	TON_MAX_FAULT_RESPONSE	0x63	Click 🗸	0x3B
	SMBALERT_MASK_INPUT	0×1B	11101000 🖂	0×E8	TON_RISE	0×61	3.00 🐥 ms	0xF00C
	SMBALERT_MASK_IOUT	0×1B	00011000 🖂	0×18	▼ Status			
	SMBALERT_MASK_MFR_SPECIFIC	0×1B	01000010 🖂	0x42	NVM_CHECKSUM [MFR 32]	0×F0	Checksu 🗸	0×E9E0
	SMBALERT_MASK_OTHER	0×1B	00000001 🖂	0×01	READ_IOUT phase ALL	0x8C	-0.52 A	0×B5F0
	SMBALERT_MASK_TEMPERATURE	0×1B	00000000 🖂	0×00	READ_TEMPERATURE_1 phase ALL	0x8D	23 °C	0×0017
	SMBALERT_MASK_VOUT	0×1B	00000010 🖂	0x02	READ_VIN phase ALL	0×88	3.301 V	0xC34D
	STACK_CONFIG [MFR 28]	0×EC	Bcx Stop 🗸	0×0001	READ_YOUT phase ALL	0×8B	0.009766 V	0×0005
	SYNC_CONFIG [MFR 20]	0xE4	SYNC_DI	0×F0	STATUS_BYTE	0×78	01000000 🗸	0x40
					STATUS CMI	0×7E	0000000	0,000
				ш				/
A Configure								
Monitor								
🧄 Status	PMBus Log							
Fusion Digital Power Designer	r v7.1.28.Beta TPS546D24A @ PMBus Address 36d	l (24h) × Not S	aved					

Figure 10-8. Configure – All Config



# 10.9 Pin Strapping

Use the *Pin Strapping* tab (Figure 10-8) to aid in selection of external pin strapping resistors used to program some of the PMBus commands at power-up. The *EEPROM Value* column shows the values currently configured to the related PMBus commands.



Figure 10-9. Configure – Pin Strapping



### 10.10 Monitor

When the *Monitor* screen (Figure 10-10) is selected, the screen changes to display real-time data of the parameters that are measured by the device. This screen provides access to:

- Graphs of Vout, Iout, Vin, Pout, and Temperature
- Start and Stop Polling which turns ON or OFF the realtime display of data
- Quick access to On/Off Config
- Control pin activation and OPERATION command
- · Margin control
- Clear Fault: Selecting Clear Faults clears any prior fault flags.

With two devices stacked together, the *lout* reading is the total load supported by both devices. There is also an *lout* which shows the current in each phase.

Configuration TP5546D2	4A @ PMBus Addr 36d (24h) / I2C Addr 72d (48h)					
File Device Tools						
$1$ Write to Hardware $\times$ Dis	oard Changes Store Config to NVM Restore NVM Config 🤯 Error Checking					
Monitor	PMBus Readings	Vin - Input Voltage 🛛 🗶	Vout - Output Voltage			
Show/Hide Plots:	Total phases Ph0 Ph1	Max Y: 26.00 😴 Min Y: 0.00 😴	Max Y: 1.00 🐑 Min Y: 0.00 👻			
Vin Vout	Vin 12.000 V 12.016 V 11.984 V	OVF: 21 ↔ V UVW: 2.50 ↔ V	OVF: 0.917404 💭 adj = 0.733 V			
Vout-phase Vin-phase	Vout 0.796875 V 0.796875 V 0.925781 V	VinON: 2.75 🐳 V VinOFF: 2.50 🐳 V	OVW: 0.870598 ⊕ adj = 0.695 V			
Pout(calc) 🗸 Temp	Tout 33.19 A 16.81 A 16.34 A	Write				
Temp-phase	Temp 31 °C 30 °C 30 °C	26.00	vout: 0.798828 🕁 adj = 0.799 V			
<ul> <li>Fit All Plots on Screen</li> </ul>			UVW: 0.727058 adj = 0.581 V			
<ul> <li>Scale Plots to Screen</li> <li>Width</li> </ul>		20.80	UVF: 0.678692 📩 adj = 0.542 V Write			
Height: 200 🕀			1.00			
Width: 400 😔	Status Registers/Lines	15.60	0.80			
Show Warn & Fault Limit Editors	lout: OK		0.60			
Show Value Labels	Temp: OK	10.40				
on Plots	CML: OK	E 20	0.40			
Polling Rate: 500 👻 (msec)	Miso: OK Mfr. OK	5.20	0.20			
	SMBALERT# Not Asserted	0.00	0.00			
Stop Polling	Clear Faults	27:20 27:40 28:00 28:20	27:20 27:40 28:00 28:20			
	0-/0ff 5ff-	Jout - Output Current				
		Max Y: 130.00 💭 Min Y: -1.00 💭	Max Y: 188.00 🛱 Min Y: 0.00 🛱			
	0x17 Mode: CONTROL Pin Only; Control: Active High, Turn off Immediately	OCE: 1040 A OCW: 80.0 A Write				
		130.00	188.00			
		103.80	150.40			
	Immediate Off	10000	10010			
	Soft Off					
	Margining:  None Margin Fault Action:  Act on Fault	77.60	112.80			
	O Low <ul> <li>Ignore Fault</li> </ul>					
	() High	51.40	75.20			
	Control Line (USB)					
	High	25.20 33.19 A	37.60			
	OLOW		<b>31.0</b> °C			
		-1.00	0.00			
		27:20 27:40 28:00 28:20	27:20 27:40 28:00 28:20			
Configure						
🚸 Monitor			$\sim$			
🤣 Status	PMBus Log					
Fusion Digital Power Designer v	.1.28.Beta TPS546D24A @ PMBus Address 36d (24h) * Not Saved					

Figure 10-10. Monitor Screen



# 10.11 Status

Selecting Status screen from lower left corner (Figure 10-11) shows the status of the device.



#### Figure 10-11. Status Screen

# **11 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

C	hanges from Revision * (December 2019) to Revision A (August 2021)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	4
•	Updated user's guide title	4

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