

Using the TPS51215AEMV

This user's guide contains information for the TPS51215A as well as support documentation for the TPS51215AEMV evaluation module. Included are the performance specifications, schematic, and the List of Materials.

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1 Introduction

The TPS51215A is a single phase, D-CAP2 synchronous buck controller with 2-bits VID inputs that can select up to four independent output voltage with fixed voltage transition slew rate. [Table 1](#) displays detailed input and output information.

The TPS51215A supports all POS-CAP and all ceramic MLCC output capacitor options in applications where remote sense is a requirement.

The TPS51215A provides full protection suite, including OVP, UVP, OCL, V5IN UVLO and OTP. It supports the conversion voltage up to 28 V. The devices are available in 3.0-mm x 3.0-mm 20 pin QFN package and the die operating temperature is specified from -40C to 125C.

Table 1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE (V_{IN}) Range	OUTPUT CURRENT (I_{OUT}) RANGE
TPS51215AEVM	5 V to 24 V	I_{DC} = 0 A to 16 A, I_{Peak} = 0 A to 30 A

2 Performance Specification Summary

A summary of the TPS51215AEVM performance specifications is provided in [Table 2](#). The TPS51215AEVM is designed and tested for V_{IN} = 5 V to 24V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS51215AEVM Performance Specifications Summary

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	5	12	24	V
I_{OUT}	Output Loading	0	16	30	A
F_{SW}	Switching Frequency		600		KHz
V_{OUT}	0 V (VID1 = 0, VID0 = 0)		0		V
	1.1 V (VID1 = 0, VID0 = 1)		1.1		
	1.65 V (VID1 = 1, VID0 = 0)		1.65		
	1.77 V (VID1 = 1, VID0 = 1)		1.77		

3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS51215AEVM. The section also includes test results typical for the evaluation modules.

3.1 Input/Output Connections

The TPS51215AEVM is provided with input/output connectors and Headers description shown in [Table 3](#), and Output Voltage selection shown in [Table 4](#), and Test points shown in [Table 5](#). A power supply capable of supplying greater than 16A must be connected to J2. The load must be connected to J3. The maximum load current capability is 30 A. Wire lengths must be minimized to reduce losses in the wires.

Table 3. Connectors and Headers

#	FUNCTIONS	COMMENT
J1	5V power input for 5VIN	
J2	VIN power input	
J3	Connects with VOUT loading	
JP1	Mode pin	For 51215A, connect Mode pin to 5VIN. Short JP1-2 and JP1-3.
JP2	VID0 control connector	Short JP2-2 and JP2-3 to make VID0 = 1, Short JP2-1 and JP2-2 to make VID0 = 0.
JP3	EN control connector	Short JP3-1 and JP3-2 to make EN connected to GND, Short JP3-2 and JP3-3 to make EN connected to 5VIN.
JP4	VID1 control connector	Short JP4-2 and JP4-3 to make VID1 = 1, Short JP4-1 and JP4-2 to make VID1 = 0.

Table 4. Output Voltage selection

JP4	VID1	JP2	VID0	VOUT
JP4-1 and JP4-2	0	JP2-1 and JP2-2	0	0 V
JP4-1 and JP4-2	0	JP2-2 and JP2-3	1	1.1 V
JP4-2 and JP4-3	1	JP2-1 and JP2-2	0	1.65 V
JP4-2 and JP4-3	1	JP2-2 and JP2-3	1	1.77 V

Table 5. Test Points

TP#	NAME	SIGNAL
TP1	5VIN	External 5V power for 5VIN
TP2	GND	GND
TP3	VIN	VIN
TP4	VIN	VIN
TP5	TRIP	OC setting
TP6	SLEW	Soft start control
TP7	VSNS	VOUT remote sense
TP8	DRVL	Low-side drive signal
TP9	DRVH	High-side drive signal
TP10	GND	GND
TP11	GND	GND
TP12	LOOP	Change R9 to ~51 ohm for loop test
TP13	LX	Switching node
TP14	VOUT	VOUT
TP15	VOUT	VOUT
TP16	VREF	Reference output
TP17	GND	GND
TP18	GND	GND
TP19	PGOOD	PGOOD output
TP20	GSNS	GND for VOUT remote sense
TP21	GND	GND
TP22	GND	GND
TP23	GND	GND
TP24	GND	GND
TP25	GND	GND
TP26	GND	GND
TP27	GND	GND
TP28	VID0	VID0 input
TP29	EN	Enable signal input
TP30	VID1	VID1 input

3.2 Start-Up Procedure

1. Jump the JP2 and JP4 accordingly or connect external drive signals to the TP28 and TP30.
2. Jump JP1 accordingly
3. Apply proper DC voltage to J1 and J2. Apply J2 12V with external power source first and then apply J1 5V with another power source.
4. Jump the JP3 accordingly or connect external drive signals to the TP29.
5. Check the output.
6. Apply loading to the output connectors.
7. Check the output again.

3.3 Power-Up

The TPS51215A EVM power up waveform is shown in Figure 1.

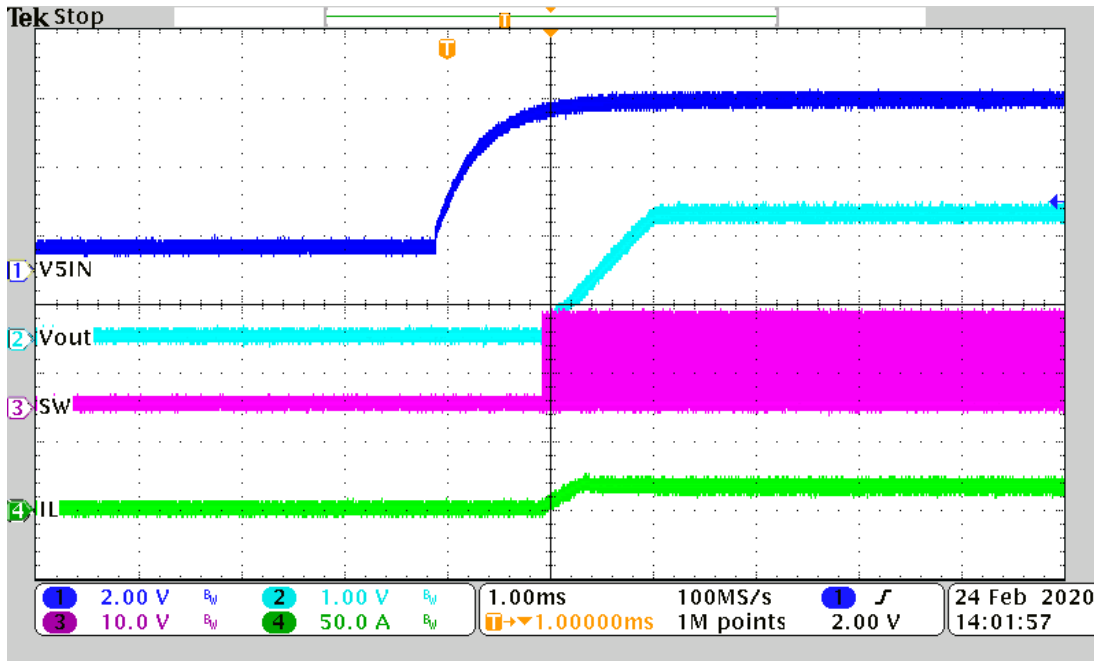


Figure 1. TPS51215A EVM Power Up, $I_{out}=16\text{ A}$, $V_{out}=1.77\text{ V}$

3.4 Power-Down

The TPS51215A EVM power down waveform is shown in Figure 2.

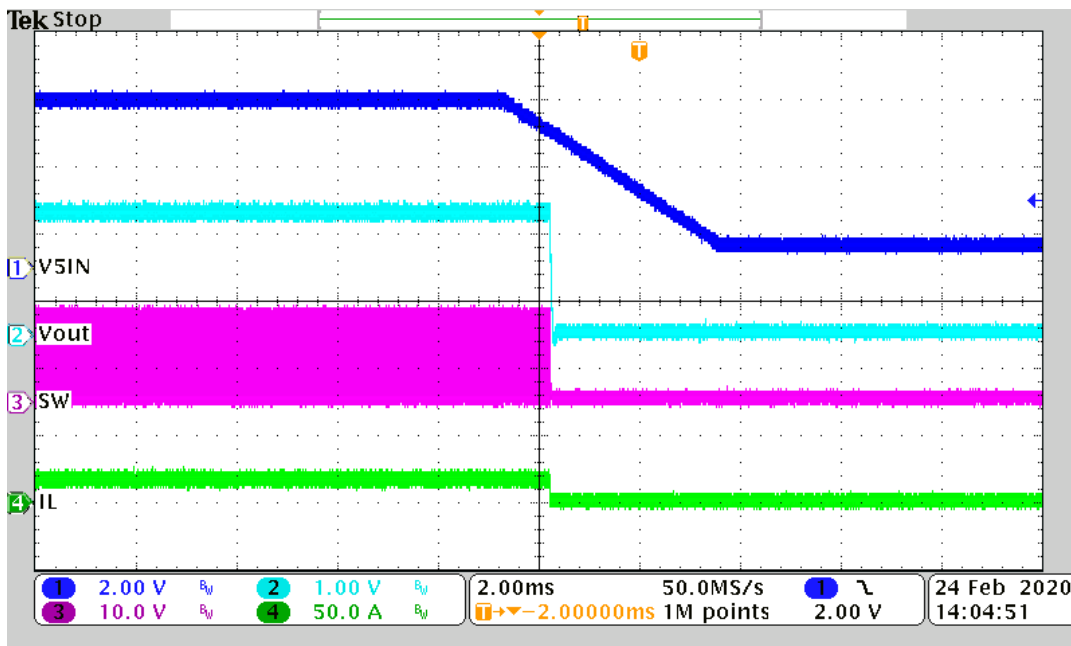


Figure 2. TPS51215A EVM Power Down, $I_{out}=16\text{ A}$, $V_{out}=1.77\text{ V}$

4 Board Layout

This section provides a description of the TPS51215AEVM board layout and layer illustrations. The board layout for the TPS51215AEVM is shown in [Figure 4 ~ Figure 11](#). The top and bottom are 2-oz. copper and internal layers are 1-oz. copper.

VIN capacitor(s), VOUT capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.

All sensitive analog traces and components such as VSNS, SLEW, VID, VREF and TRIP should be placed away from high-voltage switching nodes such as SW, DRVH, DRVL or BST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.

Connect VSNS directly to the output voltage sense point at the load device. Connect GSNS to ground return points at the load device. Routing as differential lines to avoid noise coupling.

Connect the over current setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.

Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance.

The PCB trace defined as SW node, which connects to the source of the switching MOSFET, the drain of the rectifying MOSFET and the high-voltage side of the inductor, should be as short and wide as possible.

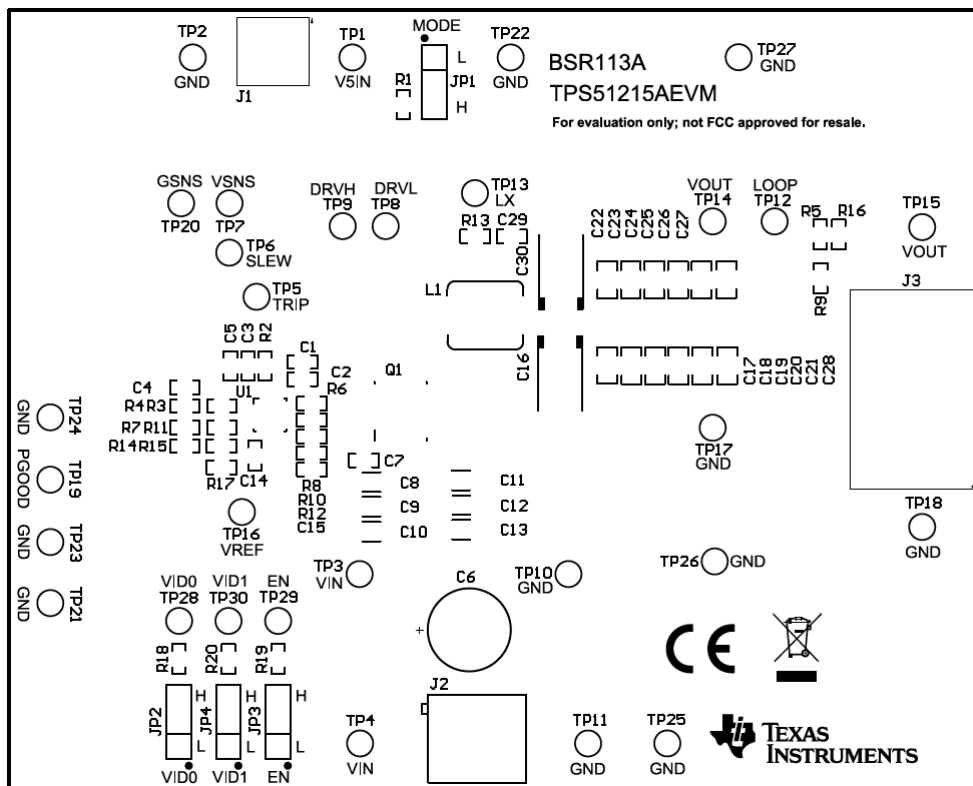


Figure 3. Top Assembly

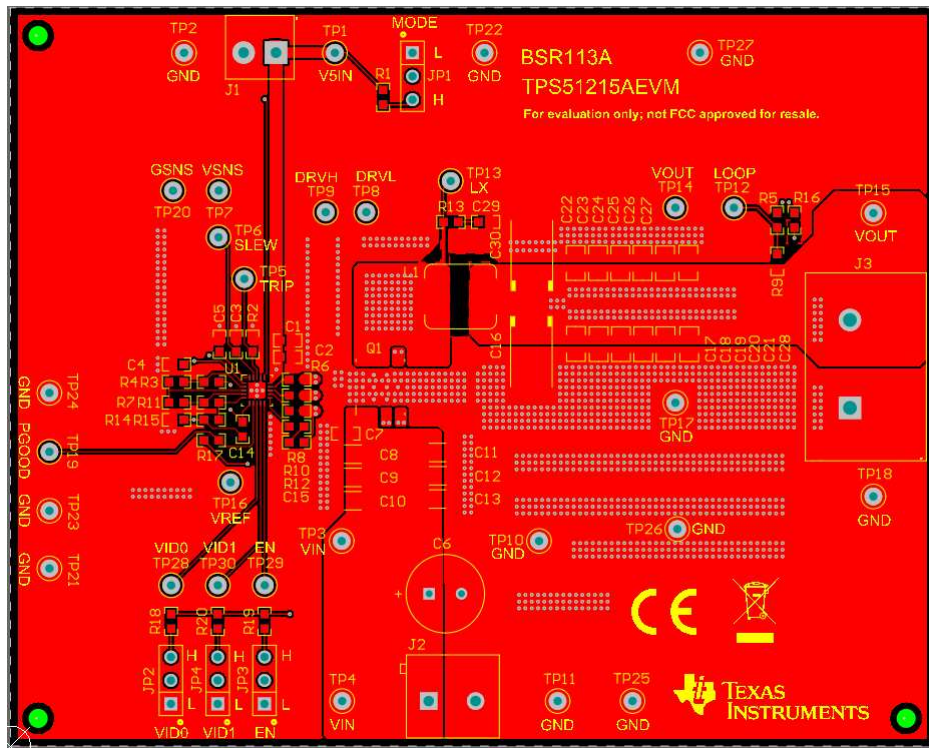


Figure 4. Top Layer

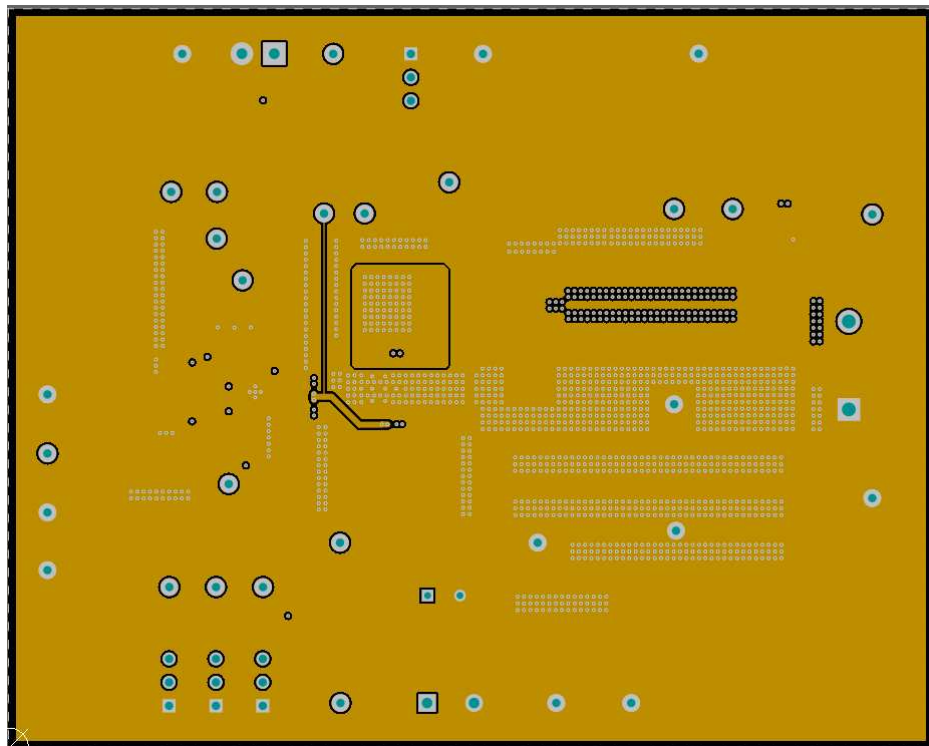


Figure 5. Inner1 Layer

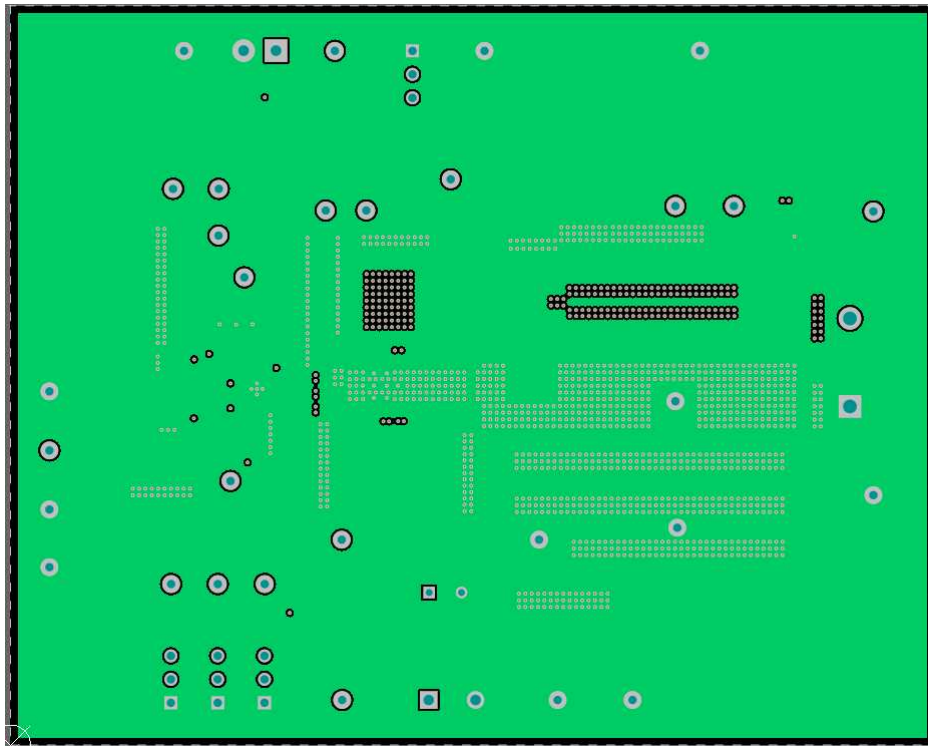


Figure 6. Inner2 Layer

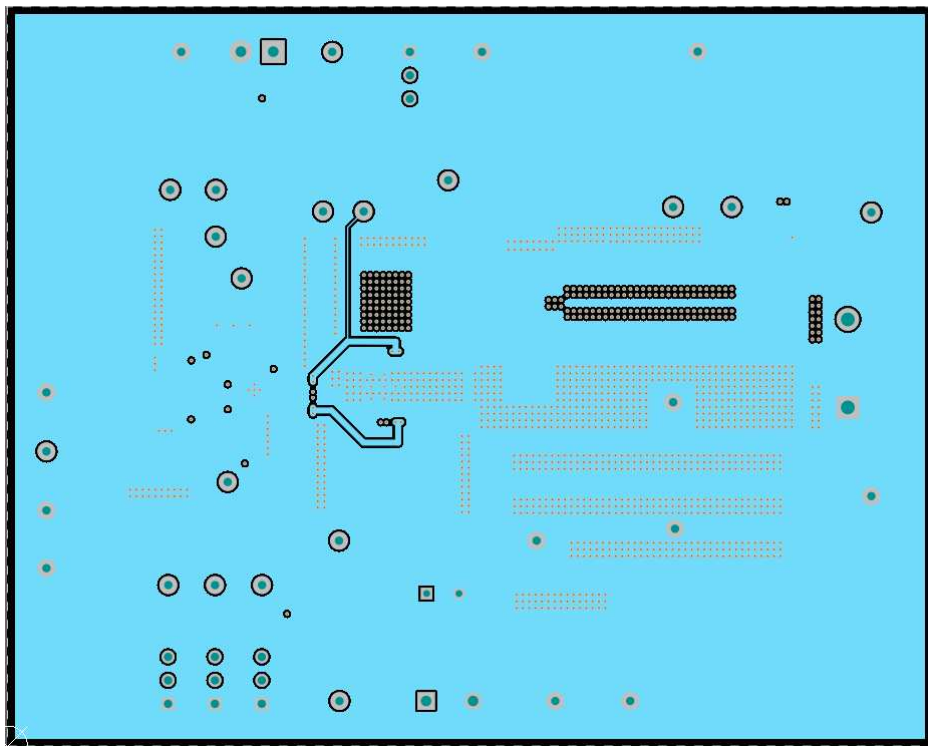


Figure 7. Inner3 Layer

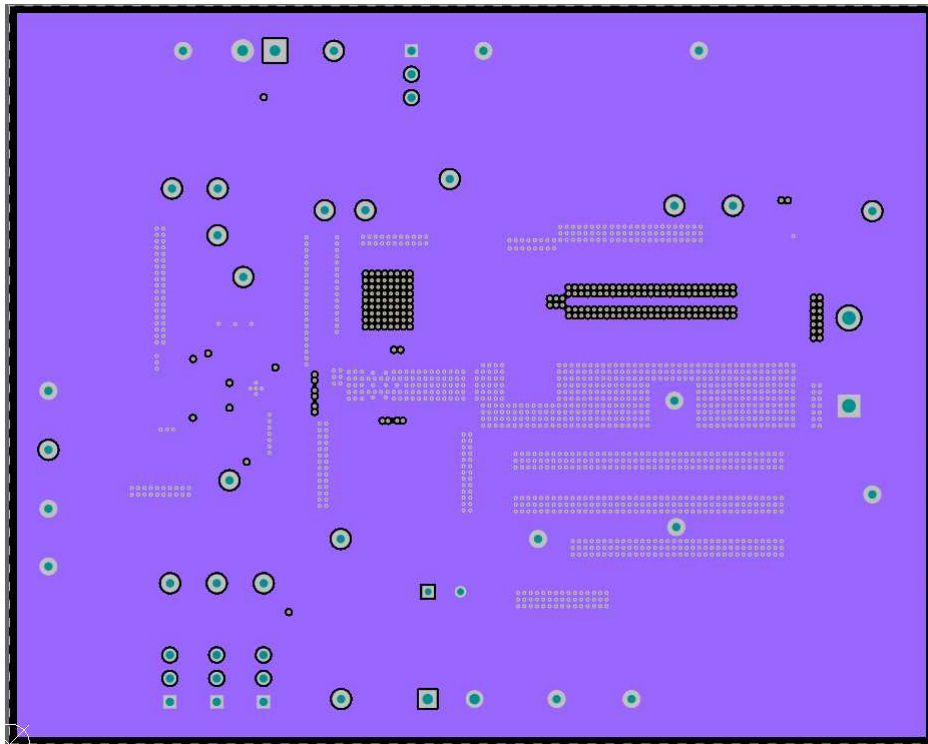


Figure 8. Inner4 Layer

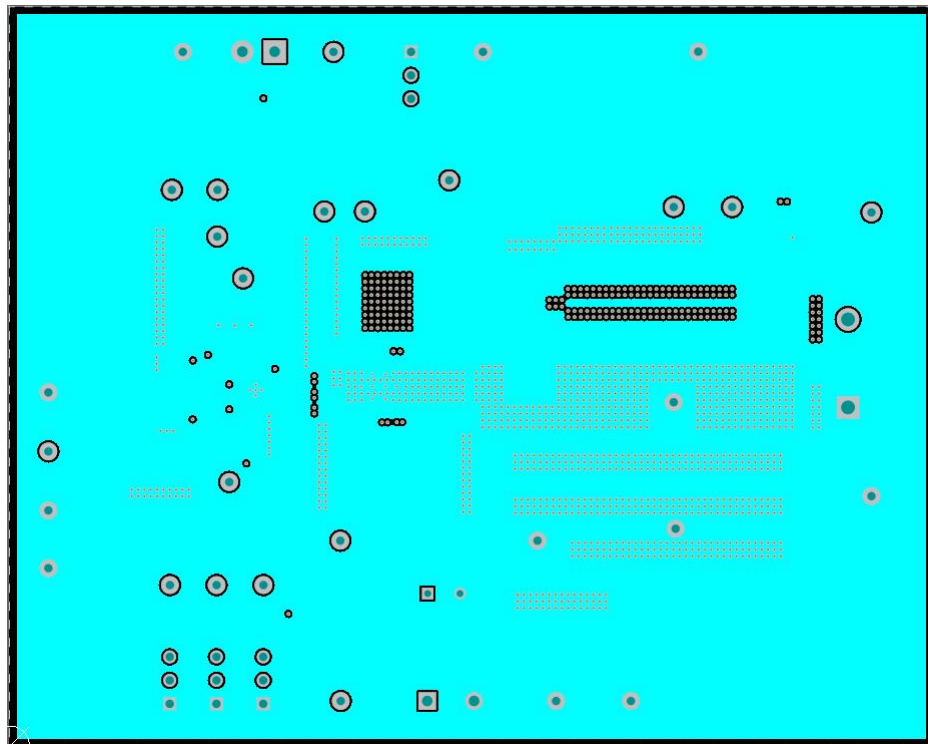


Figure 9. Inner5 Layer

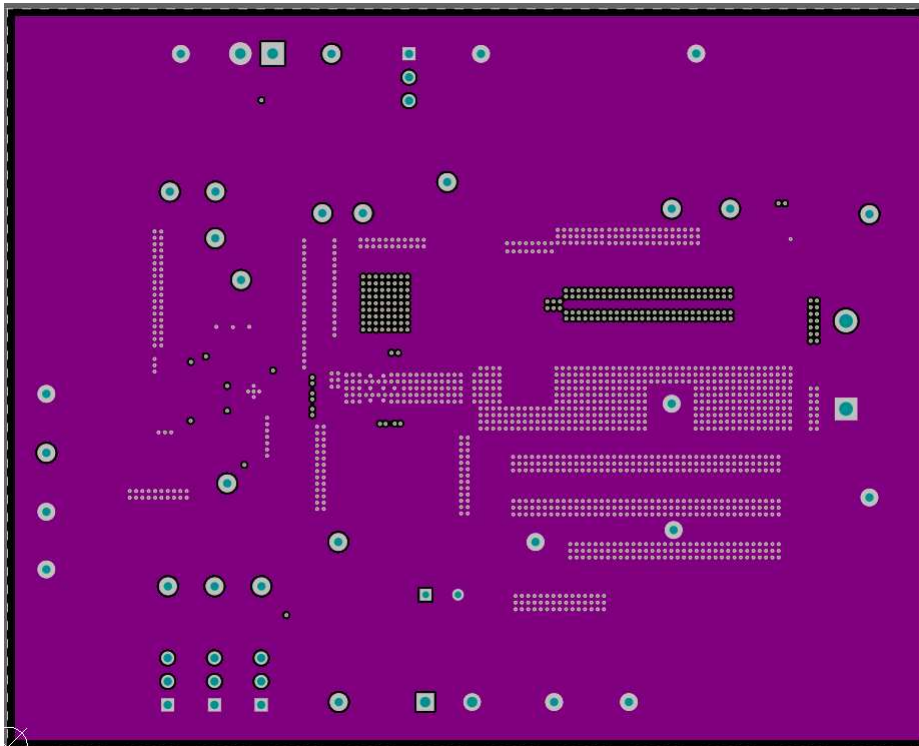


Figure 10. Inner6 Layer

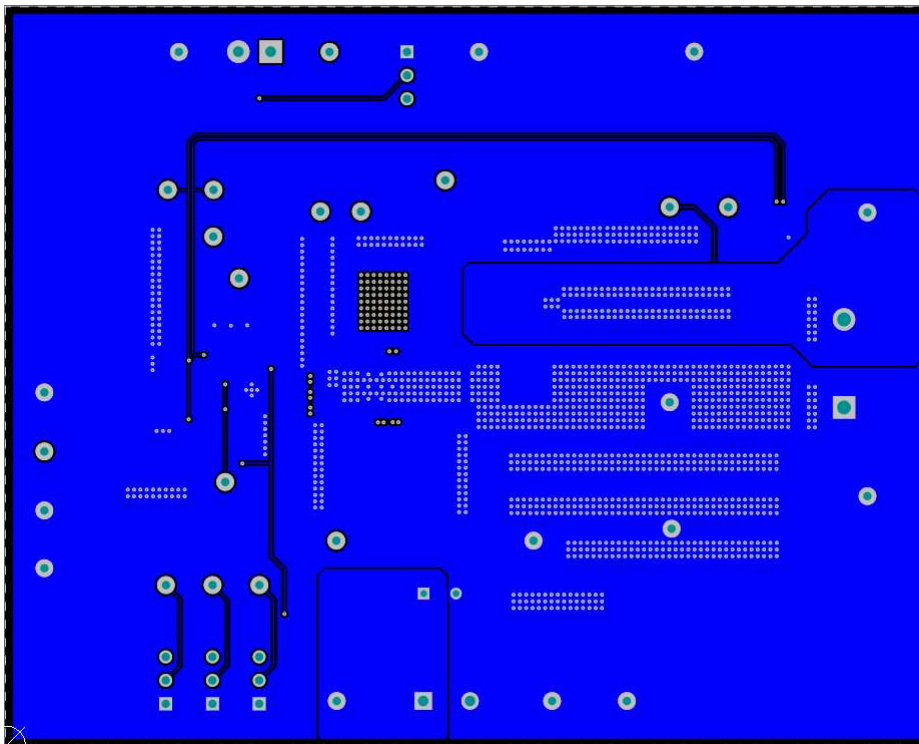


Figure 11. Bottom Layer

5 Board Profile, Schematic, List of Materials and Reference

5.1 Board Profile

Figure 12 is the top view for the TPS51215AEMV.

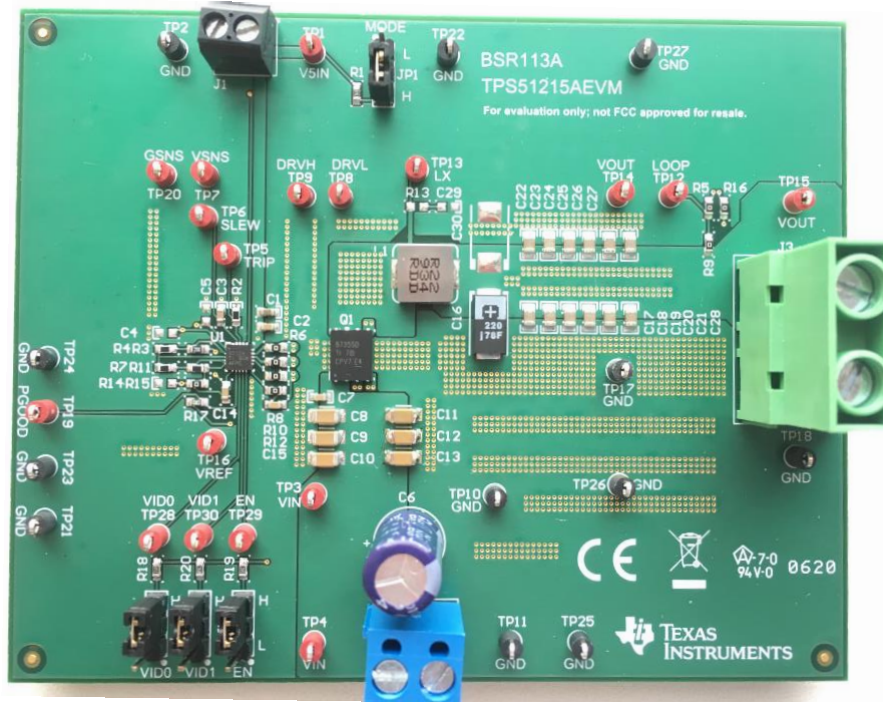


Figure 12. Top View of TPS51215AEMV

Figure 13 is the bottom view for the TPS51215AEMV.

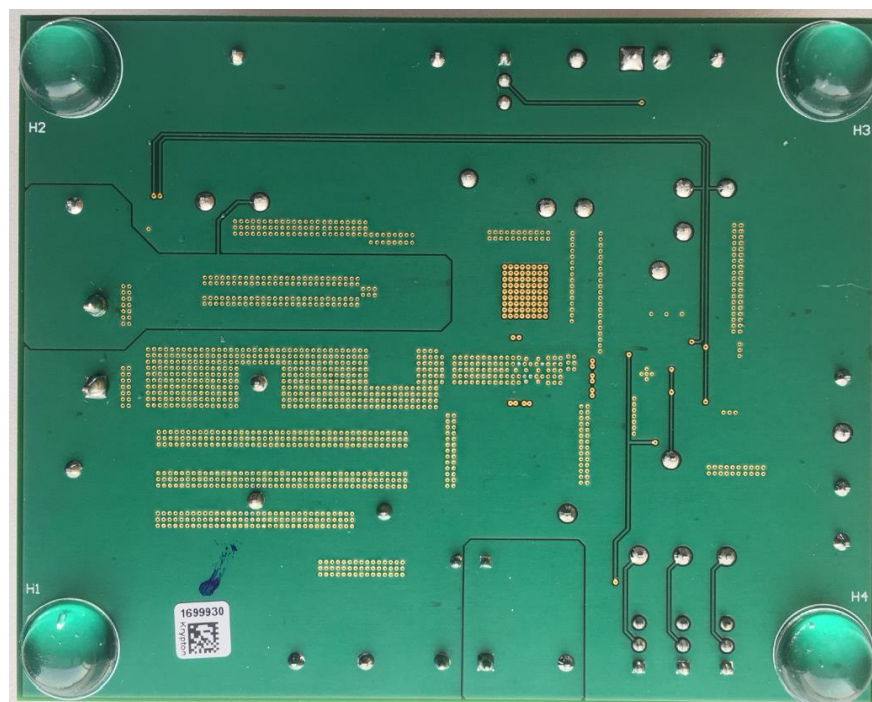


Figure 13. Bottom View of TPS51215AEMV

5.2 Schematic

Figure 14 is the schematic for the TPS51215AEMV.

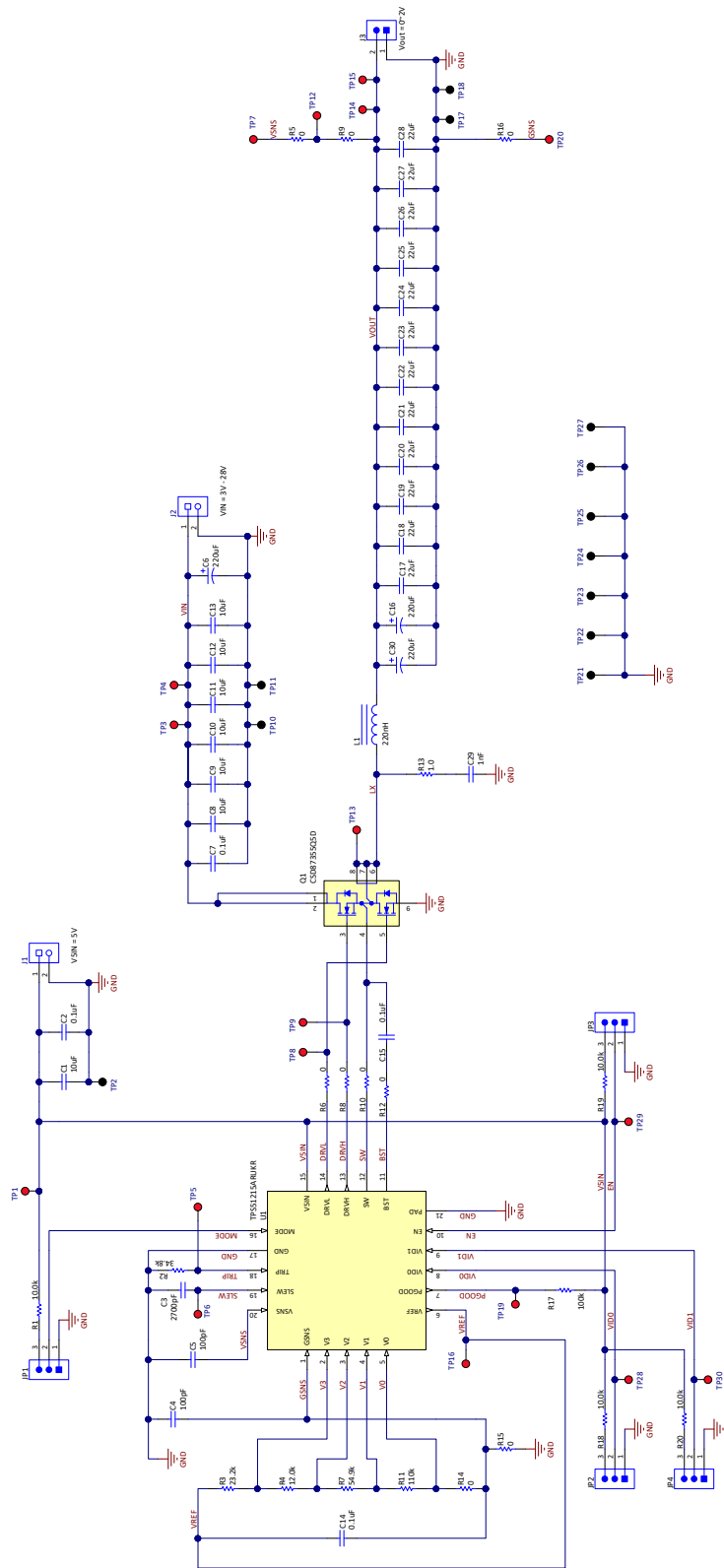


Figure 14. TPS51215AEMV Schematic

5.3 List of Materials

Table 6 displays the TPS51215AEVM bill of materials.

Table 6. List of Materials

DESIGNATOR	QUANTITY	DESCRIPTION	PART NUMBER	MANUFACTURER
PCB	1	Printed Circuit Board	BSR113	
C1	1	Capacitor, ceramic, 10 uF, 10 V, +/- 20%, X5R, 0603	GRM188R61A106MAALD	MuRata
C2, C7, C14, C15	4	Capacitor, ceramic, 0.1 uF, 50 V, +/- 10%, X7R, 0603	C1608X7R1H104K080AA	TDK
C3	1	Capacitor, ceramic, 2700 pF, 100 V, +/- 5%, X7R, 0603	06031C272JAT2A	AVX
C6	1	Capacitor, AL, 220 uF, 35 V, +/- 20%, AEC-Q200 Grade 2, TH	ELXZ350ELL221MH15D	Chemi-Con
C8, C9, C10, C11, C12, C13	6	Capacitor, ceramic, 10 uF, 35 V, +/- 20%, X5R, 1206	C3216X5R1V106M160AB	TDK
C16	1	Capacitor, AL, 220 uF, 35 V, +/- 20%, AEC-Q200 Grade 2, TH	6TPF220M5L	Panasonic
C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28	12	Capacitor, ceramic, 22 uF, 6.3 V, +/- 20%, X5R, 0805	GRM21BR60J226ME39L	MuRata
H1, H2, H3, H4	4	Bump, hemisphere, 0.44 X 0.20, Clear	SJ-5303 (CLEAR)	3M
J1	1	Terminal Block, 3.5mm Pitch, 2x1, TH	ED555/2DS	On-Shore Technology
J2	1	Terminal Block, 5.08 mm, 2x1, Brass, TH	ED120/2DS	On-Shore Technology
J3	1	Terminal Block, 30A, 9.52mm (.375) Pitch, 2-Pos, TH	OSTT7022150	On-Shore Technology
JP1, JP2, JP3, JP4	4	Header, 100 mil, 3x1, Gold, TH	PEC03SAAN	Sullins Connector Solutions
L1	1	Inductor, 220 nH, 20 A, 0.0029 ohm, SMD	CMLE063T-R22MS	Cyntec
Q1	1	MOSFET, 2-CH, N-CH, 30 V, 45 A, DQY0008A (LSON-CLIP-8)	CSD87355Q5D	Texas Instruments
R1, R18, R19, R20	4	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R2	1	RES, 34.8 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060334K8FKEA	Vishay-Dale
R3	1	RES, 23.2 k, 1%, 0.1 W, 0603	RC0603FR-0723K2L	Yageo
R4	1	RES, 12.0 k, 1%, 0.1 W, 0603	RC0603FR-0712KL	Yageo
R5, R6, R8, R9, R10, R12, R14, R16	8	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R7	1	RES, 54.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060354K9FKEA	Vishay-Dale
R11	1	RES, 110 k, 1%, 0.1 W, 0603	RC0603FR-07110KL	Yageo
R17	1	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo
SH-JP1, SH-JP2, SH-JP3, SH-JP4	4	Shunt, 100 mil, gold plated, black, 1x2	SNT-100-BK-G	Samtec
TP1, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP12, TP13, TP14, TP15, TP16, TP19, TP20, TP28, TP29, TP30	18	Shunt, 100mil, Gold plated, Black	5000	Keystone
TP2, TP10, TP11, TP17, TP18, TP21, TP22, TP23, TP24, TP25, TP26, TP27	12	Test Point, Miniature, Red, TH	5001	Keystone
U1	1	High Performance, Single Phase D CAP2 Controller with 2 bit VID, RUK0020B (WQFN-20)	TPS51215ARUKR	Texas Instruments
C4, C5	0	Capacitor, ceramic, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	06035A101JAT2A	AVX
C29	0	Capacitor, ceramic, 1000 pF, 50 V, +/- 5%, X7R, 0603	CL10C102JB8NNNC	Samsung Electro-Mechanics
C30	0	Capacitor, Tantalum Polymer, 220 uF, 6.3 V, +/- 20%, 0.005 ohm, 7.3x4.3mm SMD	6TPF220M5L	Panasonic

Table 6. List of Materials (continued)

DESIGNATOR	QUANTITY	DESCRIPTION	PART NUMBER	MANUFACTURER
R13	0	RES, 1.0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031R00JNEA	Vishay-Dale
R15	0	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo

Notes: Unless otherwise noted in the Alternate Part Number and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.

5.4 Reference

1. *TPS51215A, 3-28Vin, Synchronous Step-Down Voltage Regulator Controller Datasheet* ([SLU5DW9](#))

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