



ABSTRACT

The Texas Instruments LMR50410EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMR50410 wide-input synchronous buck regulator. This document describes the setup, input/output connections of the EVM, board layout, schematic, and bill of materials.

Table of Contents

1 Introduction	2
2 Setup	3
2.1 Input/Output Connector Description.....	3
2.2 Adjusting the Output Voltage.....	3
3 LMR50410EVM Schematic	4
4 Board Layout	5
5 Bill of Materials	6

List of Figures

Figure 1-1. LMR50410EVM Board.....	2
Figure 2-1. Enable Jumper Setting	3
Figure 3-1. LMR50410EVM Schematic.....	4
Figure 4-1. Top Layer.....	5
Figure 4-2. Middle Layer One.....	5
Figure 4-3. Middle Layer Two.....	5
Figure 4-4. Bottom Layer.....	5

List of Tables

Table 1-1. Device and Package Configurations.....	2
Table 5-1. LMR50410EVM Bill of Materials.....	6

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The Texas Instruments LMR50410EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMR50410 wide-input buck regulator.

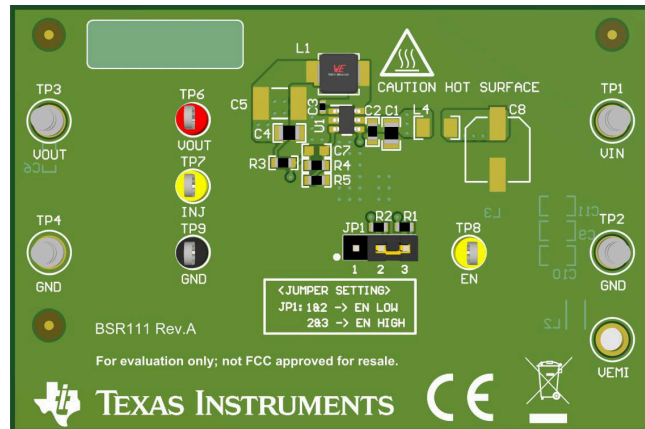


Figure 1-1. LMR50410EVM Board

EVM Features

- 4-V to 36-V input voltage range
- Default 3.3-V output
- Up to 1-A output current
- 700-kHz switching frequency
- Hiccup mode short current protection
- Internal compensation

The EVM contains one DC/DC converter (see [Table 1-1](#)).

Table 1-1. Device and Package Configurations

CONVERTER	EVM	DEVICE	PACKAGE
U1	LMR50410EVM	LMR50410	SOT23-6

2 Setup

This section describes the jumpers and connectors on the EVM and how to properly connect, set up, and use the LMR50410EVM.

2.1 Input/Output Connector Description

VIN — Terminal TP1 – Power input terminal for the converter. Adjacent to it is the GND reference ground. Use this terminal to attach the EVM to a cable harness.

VOUT — Terminal TP3 – Regulated output voltage for the converter. Adjacent to it is the GND reference ground.

GND — Terminal TP2, TP4 – Ground reference for the converter. Use these terminals to attach the EVM to a cable harness.

ENABLE SETTING — Jumper JP1 – Used to enable the switch-mode converter. The device will be enabled when the EN pin is high, and disabled when low.

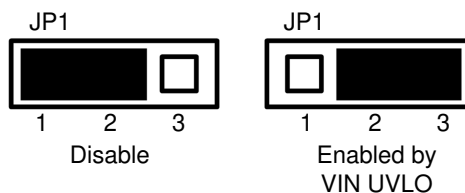


Figure 2-1. Enable Jumper Setting

Testpoint — TP6, TP7, TP9 – Test points used for loop response measurements

2.2 Adjusting the Output Voltage

If outputs need to be configured, adjust the feedback resistors using the [Equation 1](#).

$$V_{OUT} = V_{REF} \times (1 + (R4 / R5)) \tag{1}$$

where

- V_{REF} is 1.0 V

3 LMR50410EVM Schematic

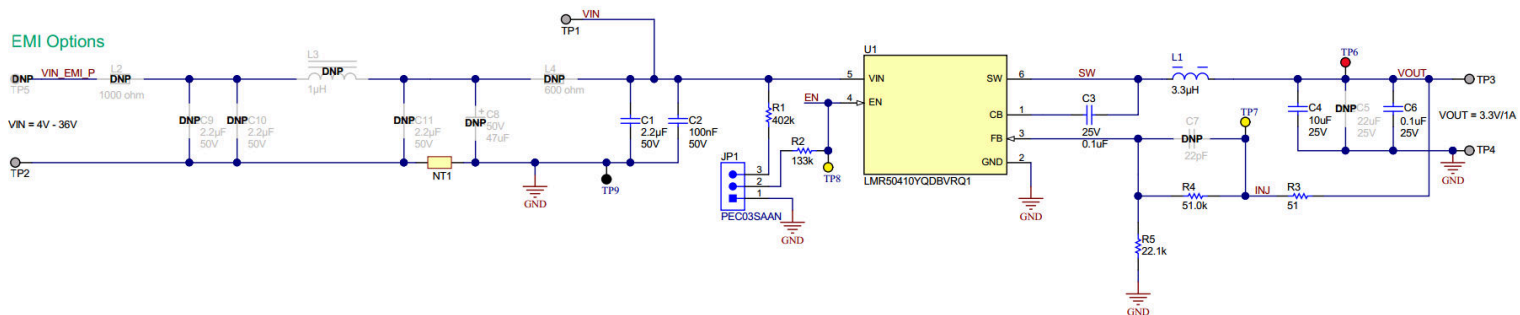


Figure 3-1. LMR50410EVM Schematic

4 Board Layout

Figure 4-1 to Figure 4-4 show the board layout for the LMR50410EVM. The PCB consists of a 4-layer design. The board size is 46-mm x 69-mm, 2-oz copper planes are applied on top and bottom layers, 1-oz copper planes are applied on middle layers.

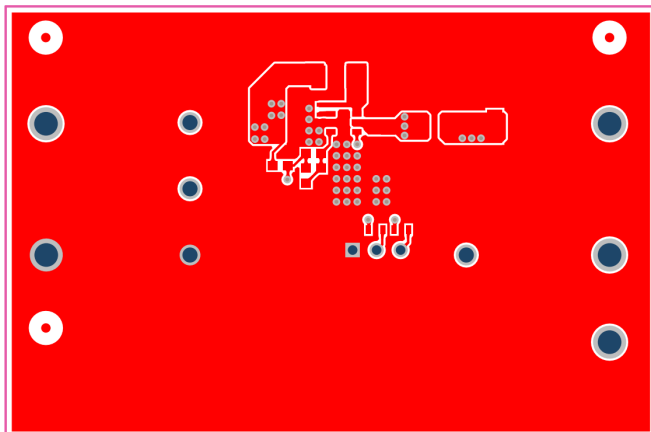


Figure 4-1. Top Layer

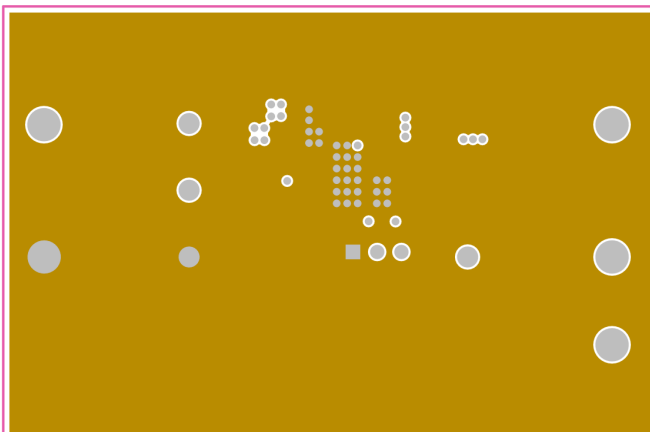


Figure 4-2. Middle Layer One

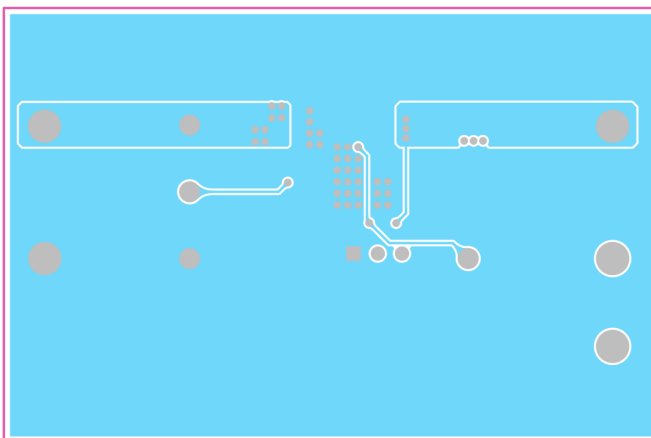


Figure 4-3. Middle Layer Two

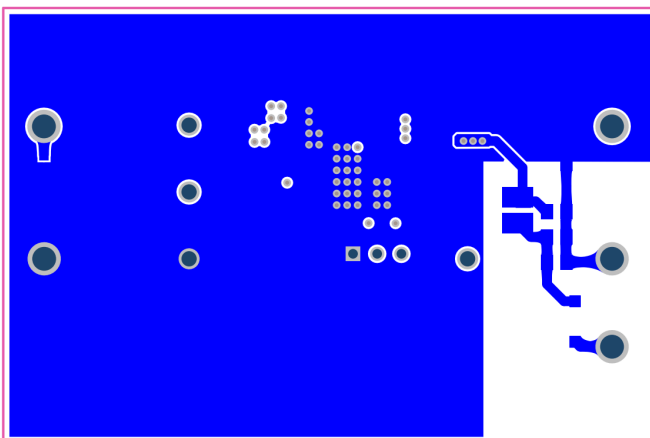


Figure 4-4. Bottom Layer

5 Bill of Materials

Table 5-1. LMR50410EVM Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1	1	2.2 μ F	CAP, CERM, 2.2 μ F, 50 V, \pm 10%, X7R, 0805	0805		
C2	1	0.1 μ F	CAP, CERM, 0.1 μ F, 50 V, \pm 10%, X7R, 0603	0603		
C3	1	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, \pm 10%, X7R, 0402	0402		
C4	1	10 μ F	CAP, CERM, 10 μ F, 25 V, \pm 10%, X7R, 0805	0805		
C6	1	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, \pm 10%, X7R, 0603	0603		
JP1	1		Header, 100 mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin		
L1	1		3.3- μ H Shielded Molded Inductor 2.5-A 76-m Ω Max Nonstandard	SMT_IND_4MM06_4MM06	74437324033	Wurth Electronics
R1	1	402 k	RES, 402 k, 1%, 0.1 W, 0603	0603		
R2	1	133 k	RES, 133 k, 1%, 0.1 W, 0603	0603		
R3	1	51	RES, 51, 5%, 0.1 W, 0603	0603		
R4	1	51.0 k	RES, 51.0 k, 1%, 0.1 W, 0603	0603		
R5	1	22.1 k	RES, 22.1 k, 1%, 0.1 W, 0603	0603		
SH-J1	1	1x2	Shunt, 100 mil, Gold plated, Black	Shunt		
TP1, TP2, TP3, TP4	4		Terminal, Turret, TH, Double	Keystone1502-2		
TP6	1		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint		
TP7, TP8	2		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint		
TP9	1		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint		
U1	1		LMR50410YQDBVRQ1, DBV0006A (SOT-23-6)	DBV0006A	LMR50410YQDBVRQ1	Texas Instruments
C5	0	22 μ F	CAP, CERM, 22 μ F, 25 V, \pm 20%, X7R	1812		
C7	0	22 pF	CAP, CERM, 22 pF, 50 V, \pm 5%, C0G/NP0, 0603	0603		
C8	0	47 μ F	CAP, AL, 47 μ F, 50 V, \pm 20%, 0.6 Ω , SMD	F80		
C9, C10, C11	0	2.2 μ F	CAP, CERM, 2.2 μ F, 50 V, \pm 10%, X7R, 0805	0805		
L2	0	1000 Ω	Ferrite Bead, 1000 Ω at 100 MHz, 1.5 A, 1806	1806	BLM41PG102SN1L	MuRata
L3	0	1 μ H	Inductor, Shielded, Metal Composite, 1 μ H, 2.9 A, 0.048 Ω , SMD	2x1.6mm	DFE201612E-1R0M	MuRata
L4	0	600 Ω	Ferrite Bead, 600 Ω at 100 MHz, 1.5 A, 1206	1206	BLM31PG601SH1L	MuRata
TP5	0		Terminal, Turret, TH, Double	Keystone1502-2		

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated