EVM User's Guide: TPS543B25TEVM

TPS543B25T SWIFT™ Step-Down Converter Evaluation Module

Description

The TPS543B25TEVM is designed to provide a quick setup to evaluate TPS543B25T device and gain familiarity. This evaluation module includes one design with the TPS543B25T and feature two M2x0.4 threaded spacers.

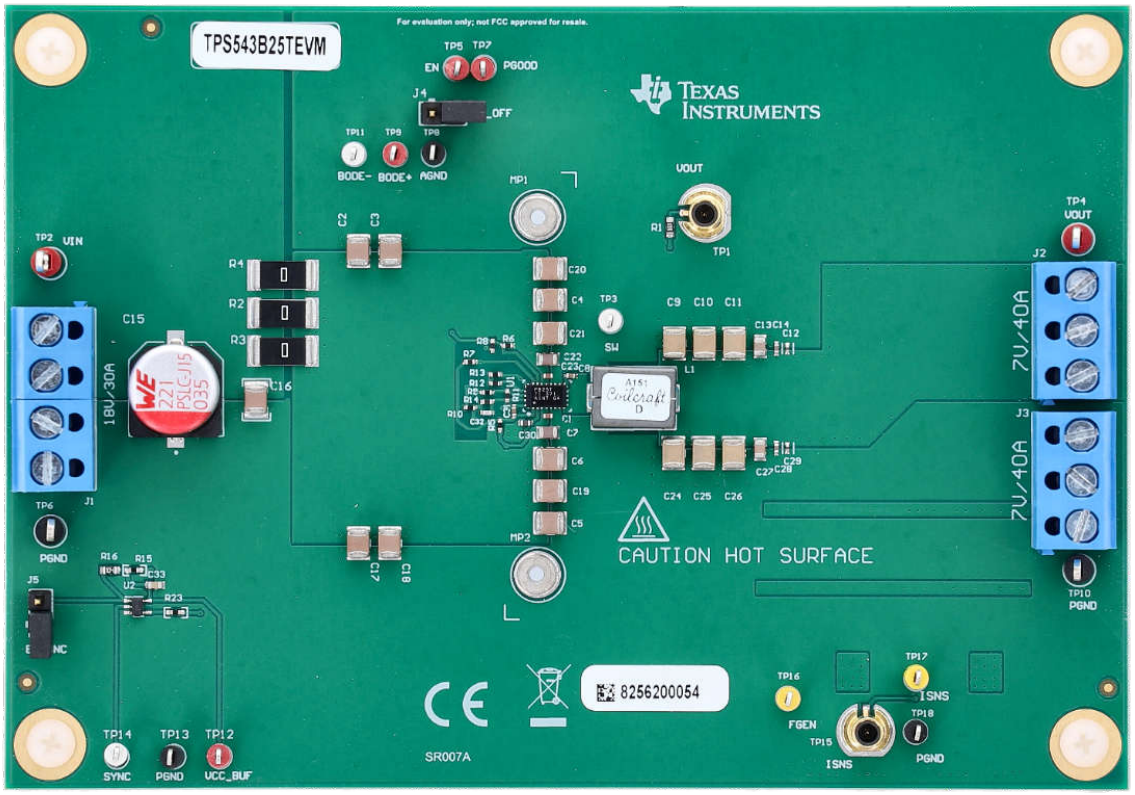
The TPS543B25T DC/DC converter is a synchronous buck converter designed to provide up to a 25-A output. The input (VIN) is rated for 4 V to 18 V.

Features

- Evaluate TPS543B25T device with two M2x0.4 threaded spacers.
- Screw terminals for supply and load
- Load transient circuit
- SMB connector to measure output voltage
- Jumper and shunt to enable device

Applications

- Wireless and wired communications infrastructure equipment
- Optical and fiber networks
- Test and measurement
- Medical healthcare



TPS543B25TEVM (Top View)

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1 Evaluation Module Overview

1.1 Introduction

This evaluation module includes a design with the TPS543B25T with thermally enhanced package with two M2x0.4 threaded steel spacers. The steel spacers are threaded and can be used to fasten a heat sink (heat sink not provided in kit). The output voltage is 1.0 V and switching frequency is 1 MHz.

This user's guide contains information for the TPS543B25T evaluation module (BSR007) and the 25 A DC/DC converter. Also included are the schematic, and bill of materials for the TPS543B25TEVM.

1.2 Kit Contents

The kit includes one TPS543B25TEVM.

1.3 Specification

Table 1-1 provides the rated input voltage and output current range for the evaluation module.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS543B25T	V_{IN} = 4 V to 18 V	0 A to 25 A

1.4 Device Information

The high-side and low-side MOSFETs are incorporated inside the TPS543B25T thermally enhanced package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS543B25T to achieve high efficiencies and helps keep the junction temperature low at the rated output current. Fixed frequency advanced current mode control allows you to synchronize the regulators to an external clock source. An external divider allows for an adjustable output voltage. The TPS543B25T FSEL and MODE pins provide selectable switching frequency, soft-start time, current limit, and internal compensation. Lastly, the TPS543B25T includes an enable pin and a power-good output, which can be used for sequencing multiple regulators.

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2 Hardware

2.1 Configurations and Modifications

These evaluation modules are designed to provide access to the features of the TPS543B25T. The U1 design provides jumpers for testing different configurations. Jumper selections must be made prior to enabling the TPS543B25T.

If a desired configuration is not available, then some modifications can be made to this module. When modifications are made to the components on the EVM, the internal compensation option selected with the MODE pin resistor needs to be changed. Changes to the f_{SW}, output voltage, output inductor, and output capacitors require a change in the compensation. TPS543B25T data sheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, f_{SW}, and inductance. Verify all components have sufficient voltage and current ratings.

2.1.1 Output Voltage

In the U1 design, the output voltage is set by the resistor divider network of R14 (R_{FBT}) and R11 (R_{FBB}). R11 is fixed at 4.99 kΩ to set the FB divider current at approximately 100 µA. To change the output voltage of the EVM, the value of resistor R14 must change. Changing the value of R14 can change the output voltage above the 0.5-V reference voltage (V_{REF}). The value of R14 for a specific output voltage can be calculated using Equation 1. After changing R14, the feedfoward capacitor (C32) can also need to be changed.

$$R_{FBT} = R_{FBB} \times \left[\frac{V_{OUT}}{V_{REF}} - 1\right] \quad (1)$$

2.1.2 Switching Frequency (FSEL Pin)

In the U1 design, change the FSEL resistor(R13) to the value which sets the desired option.

2.1.3 Current Limit, Soft-Start Time, and Internal Compensation (MODE Pin)

In the U1 design, change the MODE(R12) resistor to the value which sets the desired option.

2.1.4 Adjustable UVLO

The undervoltage lockout (UVLO) for U1 can be adjusted externally using R6(R_{ENT}) and R8 (R_{ENB}). See the TPS543B25T 4-V to 18-V Input, 25-A, Synchronous, SWIFT™ Step-Down Converter With Internally Compensated, Advanced Current Mode Control in Thermally Enhanced Packagefor detailed instructions for setting the external UVLO.

2.2 Input/Output Connections

This section describes how to properly connect, set up, and use the TPS543B25T evaluation module.

The TPS543B25T is provided with input connectors, output connectors, and test points as shown in Table 2-1 and Table 2-2.

To support the minimum input voltage with the full rated load on both outputs with the default EVM, a power supply capable of supplying greater than 30 A must be connected to J1 through a pair of 18-AWG wires or better.

For U1, the load must be connected to J2 and J3. Two pair of 18-AWG wires or better must be used for each connection. With the maximum current limit setting, the maximum load current capability is near 25 A before the TPS543B25T goes into current limit. Wire lengths must be minimized to reduce losses in the wires.

Test point TP2 provides a place to monitor the V_{IN} input voltage with TP6 providing a convenient ground reference for U1. TP4 is used to monitor the output voltage of U1 with TP10 as the ground reference.

If modifications are made to the TPS543B25T, then the input current can change. The input power supply and wires connecting the EVM to the power supply must be rated for the input current.

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Note

For the FSEL pin of the TPS543B25T to correctly detect the resistor value connected to ground, the buffers on the EVM need to be provided a VCC voltage of 2 V to 5.5 V to go high impedance.

Table 2-1. Connectors and Jumpers

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
J1	VIN	U1	VIN screw terminal to connect input voltage (see Table 2-2 for V_{IN} range).
J2	VOUT	U1	PGND ground
J3	GND	U1	VOUT screw terminal to connect load to output.
J4	EN_OFF	U1	2-pin header for enable. Add shunt to connect EN to ground and disable device.
J5	ENSYNC	U1	2-pin header to connect U2 buffer output enable to ground. Populate shunt to enable output of buffer. Remove shunt to make buffer output high impedance.

Table 2-2. Test Points

REFERENCE DESIGNATOR	NAME	RELATED IC	FUNCTION
TP1	VOUT	U1	SMB connector to measure output voltage. When using this test point, the scope must be set for 1-MΩ termination. When using 50-Ω termination, a 2:1 divider is created.
TP2	VIN	U1	VIN test point. Use this for efficiency measurements.
TP3	SW	U1	SW node solder mask opening.
TP4	VOUT	U1	VOUT test point. Use this for efficiency, output regulation, and bode plot measurements.
TP5	EN	U1	EN test point. If user is applying an external voltage, then the external voltage must be kept below the absolute maximum voltage of the EN pin of 6 V.
TP6	PGND	U1	PGND test point. Use this for efficiency measurements.
TP7	PGOOD	U1	PGOOD test point.
TP8	AGND	U1	AGND test point.
TP9	BODE+	U1	Used for Bode plot measurements.
TP10	PGND	U1	PGND test point. Use this for efficiency measurements.
TP11	BODE-	U1	Test point between voltage divider network and output voltage. Used for Bode plot measurements.
TP12	VCC_BUF	U1	VDRV Voltage Supply to Buffer.
TP13	PGND	U1	PGND test point.
TP14	SYNC	U1	SYNC test point.
TP15	ISNS	U1	Test point to measure current in load transient circuit. Gain is 20 A/V.
TP16	FGEN	U1	Test point to connect function generator to load transient circuit. Slowly increase amplitude and vary slew rate of function generator for desired load step.
TP17	ISNS	U1	Test point to measure current in load transient circuit. Gain is 20 A/V.
TP18	PGND	U1	PGND test point.

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2.3 Best Practices

The following warnings and cautions are noted for the safety of anyone using or working close to the TPS543B25T. Observe all safety precautions.

CAUTION

The TPS543B25T can become hot during operation due to dissipation of power in some operating conditions. Avoid contact with the board. Follow all applicable safety procedures applicable to your laboratory.

Caution: Hot surface.

Contact can cause burns.

Do not touch!

WARNING

The circuit module has signal traces, components, and component leads on the bottom of the board. This can result in exposed voltages, hot surfaces or sharp edges. Do not reach under the board during operation.

CAUTION

Some power supplies can be damaged by application of external voltages. If using more than 1 power supply, then check equipment requirements and use blocking diodes or other isolation techniques, as needed, to prevent damage to equipment.

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3 Implementation Results

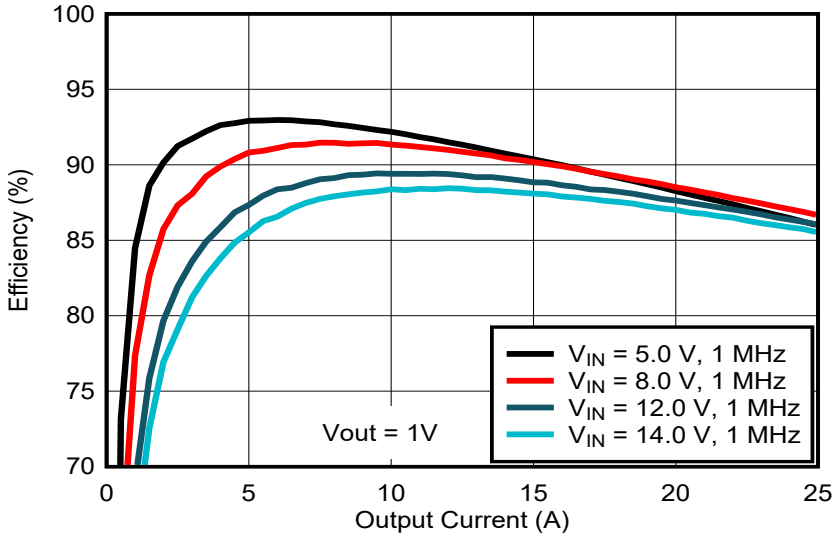

Figure 3-1. Efficiency Curves

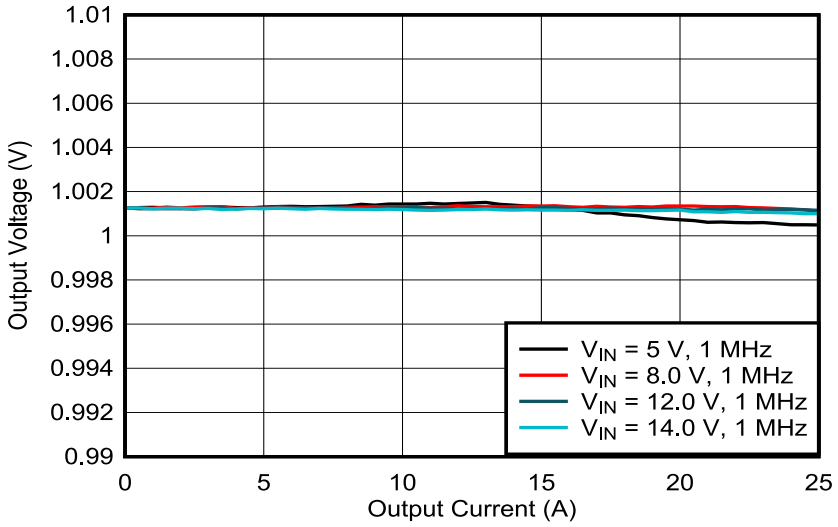

Figure 3-2. Load Regulation

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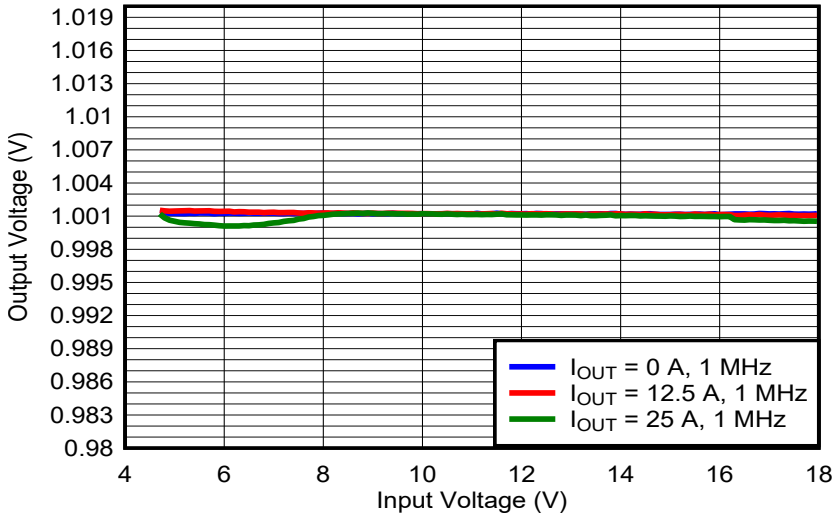

Figure 3-3. Line Regulation

3.1 Performance Characteristics Summary

A summary of the TPS543B25T performance characteristics is provided in Table 3-1. The TPS543B25T is designed and tested for V_{IN} = 4 V to 18 V. Characteristics are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.2 V, unless otherwise specified. The ambient temperature is room temperature (25°C) for all measurements, unless otherwise noted.

Table 3-1. TPS543B25T (U1) Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range		11.7	12	12.3	V
Output voltage setpoint			1.0		V
Output current range	V_{IN} = 11.7 V to 12.3 V	0		25	A
Output rise time	Set by MODE pin resistor		2		ms
Current limit	Set by MODE pin resistor		High		
Switching frequency (f_{SW})	Set by FSEL pin resistor		1000		kHz

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4 Hardware Design Files

4.1 Schematic

Figure 4-1 is the schematic for U1.

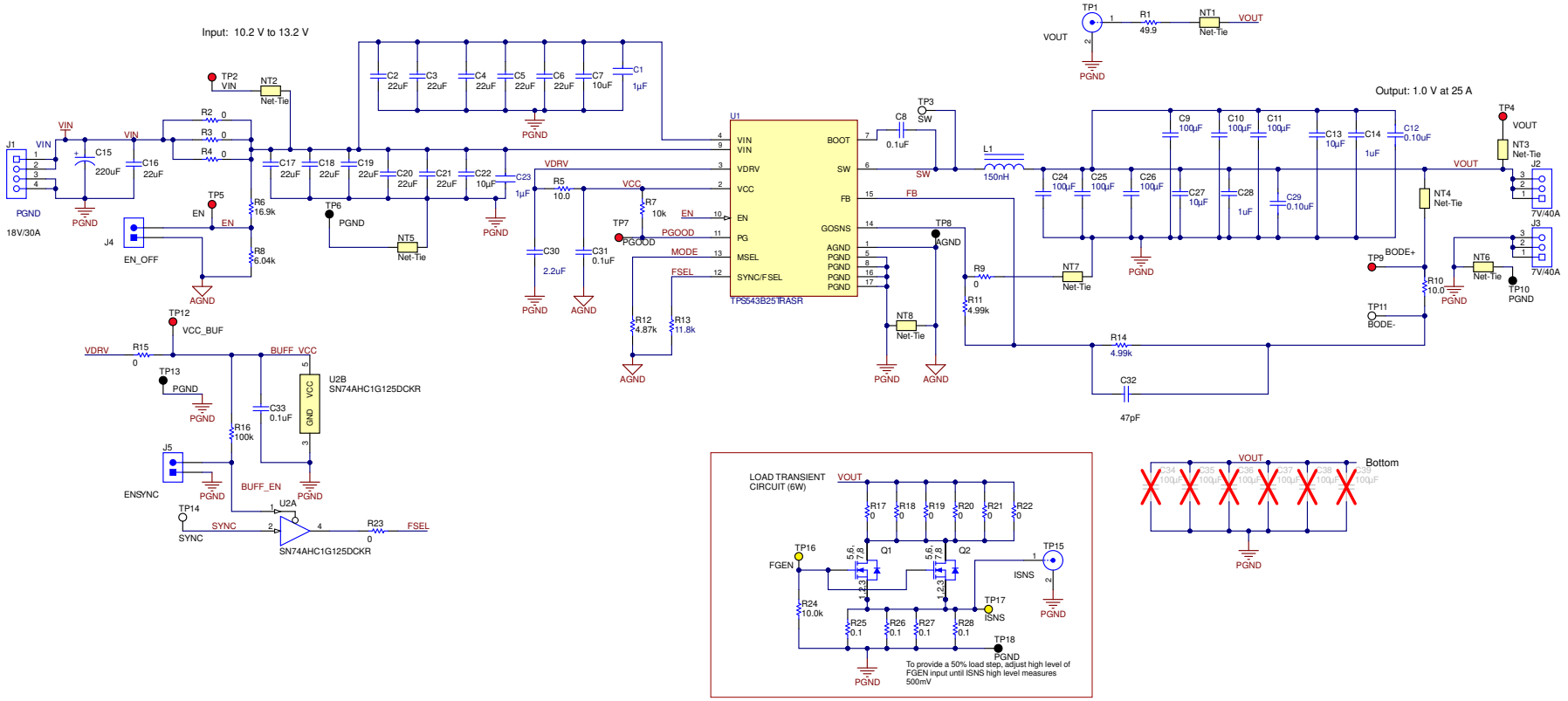

Figure 4-1. U1 schematic

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4.2 PCB Layout

This section provides a description of the TPS543B25T board layout and layer illustrations.

4.2.1 Layout

The board layout for the TPS543B25T is shown in Figure 4-2 through Figure 4-7. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

All of the required components for the TPS543B25T are placed on the top layer for U1. The input decoupling capacitors, VDRV capacitor, VCC capacitor, and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. An additional input bulk capacitor is used near the input terminal to limit the noise entering the converter from the supply used to power the board. Critical analog circuits such as the voltage set point divider, EN resistor, MODE resistor, and FSEL resistor are kept close to the IC and terminated to the quiet analog ground (AGND) island on the top layer.

The top layer contains the main power traces for VIN, VOUT, and SW. The top layer power traces are connected to the planes on other layers of the board with multiple vias placed around the board. There are multiple vias near the PGND pins of the IC to help maximize the thermal performance. Each TPS543B25T circuit has their own dedicated ground are for quiet analog ground that is connected to the main power ground plane at a single point. This single point connection is done on the internal ground planes. Lastly the voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} area on the top layer.

The signal layer 1 is a large ground plane and an analog ground island for the MSEL and FSEL resistor and VCC capacitor to connect to by vias. minimize cuts in the ground plane.

The signal layer 2 has VIN copper area beneath each IC to connect the VIN pins together with a low impedance connection. Lastly, the remaining area of this layer is filled in with PGND and additional copper plane for the 2nd stage filter. The mid layer 3 and mid layer 4 is mostly a power ground plane with minimal trace and cuts.

The bottom layer is primarily used for another ground plane. Lastly, the load transient circuit is placed on this side of the EVM.

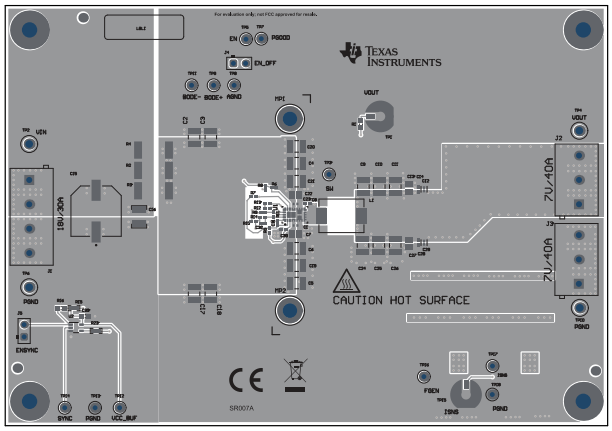

Figure 4-2. Top Composite View

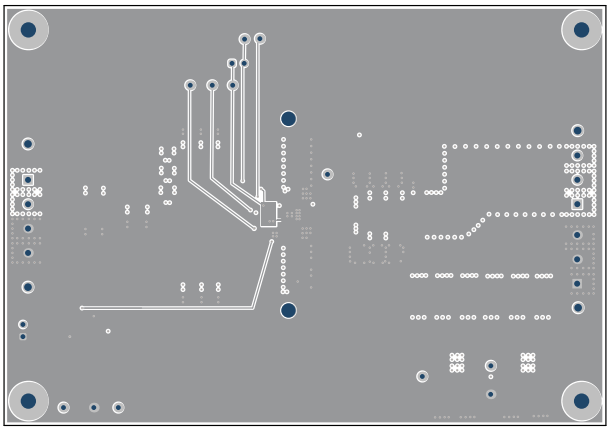

Figure 4-3. Signal 1

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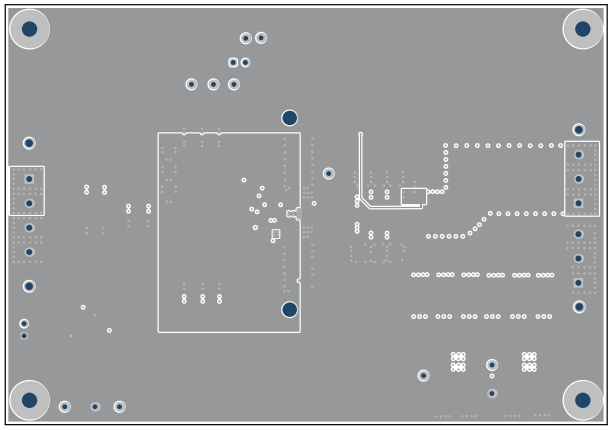

Figure 4-4. Signal 2

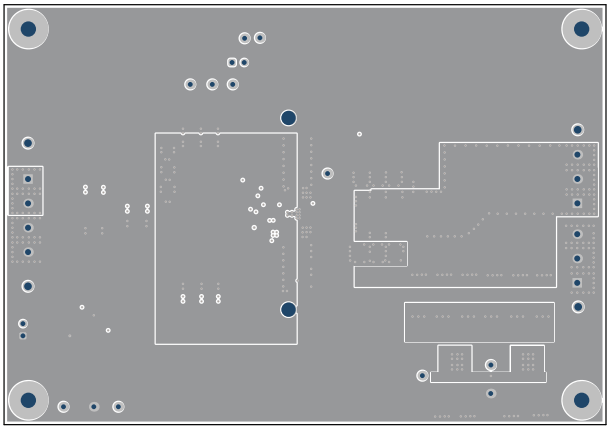

Figure 4-5. Signal 3

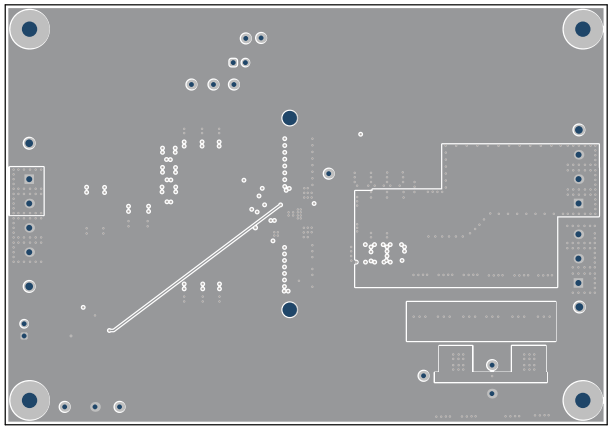

Figure 4-6. Signal 4

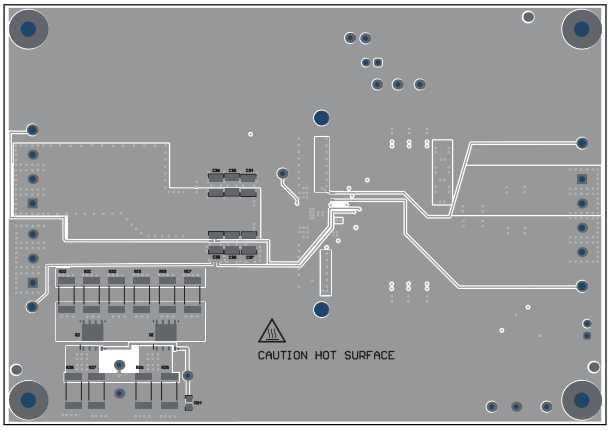

Figure 4-7. Bottom Composite View

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4.3 Bill of Materials

Table 4-1 presents the bill of materials for the TPS543B25T.

Table 4-1. TPS543B25TEVM Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		SR007	Any
C1, C23	2		CAP CER 1UF 25 V X6S 0402	0402	GRM155C81E105KE11D	Murata
C2, C3, C4, C5, C6, C16, C17, C18, C19, C20, C21	11	22uF	CAP, CERM, 22 uF, 25 V, +/- 10%, X7R, 1210	1210	GRM32ER71E226KE15L	Murata
C7, C22	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 10%, X7S, 0805	0805	GRM21BC71E106KE11L	Murata
C8, C31	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	0402	C1005X7R1H104K050BB	TDK
C9, C10, C11, C24, C25, C26	6	100uF	CAP, CERM, 100 µF, 6.3 V,+/- 20%, X7S, 1210	1210	GRM32EC70J107ME15L	Murata
C12, C29	2	100 nF	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 0.10uF, X7S, 22%, 10%, 6.3V	0201	GRM033C70J104KE14D	Murata
C13, C27	2	10uF	CAP, CERM, 10 uF, 6.3 V, +/- 10%, X7R, 0805	0805	GRM21BR70J106KE76L	Murata
C14, C28	2	1uF	CAP, CERM, 1 uF, 6.3 V,+/- 10%, X7R, 0402	0402	GRM155R70J105KA12D	Murata
C15	1	220 µF	220 µF 35 V Aluminum - Polymer Capacitors Radial, Can - SMD 22mOhm 2000 Hrs @ 105°C	SMT_ECAP_10MM3_10MM3	875075661008	Wurth Electronics
C30	1	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7S, 0402	0402	C1005X7S1A225K050BC	TDK
C32	1	47 pF	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G/NP0, 0402	0402	GRM1555C1H470FA01D	Murata
C33	1	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply

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Table 4-1. TPS543B25TEVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Terminal Block, 5.08 mm, 4x1, Brass, TH	4x1 5.08 mm Terminal Block	ED120/4DS	On-Shore Technology
J2, J3	2		Terminal Block, 5.08 mm, 3x1, Brass, TH	3x1 5.08 mm Terminal Block	ED120/3DS	On-Shore Technology
J4, J5	2		Header, 2.54mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	TSW-102-08-G-S	Samtec
L1	1	150nH	Inductor, Shielded, Ferrite, 150 nH, 51 A, 0.00039 ohm, SMD	10.2x7mm	SLR1050A-151KEC	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1, MP2	2			ROUND_SPACER	9774010243R	Wurth Electronics
Q1, Q2	2	30 V	MOSFET, N-CH, 30 V, 25 A, DQJ0008A (VSONP-8)	DQJ0008A	CSD17579Q5A	Texas Instruments
R1	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo
R2, R3, R4	3	0	RES, 0, 0%, 1 W, AEC-Q200 Grade 0, Body 6.3x3.2mm	Body 6.3x3.2mm	RMCF2512ZT0R00	Stackpole Electronics Inc
R5, R10	2	10	RES, 10.0, 1%, 0.063 W, 0402	0402	CRCW040210R0FKED	Vishay-Dale
R6	1	16.9k	RES, 16.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040216K9FKED	Vishay-Dale
R7	1	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GEJ103X	Panasonic
R8	1	6.04k	RES, 6.04 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K04FKED	Vishay-Dale
R9	1	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
R11, R14	2	4.99k	RES, 4.99 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF4991X	Panasonic
R12	1	4.87k	RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K87FKED	Vishay-Dale
R13	1	11.8k	RES, 11.8 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040211K8FKED	Vishay-Dale
R15, R23	2	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale

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Table 4-1. TPS543B25TEVM Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R16	1	100k	RES, 100 k, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEAC	Vishay-Dale
R17, R18, R19, R20, R21, R22	6	0	RES, 0, 5%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW25120000Z0EG	Vishay-Dale
R24	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic
R25, R26, R27, R28	4	0.1	RES, 0.1, 1%, 3 W, 2512	2512	CRA2512-FZ-R100ELF	Bourns
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP15	2		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
TP2, TP4	2		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
TP3, TP11, TP14	3		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP5, TP7, TP9, TP12	4		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP6, TP10	2		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP8, TP13, TP18	3		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP16, TP17	2		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1	1		4-V to 18-V Input, 25-A, Synchronous, SWIFT™ Step-Down Converter With Internally Compensated, Advanced Current Mode Control in Thermally Enhanced Package	WQFN-FCRLF17	TPS543B25TRASR	Texas Instruments
U2	1		Single Bus Buffer Gate with 3-State Output, DCK0005A, LARGE T&R	DCK0005A	SN74AHC1G125DCKR	Texas Instruments
C34, C35, C36, C37, C38, C39	0	100uF	CAP, CERM, 100 µF, 6.3 V,+/- 20%, X7S, 1210	1210	GRM32EC70J107ME15L	Murata

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