TEXAS INSTRUMENTS

High-Performance Synchronous Buck EVM

Using the TPS56100 in Systems With Only 5 V Available

User's Guide

July 1999

Mixed Signal Products

SLVU018

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Preface

Read This First

About This Manual

This user's guide describes the TPS56100EVM 128 synchronous buck converter evaluation module (SLVP128). The SLVP128 provides a convenient method for evaluating the performance of a synchronous buck converter using the TPS56100 ripple regulator controller. A complete designed and tested power supply is presented. The power supply is a programmable step-down dc-dc EVM that can deliver up to 6 A of continuous output current at a programmable output voltage from 1.3 V approximately 4.4 V determined by a 5 bit DAC code and the use of three external components with an input voltage of 5 V.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 *Introduction* provides introductory and background information.
- Chapter 2 *Test Results* shows the test setups used, and the test results obtained, in designing the SLVP128 EVM.
- Chapter 3 *Schematic* contains the schematic diagram for the SLVP128 EVM.
- Chapter 4 *Physical Layouts* contains the board layout, and assembly drawings for the SLVP128 EVM.
- Chapter 5 *Bill of Materials* contains the bill of materials required for the SLVP128 EVM.

Related Documentation From Texas Instruments

- *Designing Fast Response Synchronous Buck Converters Using the TPS5210* Application Report, Literature Number SLVA044.
- *TPS5210 Programmable Synchronous-buck Regulator Controller* Data Sheet, Literature Number SLVS171.
- *VRM 8.3 DC-DC Converter Design Guidelines,* Intel document order number: 243870-001, June 1998.
- *High-Density Synchronous Buck Converter Design Using TPS56xx Controllers* User's Guide, Literature Number SLVU013

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This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

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Chapter 1

Introduction

Topic Page

1.1 Background

New high performance microprocessors may require from 40 to 80 watts of power for the CPU alone. Load current must be supplied with up to 30 A/μs slew rate while keeping the output voltage within tight regulation and response time tolerances [3]. Parasitic interconnect impedances between the power supply and the processor must be kept to a minimum. Fast responding synchronous buck dc/dc converters controlled by the Texas Instruments TPS56100 hysteretic controller are ideally suited for microprocessor power applications requiring fast response and precise regulation of rapidly changing loads.

Conventional synchronous regulator control techniques include fixed frequency voltage-mode, fixed frequency current-mode, variable frequency current-mode, variable on-time, or variable off-time. CPU power supplies that are designed using these types of control methods require additional bulk storage capacitors on the output to maintain V_O within the regulation limits during the high di/dt load transients because of the limited bandwidth of the controller. Some controllers add a fast loop around the slower main control loop to improve the response time, but V_O must deviate outside a fixed tolerance band before the fast loop becomes active. The hysteretic control method employed by the TPS56100 offers superior performance with no requirements for additional output capacitance or difficult loop compensation design.

The TPS56100 controller was optimized for tight Vout regulation under static and dynamic load conditions, for improved system efficiency, and can operate in systems that derive main power from 5 V.

1.2 Performance Specification Summary

This section summarizes the performance specifications of the SLVP128 converter. Table 1–1 gives the performance specifications of the converters.

Table 1–1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range		4.5	5	5.5	V
Output voltage range	See Note 1	1.3	2.0	4.4	V
Static voltage tolerance	See Note 2	1.98	2.0	2.02	V
Line regulation	See Notes 1, 3		± 0.05%	± 0.1%	
Load regulation	See Notes 4, 5		± 0.1%	± 0.4%	
Transient response	See Note 6		± 55 50		mV pk µs
Output current range	See Note 3	0		6	A
Current limit	See Note 3	8			A
Output ripple	See Note 3		35		mV
Soft-start rise time	See Note 4		10		ms
Operating frequency	See Notes 1,4		235		kHz
Efficiency, 6 A load	See Notes 2, 4		84%		
Efficiency, 3 A load	See Notes 2, 4		83%		

Notes:
1) I_O = 6 A.
2) VID inputs set for V_{REF} = 2 V.
3) Input voltage can be at any point over entire range.
4) Input voltage adjusted to 5 VDC.
5) I_O varied can be at any point over entire range.
6) I_O pulsed from 0 A to 6 A, di/dt = 30 A/µs.

1.3 Voltage Programming Code

A voltage programming network (VP) consisting of a 5–bit DAC programs the regulated voltage within a range from 1.3 V to 2.6 V. The output voltage for a given VP Code is shown in Table 1–2.

Table 1–2. Voltage Programming Code

VP Terminals (0 = GND, 1 = floating or pull-up to 5 V)					VREF
VP4	VP3	VP2	VP1	VP0	(Vdc)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No CPU
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.60
1	0	1	1	1	2.60
1	0	1	1	0	2.60
1	0	1	0	1	2.60
1	0	1	0	0	2.60
1	0	0	1	1	2.60

Table 1–2. Voltage Programming Code (Continued)

VP Terminals (0 = GND, 1 = floating or pull-up to 5 V)					VREF
VP4	**VP3**	**VP2**	**VP1**	**VP0**	**(Vdc)**
1	0	0	1	0	2.60
1	0	0	0	1	2.60
1	0	0	0	0	2.60

Note: If the VP bits are set to 11111, then the high-side and low-side driver outputs will be set low.

Chapter 2

Test Results

This chapter shows the test setups used, and the test results obtained, in designing the SLVP128 EVM.

Topic **Page**

2.1 Test Summary

The detailed test results and waveforms are presented in Figure 2–2 to Figure 2–7 for the SLVP128. The following are summarized results.

2.1.1 Static Line and Load Regulation

The precise reference voltage regulator implemented in the TPS56100 controller using both positive and negative remote sense pins provides excellent regulation characteristics. The load regulation from no load to 6 amps load current does not exceed 0.32%. The line regulation is less than 0.31% for the input voltage range from 4.5 V to 5.5 V. Line and load regulation is shown in Figure 2–2. The set point tolerance is approximately 1.0%.

2.1.2 Output Voltage Ripple

The output voltage peak-to-peak ripple is less than ±1%. This is a typical value but it can be optimized for lower ripple applications. Measured output ripple waveform is shown in Figure 2–6. The output filter for this EVM design is optimized for fast transient response due to the high slew-rate load current transitions. Therefore, the output filter is not optimized for low ripple and has a moderate amount of output ripple.

2.1.3 Efficiency and Power Losses

Efficiency and power losses for 5 V input voltage and maximum output current of 6 A are presented in the following table:

Table 2–1. Evaluation Board Efficiency and Power Losses

Evaluation Board	Efficiency, %	Power Losses, W
SLVP128 (1.8V)	84	2.02

An efficiency graph versus load at different line voltages is shown in Figure 2–3. Low power loss in each component decreases their temperature rise and improves long term reliability. The EVM does not require forced air cooling over a temperature range of 0°C to 70°C.

2.1.4 Output Start-Up and Overshoot

Output voltage rise time does not depend on the load current and ramps up in a linear fashion There is no discernable overshoot in the waveform. In this application, output voltage rise time is set to approximately 10 mS with an external capacitor (C7).

2.1.5 Frequency Variation

The switching frequency for a hysteretic controller depends on the input and output voltages and the output filter characteristics. It has approximately the same frequency variation as constant OFF time controllers. The precise

equation for switching frequency, confirmed by experiment, is presented in the TPS56100 datasheet. A more detailed analysis of the switching frequency variation for a hysteretic converter can be found in TI's application report *Designing Fast Response Synchronous Buck Converters Using the TPS5210*, Literature Number SLVA044 and in the paper presented at HFPC-98: A *Fast, Efficient Synchronous-Buck Controller for Microprocessor Power Supplies*. This paper can also be downloaded from the URL: http://www.ti.com/sc/docs/msp/papers/index.htm.

The frequency variation over all input voltage and output current combinations is presented in the following table.

Table 2–2. Evaluation Board Frequency Variation

Evaluation Board	Frequency Variation, kHz
SLVP128 (1.8V)	215–250

A graph of switching frequency versus load at different line voltages is shown in Figure 2–5.

2.1.6 Conclusion

The test results of the SLVP128 EVM demonstrate the advantages of the TPS56100 controller to meet stringent supply requirements to power supplies, especially for powering DSPs and microprocessors. The power system designer has a good solution to optimize the system for his particular application. Detailed information on how to design a dc-dc converter by using the TPS56100 hysteretic controller is presented the TPS56100 datasheet. Other sources of information on designing hysteretic controlled power supplies can be found in TI's User's Guide *High-Density Synchronous Buck Converter Desing Using TPS56xx Controllers*, Literature Number SLVU013 or the application report *Designing Fast Response Synchronous Buck Regulators Using the TPS5210*, Literature Number SLVA044.

2.2 Test Setup

Follow these steps for initial power up of the SLVP128:

1) Connect an electronic load from Vout to PwrGND (J9 and J10 to J11, J12, and J13) adjusted to draw approximately 1 A at 1.8 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic load. The output current drawn by the resistor is I_L = 1.8 V/R, where R is the value of the load resistor. The resistor power rating, P_R should be at least $2 \times 1.8^2/R$ Watts.

   Connect the sense lines from the load to VsenseH and VsenseL (J1 and J2).

2) Connect a 5-V lab power supply to the 5–V input (J4, J5 and J6 referenced to PwrGND, J7 and J8) of the SLVP128. Adjust the current limit to approximately 1 A.

3) Turn on the 5-V power supply and ramp the input voltage up to 5 V.

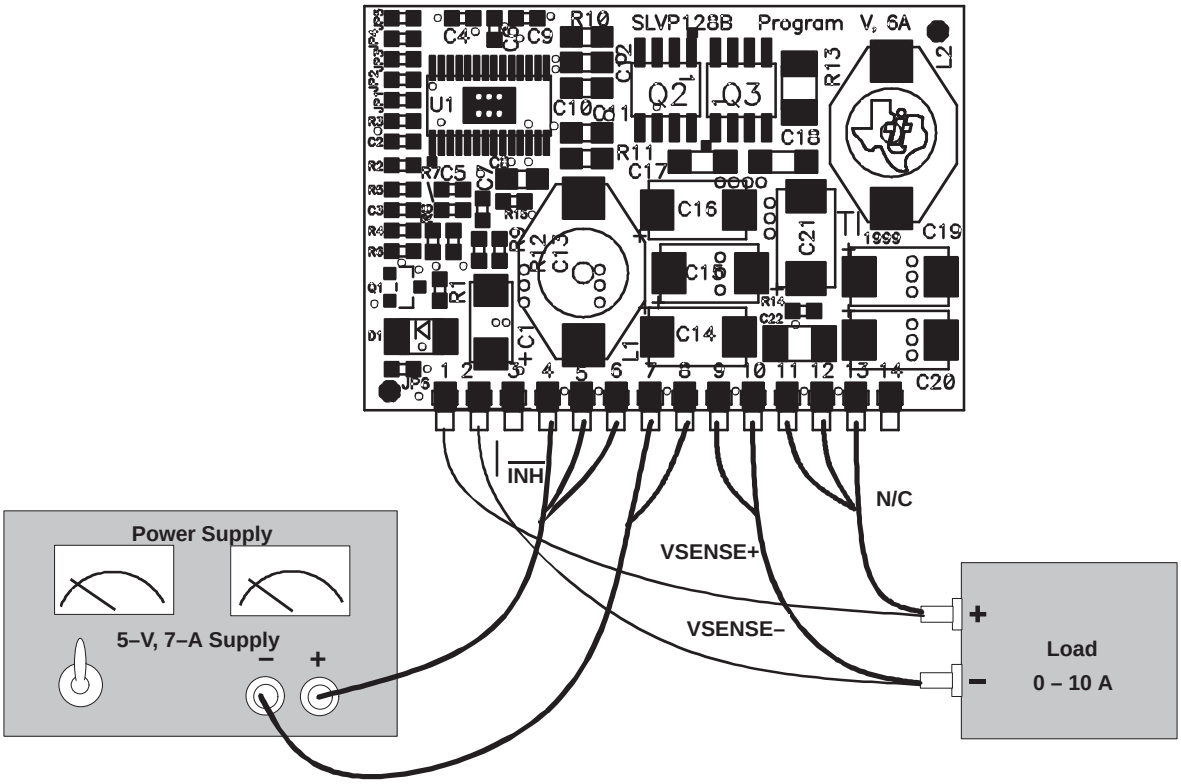
4) Verify that the SLVP128 output voltage (measured at the module output pins) is 1.8 V $\pm$ 0.020 V.

5) For subsequent testing, ensure the lab supply output current capacity and current limit are at least 5 A so that the SLVP128 can be operated at maximum load of 6 A.

6) Refer to the Test Results for selected typical waveforms and operating conditions for verification of proper module operation.

Figure 2–1 shows the SLVP128 test setup.

Figure 2–1. SLVP128 Test Setup



Note: All wire pairs should be twisted.

2.3 Test Results

Figures 2–2 to 2–7 show test results for the SLVP128.

Figure 2–2. SLVP128 Measured Load and Line Regulation

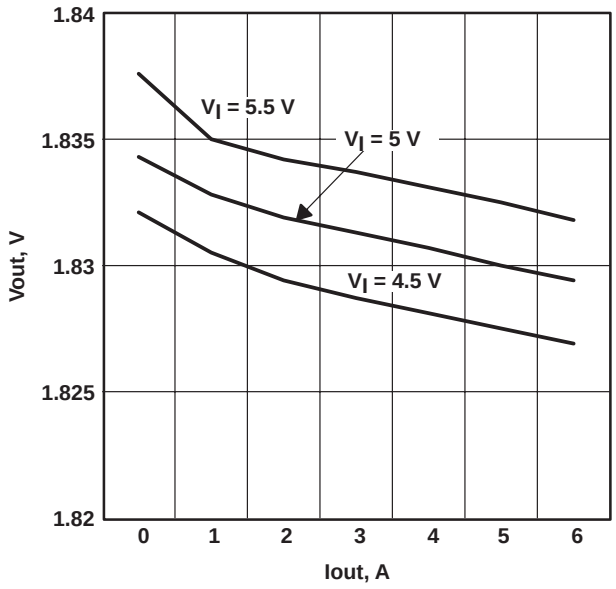


Figure 2–3. SLVP128 Measured Efficiency

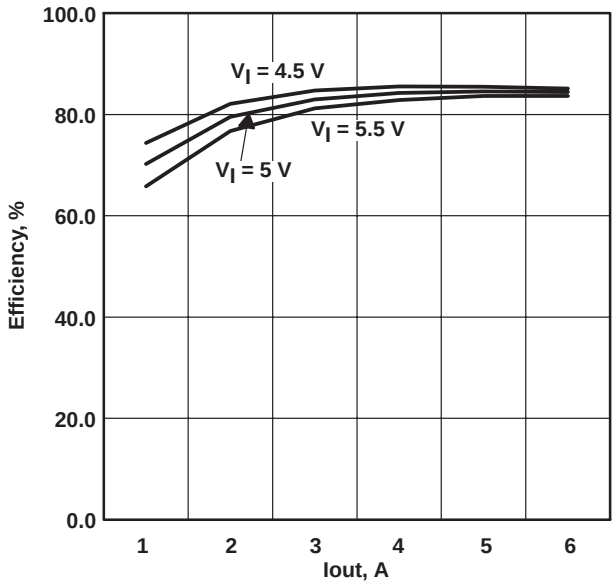


Figure 2–4. SLVP128 Measured Power Dissipation

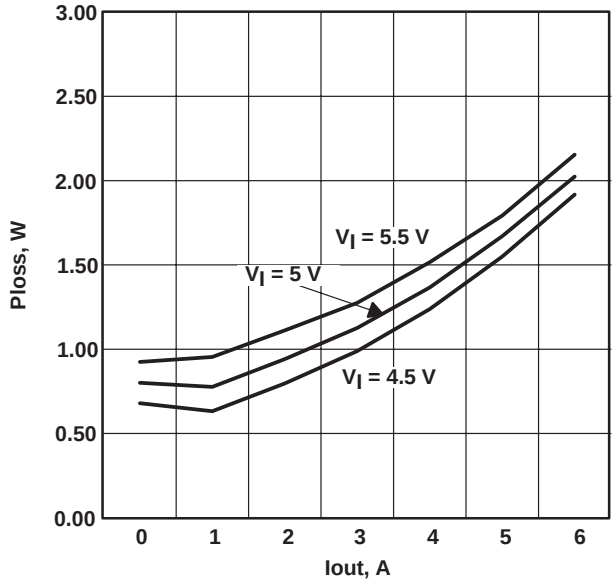


Figure 2–5. SLVP128 Measured Switching Frequency

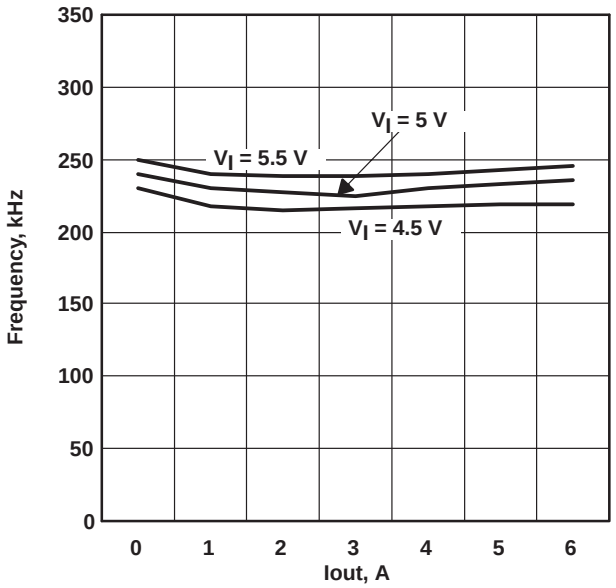


Figure 2–6. SLVP128 Measured Switching Waveforms

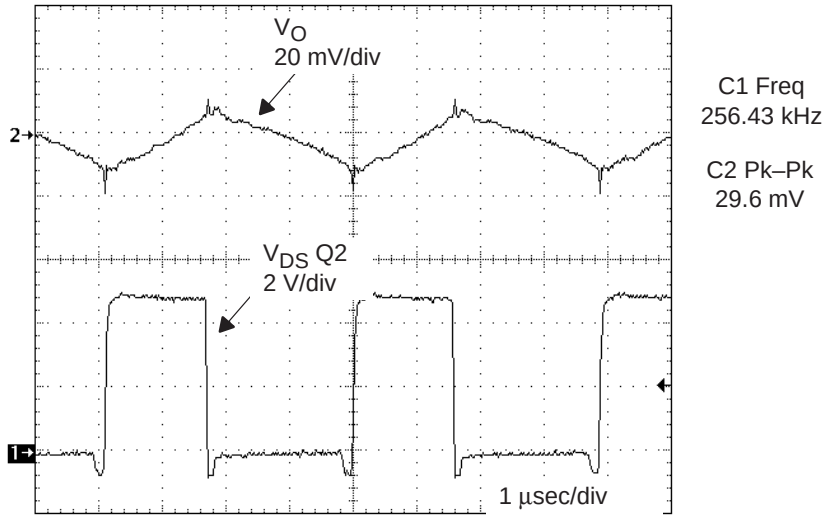
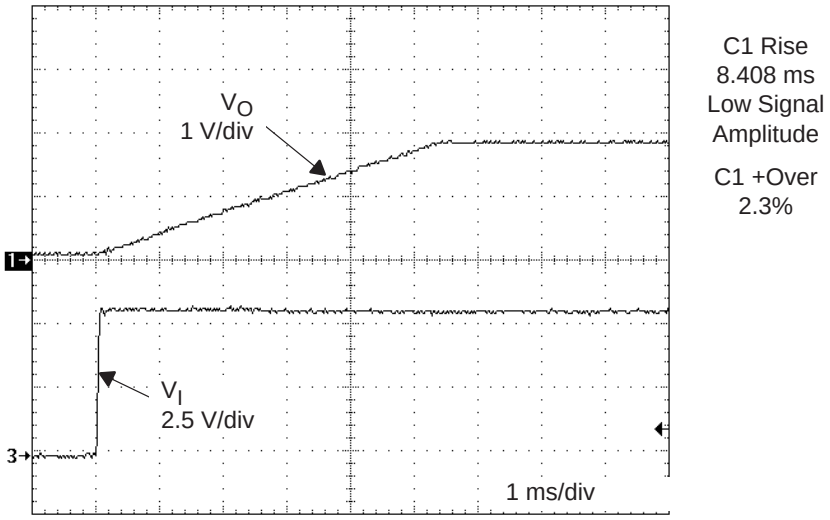


Figure 2–7. SLVP128 Measured Start-Up Waveforms



Chapter 3

Schematic

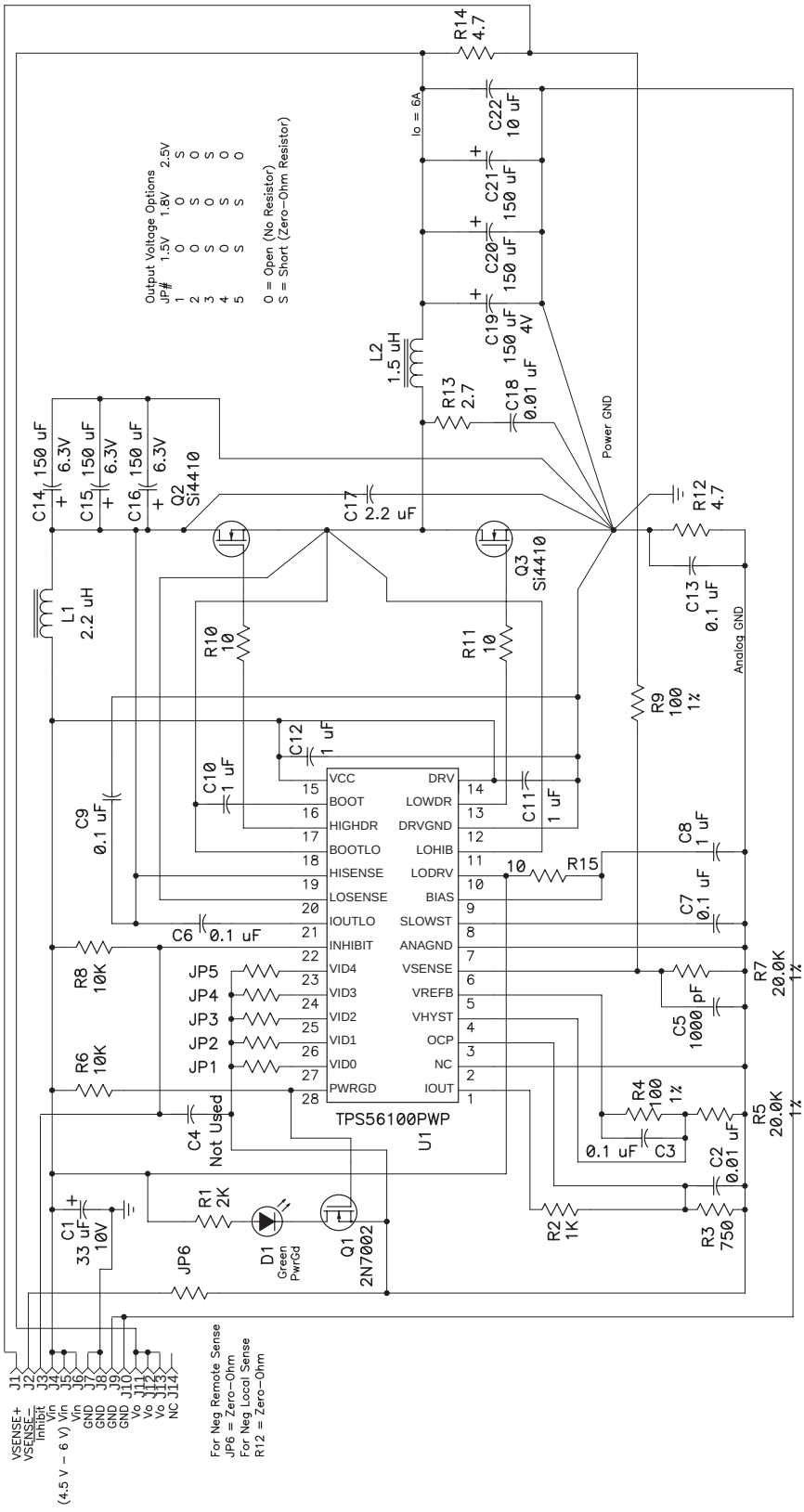
This chapter contains the schematic diagram for the SLVP128 EVM.

Topic **Page**

3.1 Schematic

Figure 3–1 shows the SLVP128 EVM schematic diagram.

Figure 3–1. SLVP128 Schematic Diagram



Chapter 4

Physical Layouts

This chapter contains the board layout, and assembly drawings for the SLVP128 EVM.

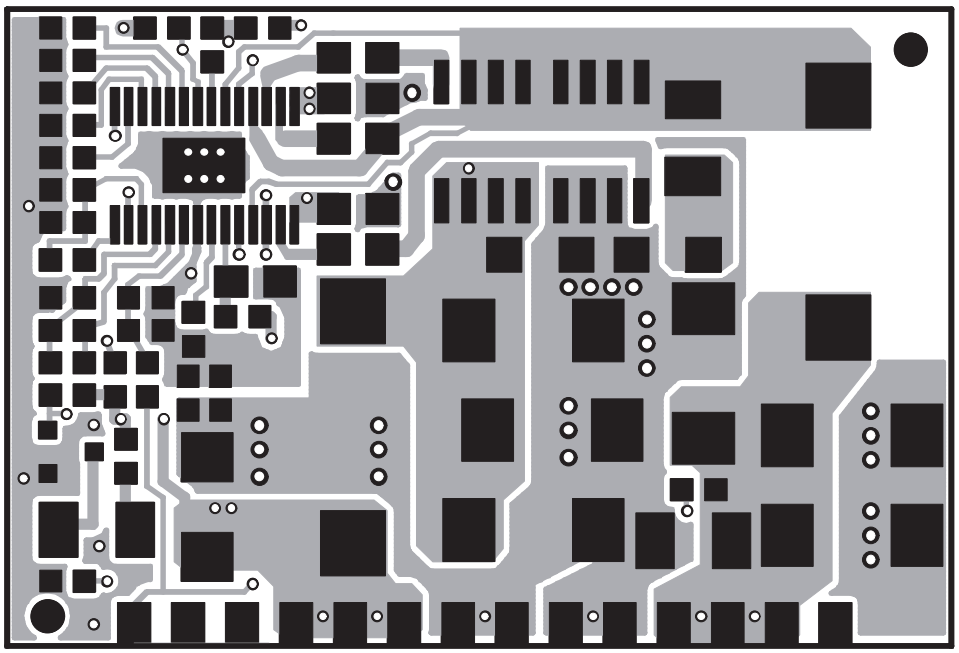
Topic **Page**

4.1 Board Layout

The power supply module consists of one PWB. Figure 4–1 shows the top layer (front view) of the SLVP128 PWB. Figure 4–2 shows the bottom layer (top view) of the SLVP128 PWB.

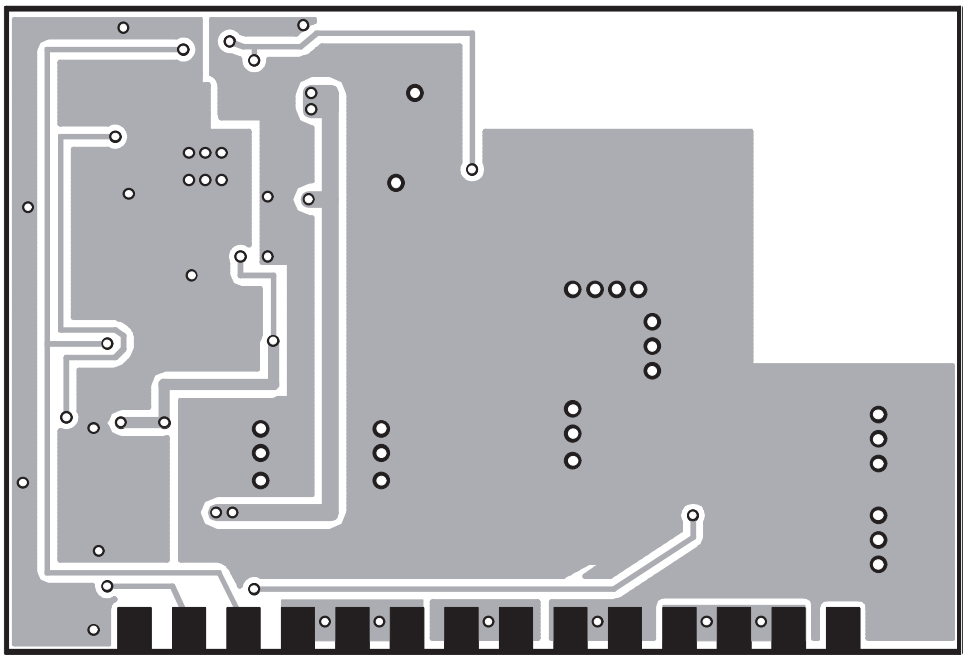
Figure 4–3 shows the SLVP128 top assembly view. Figure 4–4 shows a side view of the SLVP128 assembly. Figure 4–5 shows the pin setup detail for the SLVP128.

Figure 4–1. SLVP128 Board Layout Top Layer



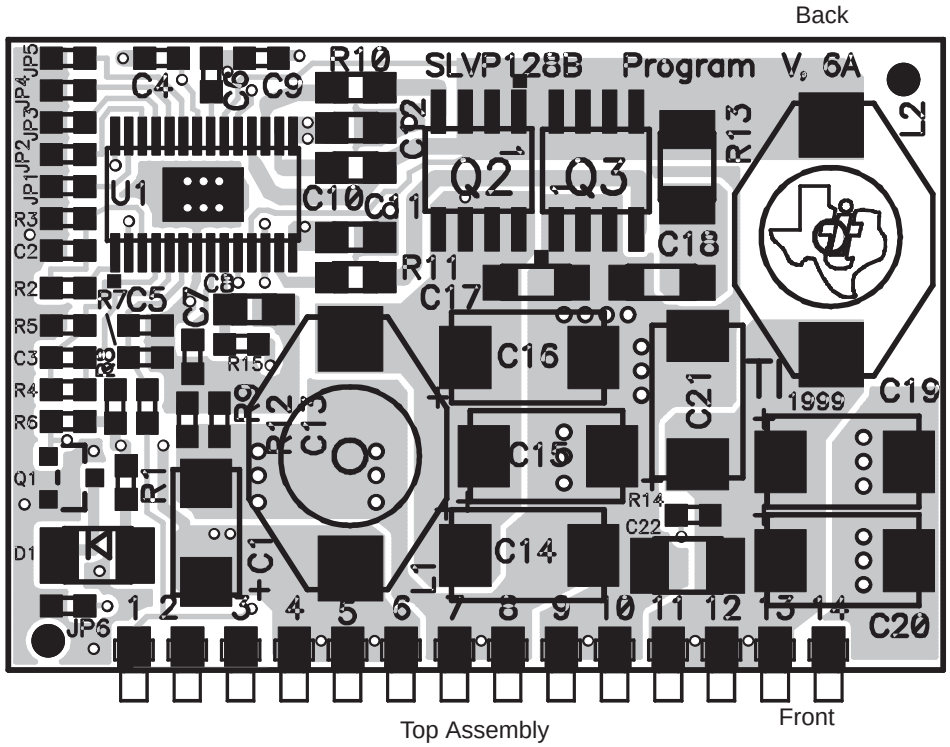
Top Layer

Figure 4–2. SLVP128 Board Layout Bottom Layer



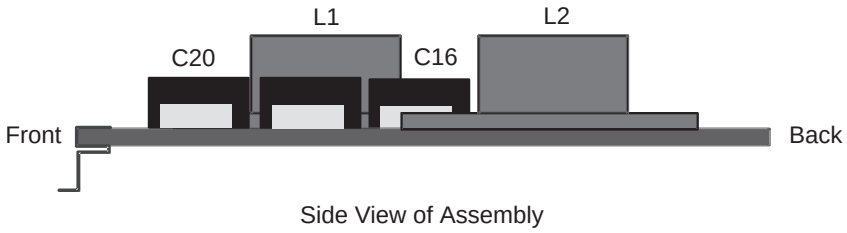
Bottom Layer (Top View)

Figure 4–3. SLVP128 Top Assembly View



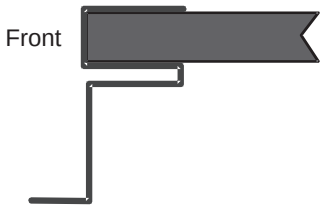
Top Assembly

Figure 4–4. SLVP128 Side View of Assembly



Side View of Assembly

Figure 4–5. SLVP128 Pin Setup Detail View



Detail of Pin Setup

Chapter 5

Bill of Materials

This chapter contains the bill of materials required for the SLVP128 EVM.

Topic **Page**

5.1 Bill of Materials

EVM. Table 5–1 lists materials required for the SLVP128 EVM.

Table 5–1. SLVP128 Bill of Materials

Ref Des	Qty	Part Number	Description	MFG	Size
C1	1	10TPA33M	Capacitor, POSCAP, 33 uF, 10 V, 20%	Sanyo	C
C2	1	GRM39X7R103K025A	Capacitor, Ceramic, 0.01uF, 25V, 10%, X7R	muRata	603
C3	5	GRM39X7R104K016A	Capacitor, Ceramic, 0.1 uF, 16V, 10%, X7R	muRata	603
C4			Not Used		603
C5	1	GRM39X7R102K050A	Capacitor, Ceramic, 1000 pF, 50V, 10%, X7R	muRata	603
C6		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 uF, 16V, 10%, X7R	muRata	603
C7		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 uF, 16V, 10%, X7R	muRata	603
C8	4	ECJ-2VF1C105Z	Capacitor, Ceramic, 1.0 uF, 16V, +80%-20%, Y5V	Panasonic	805
C9		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 uF, 16V, 10%, X7R	muRata	603
C10		ECJ-2VF1C105Z	Capacitor, Ceramic, 1.0 uF, 16V, +80%-20%, Y5V	muRata	805
C11		ECJ-2VF1C105Z	Capacitor, Ceramic, 1.0 uF, 16V, +80%-20%, Y5V	Panasonic	805
C12		ECJ-2VF1C105Z	Capacitor, Ceramic, 1.0 uF, 16V, +80%-20%, Y5V	Panasonic	805
C13		GRM39X7R104K016A	Capacitor, Ceramic, 0.1 uF, 16V, 10%, X7R	Panasonic	603
C14	3	6TPB150M	Capacitor, POSCAP, 150 uF, 6.3 V, 20%	Sanyo	D
C15		6TPB150M	Capacitor, POSCAP, 150 uF, 6.3 V, 20%	Sanyo	D
C16		6TPB150M	Capacitor, POSCAP, 150 uF, 6.3 V, 20%	Sanyo	D
C17	1	GRM42-6Y5V225Z016A	Capacitor, Ceramic, 2.2 uF, 16V, Y5V	muRata	1206
C18	1	GRM42-6X7R103K025A	Capacitor, Ceramic, 0.01uF, 25V, 10%, X7R	muRata	1206
C19	3	4TPC150M	Capacitor, POSCAP, 150 uF, 4 V, 20%	Sanyo	D2
C20		4TPC150M	Capacitor, POSCAP, 150 uF, 4 V, 20%	Sanyo	D2
C21		4TPC150M	Capacitor, POSCAP, 150 uF, 4 V, 20%	Sanyo	D2
C22	1	GRM235Y5V106Z016A	Capacitor, Ceramic, 10uF, 16V, Y5V	muRata	1210

Table 5–1. SLVP128 Bill of Materials (Continued)

Ref Des	Qty	Part Number	Description	MFG	Size
D1	1	SML-LX2832GC-TR	Diode. LED, Green, 2.1 V, SM	Lumex	1210
J1–J14	14	CA21BA-D36K-0FA	Clip, surface-mount, 0.040” board, 0.090” stand-off	NAS Interplex	0.1 Ctrs
JP1			Not used		603
JP2	4	Std	Resistor, chip, 0 Ω, 1/16W		603
JP3			Not used		603
JP4		Std	Resistor, chip, 0 Ω, 1/16W		603
JP5		Std	Resistor, chip, 0 Ω, 1/16W		603
JP6		Std	Resistor, chip, 0 Ω, 1/16W		603
L1	1	DO3316P-222HC	Inductor, 2.2 uH, 7.4 A	Coilcraft	DO3316P
L2	1	DO3316P-152HC	Inductor, 1.5 uH, 9.0 A	Coilcraft	DO3316P
Q1	1	2N7002DICT-ND	MOSFET, N-ch, 60 V, 115 mA, 1.2 Ω	Diodes, Inc.	TO-236
Q2	2	IRF7811	FET, N-ch, 30-V, 10-A, 11 mΩ	I.R.	SO-8
Q3		IRF7811	FET, N-ch, 30-V, 10-A, 11 mΩ	I.R.	SO-8
R1	1	Std	Resistor, chip, 2 kΩ, 1/16W, 5%		603
R2	1	Std	Resistor, chip, 1 kΩ, 1/16W, 1%		603
R3	1	Std	Resistor, chip, 750 Ω, 1/16W, 5%		603
R4	2	Std	Resistor, chip, 100 Ω, 1/16W, 1%		603
R5	2	Std	Resistor, chip, 20 kΩ, 1/16W, 1%		603
R6	2	Std	Resistor, chip, 10 kΩ, 1/16W, 5%		603
R7		Std	Resistor, chip, 20 kΩ, 1/16W, 1%		603
R8		Std	Resistor, chip, 10 kΩ, 1/16W, 5%		603
R9		Std	Resistor, chip, 100 Ω, 1/16W, 1%		603
R10	2	Std	Resistor, chip, 10 Ω, 1/10W, 5%		805
R11		Std	Resistor, chip, 10 Ω, 1/10W, 5%		805
R12	2	Std	Resistor, chip, 4.7 Ω, 1/16W, 5%		603
R13	1	Std	Resistor, chip, 2.7 Ω, 1/4W, 5%		1210
R14		Std	Resistor, chip, 4.7 Ω, 1/16W, 5%		603
R15	1	Std	Resistor, chip, 10 Ω, 1/16W, 5%		603
U1	1	TPS56100PWP	IC, PWM ripple controller, programmable	TI	PWP-28
	1	SLVP128, Rev. A	PCB, 2-Layer, 2-oz, 1.75”(L) × 1.18”(W) × 0.040”(T)		