This user’s guide describes the characteristics, operation, and use of the TPS62110EVM evaluation module (EVM). This EVM is designed to help the user easily evaluate and test the operation and functionality of the TPS62110. This User’s Guide includes setup instructions for the hardware, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

The Texas Instruments TPS62110 is a 1.5-A synchronous step-down converter in a 16-pin QFN package. Both fixed and adjustable output voltage units are available.

1.1 Background

The TPS62110EVM-101 uses the TPS62110 adjustable version and is set to 3.3 V output. The EVM operates with full rated performance with an input voltage between 3.6 V and 17 V.
1.2 Performance Specification

Table 1 provides a summary of the TPS62110EVM-101 performance specifications. All specifications are given for an ambient temperature of 25°C.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td></td>
<td>3.6</td>
<td></td>
<td>17</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>Iout = 10 mA to 1500 mA</td>
<td>3.267</td>
<td>3.3</td>
<td>3.333</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td></td>
<td>0</td>
<td></td>
<td>1500</td>
<td>mA</td>
</tr>
<tr>
<td>Low Battery Output (LBO)</td>
<td>VIN</td>
<td>5.8</td>
<td>6.0</td>
<td>6.2</td>
<td>V</td>
</tr>
<tr>
<td>Power Good (PG)</td>
<td>VOUT</td>
<td>3.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

1.3 Modifications

The PWB for this EVM is designed to accommodate both the fixed and adjustable versions of this IC. If the fixed version is installed, replace R1 with a 0-Ω resistor; R1 and C3 are open. If additional filtering is desired, C5 can be added.

1.3.1 Adjustable Output IC U1 Operation

U1 is configured for evaluation of the adjustable output version. This unit is configured for 3.3 V. Resistors R1 and R2 are used to set the output voltage between 1.2 V and 16 V. See the TPS62110 datasheet (SLVS585) for recommended values. The feedforward capacitor C3 may also need to be changed. For more information see the data sheet.

1.3.2 Fixed Output Operation

U1 can be replaced with the fixed version for evaluation. For fixed-version operation, replace R1 with a 0-Ω resistor; R2 and C3 positions remain unpopulated.

2 Setup

This section describes how to properly use the TPS62110EVM-101.

2.1 Input / Output Connector Descriptions

- **J1–VIN**: Positive input connection from the input supply for U1
- **J2–GND**: Return connection from the input supply for U1, common with J4.
- **J3–VOUT**: Output voltage connection
- **J4–GND**: Output return connection, common with J2
- **J5–LBO/PG**: Low battery output (LBO) pulled up to Vout; low indicates LBI is below its threshold. Power good (PG), low indicates output voltage is less than 98.4% of the normal value.
- **JP1–SYNC**: Input for synchronization to external clock signal. High forces low-noise PWM mode, PFM/PWM low enables power save PFM/PWM mode.
- **JP2–EN**: Enable pin, low on the EN turns unit off.
2.2 **Setup**

To operate the EVM, simply connect an input supply to the appropriate pins, and then connect a load to the appropriate pins. Maximum recommended load is 1.5 A or 2.2 Ω. Input supply of 6 V to 17 V is recommended.

3 **Board Layout**

This section provides the TPS62110EVM-101 board layout and illustrations.

3.1 **Layout**

Figure 1 shows the board layout for the TPS62110EVM-101 PWB.
Figure 2. Top Layer Routing
Figure 3. Bottom Layer Routing
4 Schematic and Bill of Materials

This section provides the TPS62110EVM-101 schematic and bill of materials.

4.1 Schematic

Figure 4. TPS62110EVM-101 Schematic
4.2 Bill of Materials

Table 2. TPS62110EVM-101 Bill of Materials

<table>
<thead>
<tr>
<th>COUNT</th>
<th>Ref Des</th>
<th>DESCRIPTION</th>
<th>SIZE</th>
<th>PART NUMBER</th>
<th>MFR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1</td>
<td>Capacitor, Ceramic, 10-µF, 25-V, X5R, 10%</td>
<td>1210</td>
<td>C3225X5R1E106K</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>C2</td>
<td>Capacitor, Ceramic, 1.0-µF, 16-V, X7R, 10%</td>
<td>0603</td>
<td>C1608X7R1C105K</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>C3</td>
<td>Capacitor, Ceramic, 10-pF, 50-V, C0G, 5%</td>
<td>0603</td>
<td>C1608C0G1H100DB</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>C4</td>
<td>Capacitor, Ceramic, 22-µF, 16-V, X7R, 20%</td>
<td>1210</td>
<td>C3225X7R1C226M</td>
<td>TDK</td>
</tr>
<tr>
<td>0</td>
<td>C5</td>
<td>Capacitor, Ceramic, xx-µF, xx-V</td>
<td>0805</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>J1–J5</td>
<td>Header, 2-pin, 100-mil spacing, (36-pin strip)</td>
<td>0.100 × 2</td>
<td>PTC36SAAN</td>
<td>Sullins</td>
</tr>
<tr>
<td>2</td>
<td>JP1, JP2</td>
<td>Header, 3-pin, 100-mil spacing, (36-pin strip)</td>
<td>0.100 × 3</td>
<td>PTC36SAAN</td>
<td>Sullins</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>Inductor, SMT, 6.8-µH, 1.6-A, 49.2-mΩ</td>
<td>0.276 sq</td>
<td>SLF7032T-6R8M1R6</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>Resistor, Chip, 549 kΩ, 1/16-W, 1%</td>
<td>0603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td>1</td>
<td>R2</td>
<td>Resistor, Chip, 294 kΩ, 1/16-W, 1%</td>
<td>0603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td>5</td>
<td>R3–R8</td>
<td>Resistor, Chip, 1.00 MΩ, 1/16-W, 1%</td>
<td>0603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td>1</td>
<td>R6</td>
<td>Resistor, Chip, 261 kΩ, 1/16-W, 1%</td>
<td>0603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td>1</td>
<td>U1</td>
<td>IC, Synchronous Step-Down Converter, 17V, 1.5A</td>
<td>QFN-16</td>
<td>TPS62110RSA</td>
<td>TI</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>PCB, 1.7-Inch × 1.25-Inch × 0.062-Inch</td>
<td>HPA101</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Shunt, 100-mil, black</td>
<td>0.100</td>
<td>929950-00</td>
<td>3M</td>
</tr>
</tbody>
</table>

5 Related Documentation From Texas Instruments
1. TPS62110 data sheet (SLVS585)
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