*User's Guide*

# *TPS54225 Step-Down Converter Evaluation Module User's Guide*

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## Trademarks

D-CAP2™ is a trademark of Texas Instruments.

# 1 Introduction

This user's guide contains background information for the TPS54225 as well as support documentation for the TPS54225EVM-538 evaluation module. Also included are the performance specifications, schematic and the bill of materials for the TPS54225EVM-538.

## 1.1 Background

The TPS54225 is a single, adaptive on-time D-CAP2™ mode synchronous buck converter requiring a very low external component count. The D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS54225 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS54225 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS54225 DC/DC synchronous converter is designed to provide up to a 2-A output from an input control voltage source of 4.5 V to 18 V and an input power voltage source of 2 V to 18 V. The output voltage range is from 0.76 V to 5.5 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1.

The TPS54225EVM-538 evaluation module is a single synchronous buck converter providing 1.05 V at 2 A from 5-V to 17-V input. This user's guide describes the TPS54225EVM-538 performance.

**Table 1-1. Input Voltage and Output Current Summary**

| EVM | INPUT VOLTAGE RANGE | OUTPUT CURRENT RANGE |
|---|---|---|
| TPS54225EVM-538 | VIN = 4.5 V to 17 V | 0 A to 2 A |

## 1.2 Performance Specification Summary

A summary of the TPS54225EVM-538 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of VIN = 12 V and an output voltage of 1.05 V, unless otherwise noted. The ambient temperature is 25°C for all measurement, unless otherwise noted.

**Table 1-2. TPS54225EVM-538 Performance Specifications Summary**

| SPECIFICATIONS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input voltage range (VIN) | | | 4.5 | 12 | 17 | V |
| CH1 | Output voltage | | | 1.05 | | V |
| | Operating frequency | VIN = 12 V, $I_O$ = 1 A | | 700 | | kHz |
| | Output current range | | 0 | | 2 | A |
| | Over current limit | VIN = 12 V | | 3.1 | | A |
| | Output ripple voltage | VIN = 12 V, $I_O$ = 2 A | | 7 | | $mV_{PP}$ |

## 1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54225. Some modifications can be made to this module.

### 1.3.1 Output Voltage Set Point

To change the output voltage of the EVMs, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage above 0.765 V. The value of R1 for a specific output voltage can be calculated using Equation 1 and Equation 2.

For output voltage from 0.76 V to 2.5 V:

$$VO = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

For output voltage over 2.5 V:

$$VO = (0.763 + 0.0017 \times VO) \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Table 1-3 lists the R1 values for some common output voltages. For higher output voltages, a feedforward capacitor may be required. Pads for this component (C2) are provided on the printed circuit board. C2 is used for faster load transient response and is normally not used. Note that the values given in Table 1-3 are standard values, and not the exact value calculated using Table 1-3.

**Table 1-3. Output Voltages**

| OUTPUT VOLTAGE (V) | R1 (kΩ) | R2 (kΩ) | C2 (pF) | L1 (µH) |
|---|---|---|---|---|
| 1.0 | 6.81 | 22.1 | | 2.2 |
| 1.05 | 8.25 | 22.1 | | 2.2 |
| 1.2 | 12.7 | 22.1 | | 2.2 |
| 1.8 | 30.1 | 22.1 | | 3.3 |
| 2.5 | 49.9 | 22.1 | | 3.3 |
| 3.3 | 73.2 | 22.1 | 680 | 3.3 |
| 5.0 | 121 | 22.1 | 220 | 4.7 |

# 2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54225EVM-538. The section also includes test results typical for the evaluation modules and the following:

- Efficiency
- Output load regulation
- Output line regulation
- Load transient response
- Output voltage ripple
- Input voltage ripple
- Start up
- Switching frequency

## 2.1 Input / Output Connections

The TPS54225EVM-538 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20 AWG wires. The load must be connected to J2 through a pair of 20 AWG wires. The maximum load current capability is 2 A. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the $V_{IN}$ input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

**Table 2-1. Connection and Test Points**

| Reference Designator | Function |
|---|---|
| J1 | $V_{IN}$ (see Table 1-1 for $V_{IN}$ range) |
| J2 | $V_{OUT}$, 1.05 V at 2 A maximum |
| JP1 | EN control. Connect EN to OFF to disable, connect EN to ON to enable. |
| TP1 | $V_{IN}$ test point at $V_{IN}$ connector |
| TP2 | GND test point at $V_{IN}$ |
| TP3 | EN test point |
| TP4 | $V_{CC}$ test point |
| TP5 | Analog ground test point |
| TP6 | Switch node test point |
| TP7 | Power good test point |
| TP8 | Output voltage test point |
| TP9 | Ground test point at output connector |

## 2.2 Start-Up Procedure

1. Make sure the jumper at JP1 (Enable control) is set from EN to OFF.
2. Apply appropriate VIN voltage to VIN and PGND terminals at J1.
3. Move the jumper at JP1 (Enable control) to cover EN and ON. The EVM will enable the output voltage.

## 2.3 Efficiency

Figure 2-1 shows the efficiency for the TPS54225EVM-538 at an ambient temperature of 25°C.

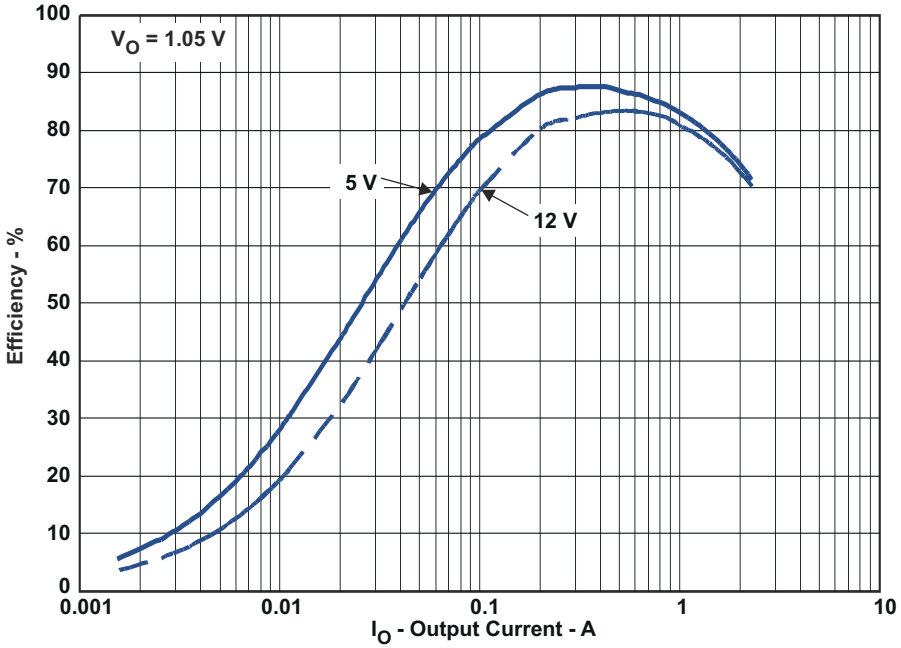


**Figure 2-1. TPS54225EVM-538 Efficiency**

## 2.4 Load Regulation

The load regulation for the TPS54225EVM-538 is shown in Figure 2-2.

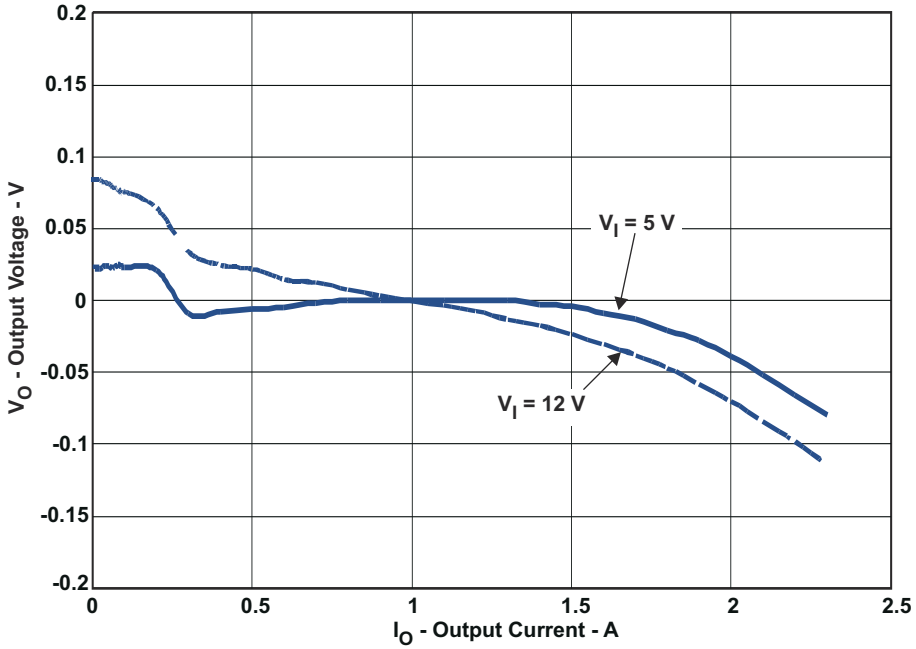


**Figure 2-2. TPS54225EVM-538 Load Regulation**

## 2.5 Line Regulation

The line regulation for the TPS54225EVM-538 is shown Figure 2-3.

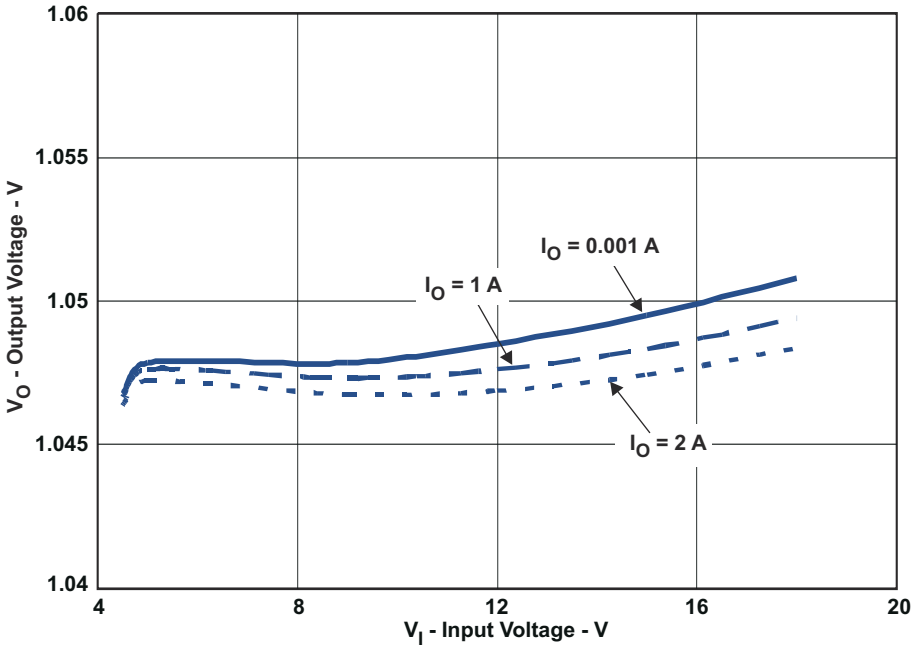


**Figure 2-3. TPS54225EVM-538 Line Regulation**

## 2.6 Load Transient Response

The TPS54225EVM-538 response to load transient is shown in Figure 2-4. The current step is from 0.5 A to 2 A. Total peak to peak voltage variation is as shown.

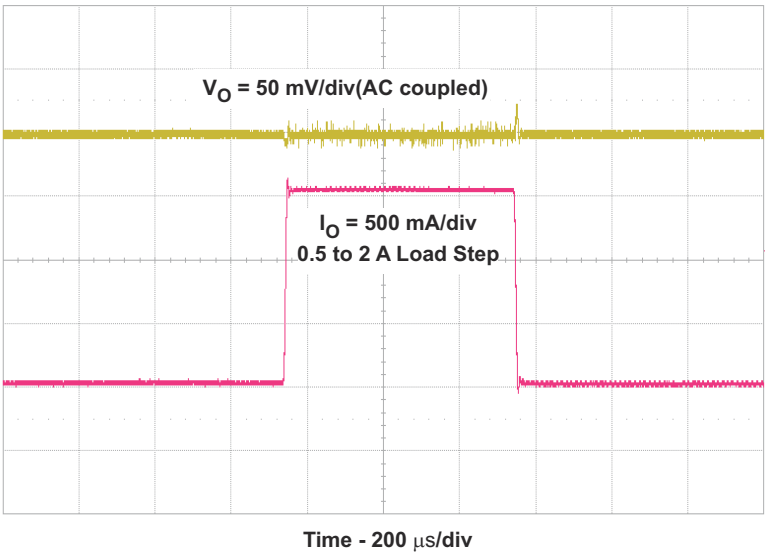


**Figure 2-4. TPS54225EVM-538 Load Transient Response**

## 2.7 Output Voltage Ripple

The TPS54225EVM-538 output voltage ripple is shown in Figure 2-5. The output current is the rated full load of 2A.

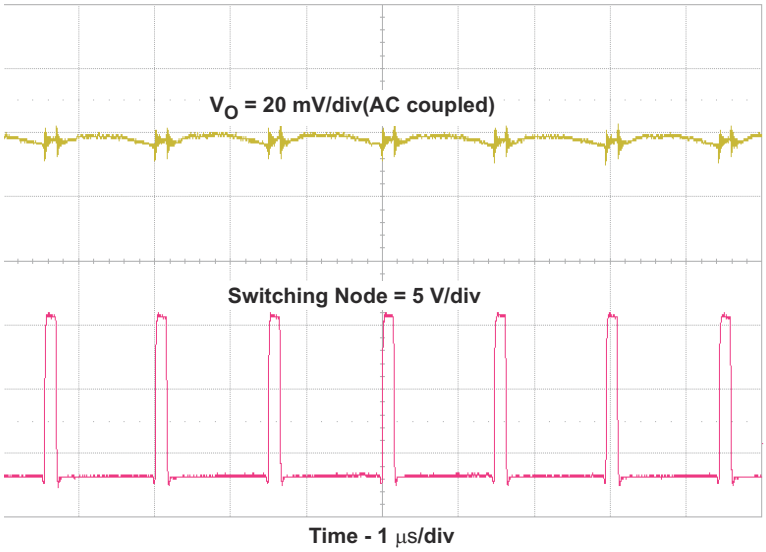


**Figure 2-5. TPS54225EVM-538 Output Voltage Ripple**

## 2.8 Input Voltage Ripple

The TPS54225EVM-538 input voltage ripple is shown in Figure 2-6. The output current is the rated full load of 2A.

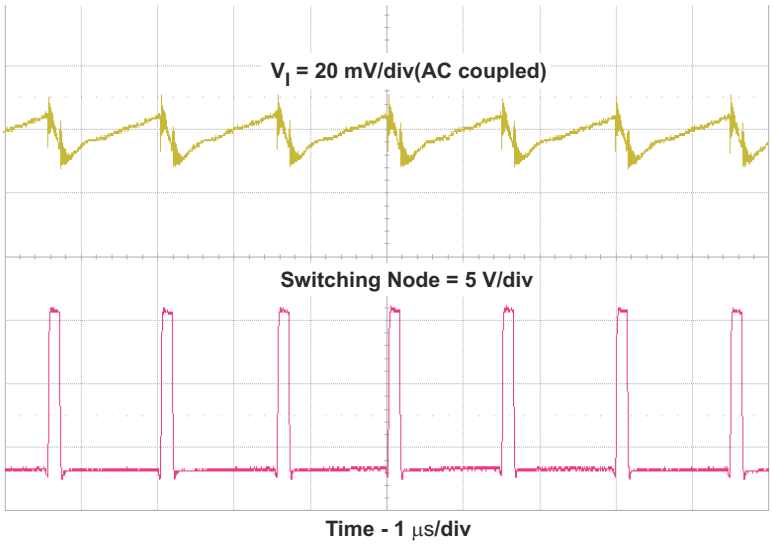


**Figure 2-6. TPS54225EVM-538 Input Voltage Ripple**

## 2.9 Start Up

The TPS54225EVM-538 start up waveform is shown in Figure 2-7.

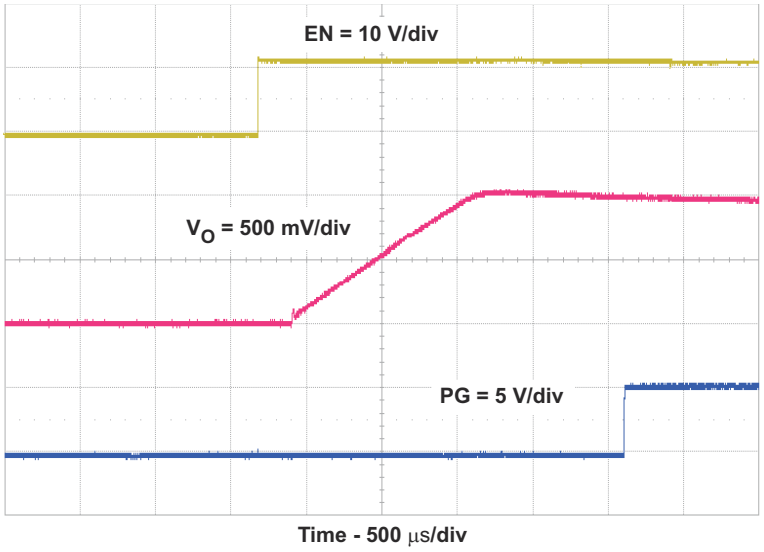


**Figure 2-7. TPS54225EVM-538 Start Up**

## 2.10 Switching Frequency

The TPS54225EVM-538 switching frequency is shown in Figure 2-8.

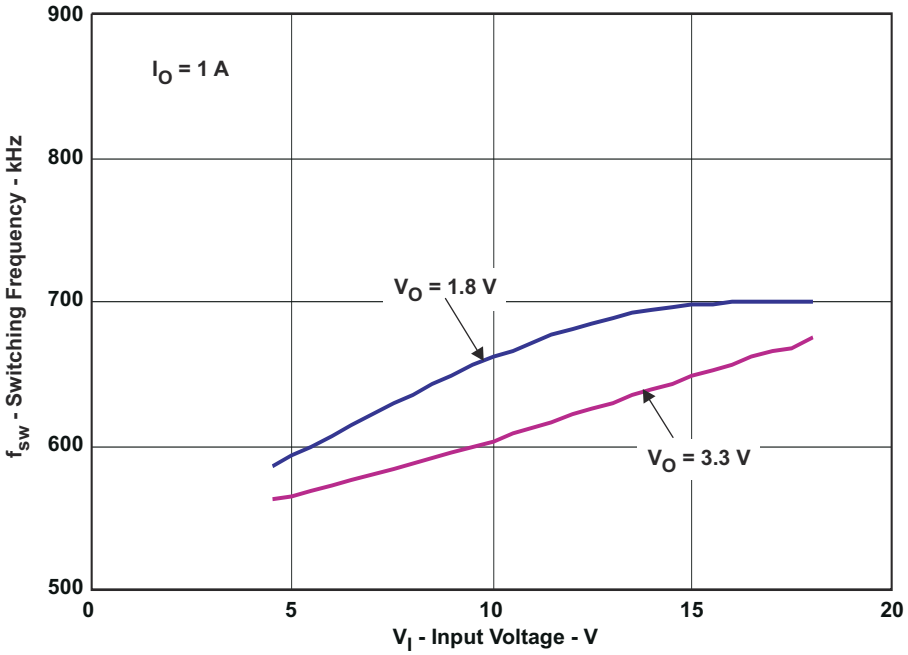


**Figure 2-8. TPS54225EVM-538 Switching Frequency**

# 3 Board Layout

This section provides description of the TPS54225EVM-538, board layout, and layer illustrations.

## 3.1 Layout

The board layout for the TPS54225EVM-538 and is shown in Figure 3-1 through Figure 3-6. The top layer contains the main power traces for VIN, VO and ground. Also on the top layer are connections for the pins of the TPS54225 and a large area filled with ground. Many of the signal traces are also located on the top side. The input decoupling capacitor are located as close to the IC as possible. The input and output connectors, test points and most of the components are located on the top side. R3, the 0-Ω resistor that connects VIN to VCC and R4, the power good pull up, are located on the back side. Analog ground and power ground are connected at a single point on the top layer near pin 5 of the TPS54225. The internal layer 1 is a split plane containing analog and power grounds. The internal layer 2 is primarily power ground. There are also a fill area of VIN and a trace routing VCC to the enable control jumper JP1. The bottom layer is primarily analog ground. There are also traces to connect VIN to VCC through R3, traces for the power good signal and the feedback trace from VOUT to the voltage setpoint divider network.

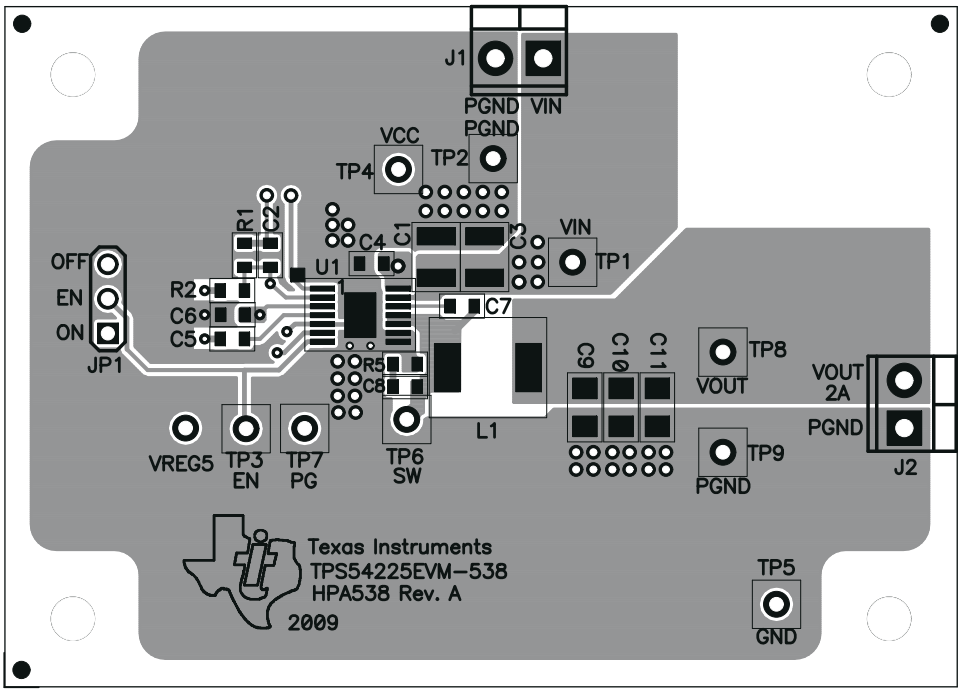


**Figure 3-1. Top Assembly**

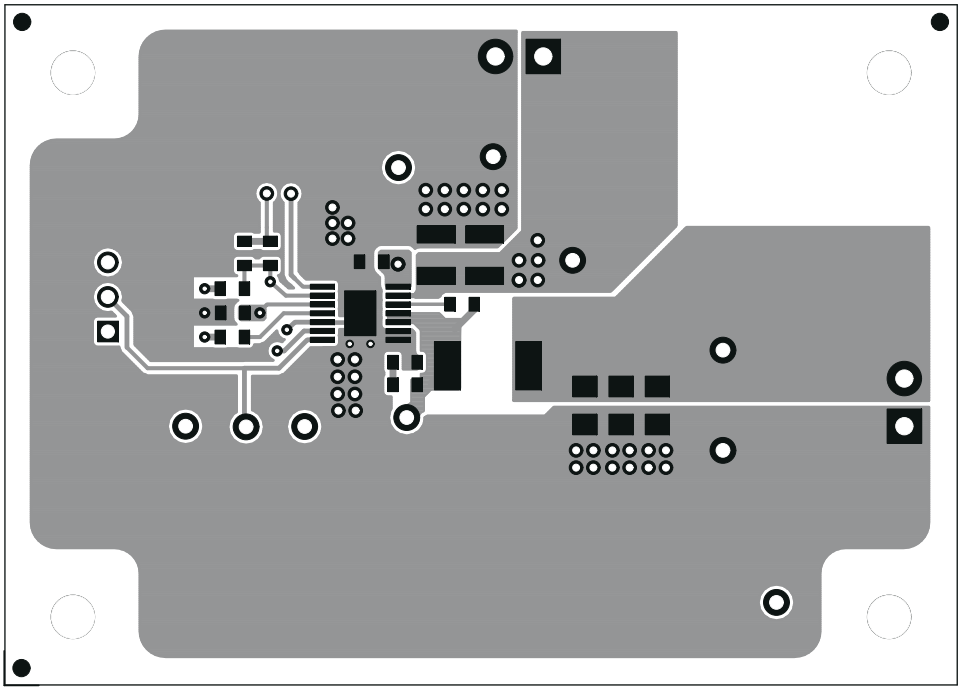

**Figure 3-2. Top Layer**

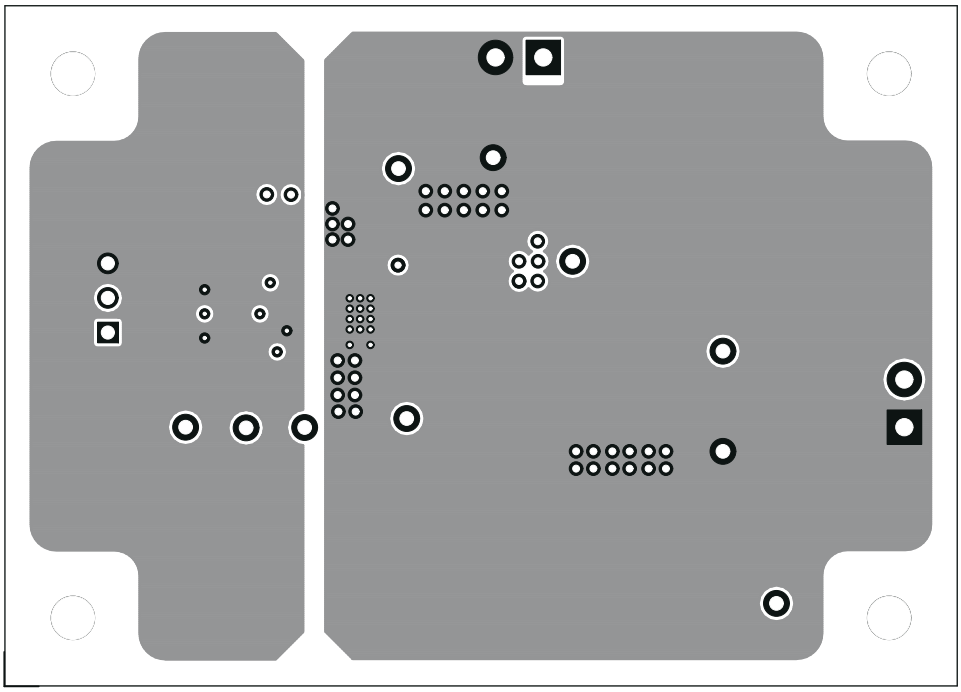

**Figure 3-3. Internal Layer 1**

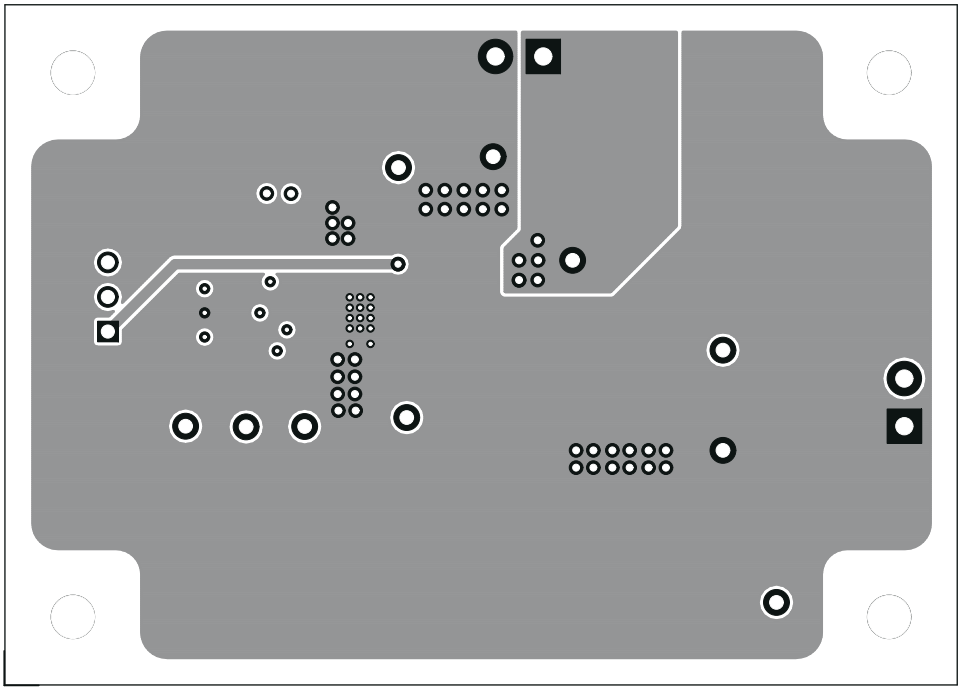

**Figure 3-4. Internal Layer 2**

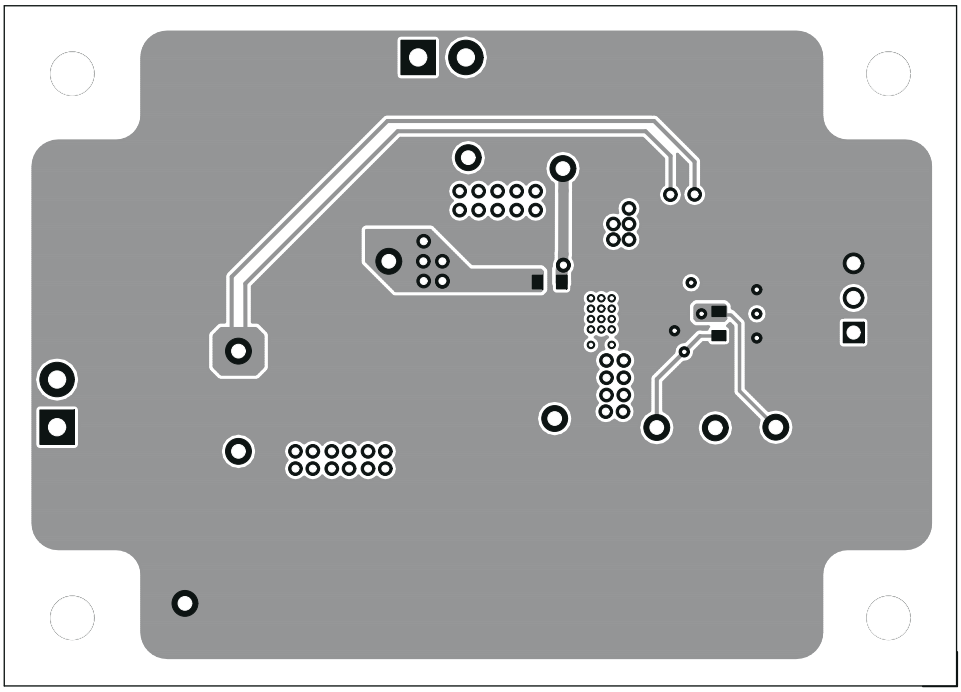

**Figure 3-5. Bottom Layer**

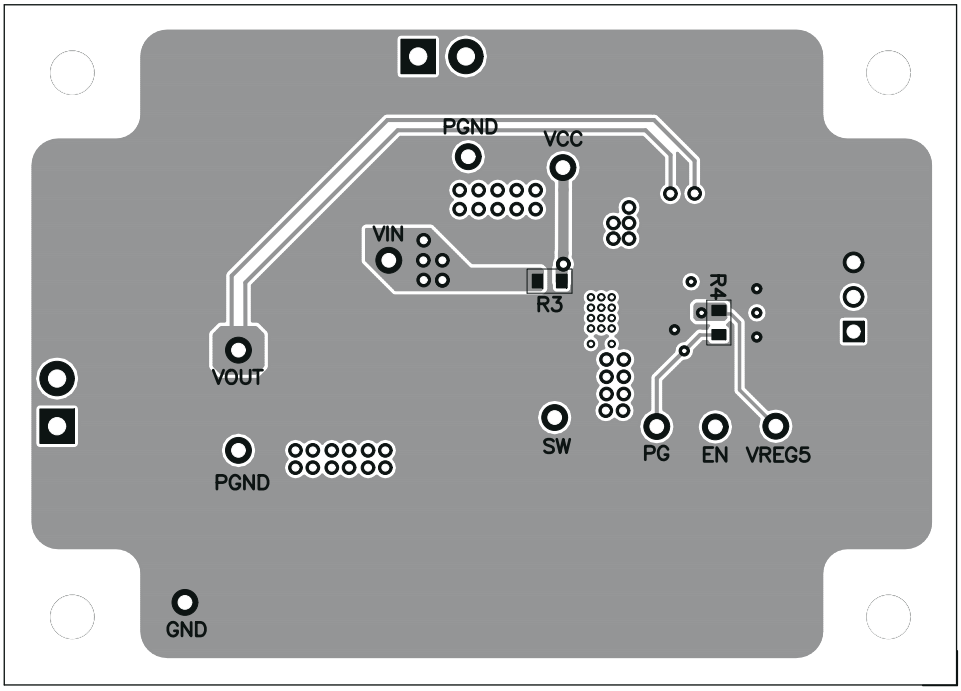


**Figure 3-6. Bottom Assembly**

# 4 Schematic, Bill of Materials and Reference

This section presents the TPS54225EVM-538 schematic, bill of materials and reference.

## 4.1 Schematic

Figure 4-1 is the schematic for the TPS54225EVM-538.

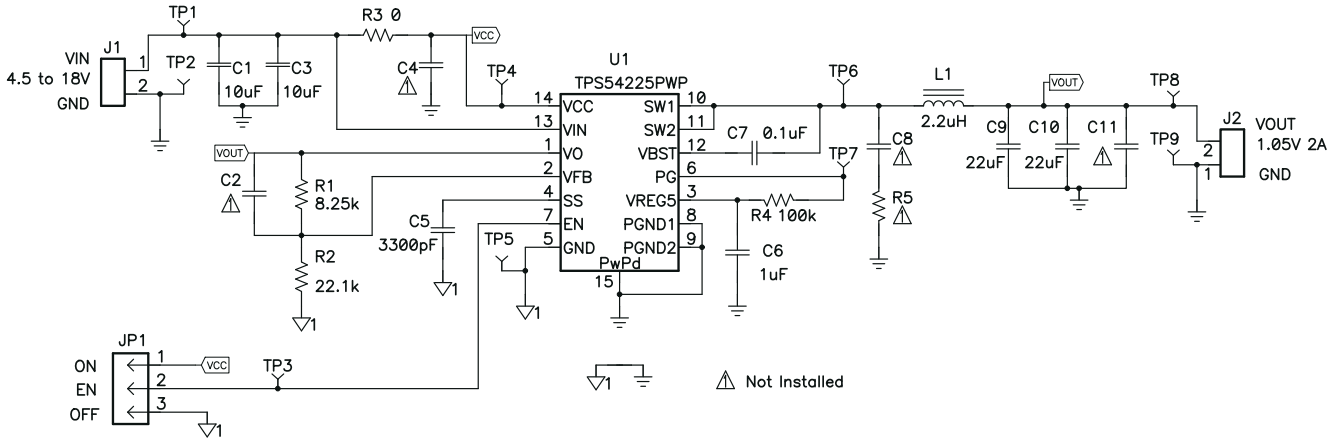


**Figure 4-1. TPS54225EVM-538 Schematic Diagram**

## 4.2 Bill of Materials

**Table 4-1. Bill of Materials**

| RefDes | QTY | Value | Description | Size | Part Number | MFR |
|---|---|---|---|---|---|---|
| C1, C3 | 2 | 10 µF | Capacitor, Ceramic, 25 V, X5R, 20% | 1210 | C3225X5R1E106M | TDK |
| C11 | 0 | Open | Capacitor, Ceramic | 1206 | Std | Std |
| C2, C4, C8 | 0 | Open | Capacitor, Ceramic | 0603 | Std | Std |
| C5 | 1 | 3300 pF | Capacitor, Ceramic, 25 V, X7R , 10% | 0603 | Std | Std |
| C6 | 1 | 1 µF | Capacitor, Ceramic, 16 V, X7R, 10% | 0603 | Std | Std |
| C7 | 1 | 0.1 µF | Capacitor, Ceramic, 50 V, X7R, 10% | 0603 | Std | Std |
| C9, C10 | 2 | 22 µF | Capacitor, Ceramic, 6.3 V, X5R, 20% | 1206 | C3216X5R0J226M | TDK |
| J1, J2 | 2 | ED555/2DS | Terminal Block, 2-pin, 6-A, 3.5mm | 0.27 × 0.25 inch | ED555/2DS | Sullins |
| JP1 | 1 | PEC03SAAN | Header, Male 3-pin, 100-mil spacing | 0.100 inch × 3 | PEC03SAAN | Sullins |
| L1 | 1 | 2.2 µH | Inductor, SMT, 8.2 A, 17.3 milliΩ | 0.256 × 0.280 inch | SPM6530T-2R2M | TDK |
| R1 | 1 | 8.25 k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R2 | 1 | 22.1 k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R3 | 1 | 0 | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R4 | 1 | 100 k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| R5 | 0 | Open | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std |
| TP1, TP3, TP4, TP6, TP7, TP8, TP9 | 3 | 5000 | Test Point, Red, Thru Hole Color Keyed | 0.100 × 0.100 inch | 5000 | Keystone |
| TP2, TP5, TP9 | 3 | 5001 | Test Point, Black, Thru Hole Color Keyed | 0.100 × 0.100 inch | 5001 | Keystone |
| U1 | 1 | TPS54225PWP | IC, 2-A Output Single Sync. Step-Down | | TPS54225PWP | TI |
| – | 1 | | Shunt, 100-mil, Black | 0.100 | 929950-00 | 3M |
| – | 1 | | PCB, 2.76 In × 1.97 In × 0.062 In | | HPA538 | Any |

## 4.3 Reference

Texas Instruments, *TPS54225 Single Synchronous Converter with Integrated High Side and Low Side MOS FET*

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision * (November 2009) to Revision A (October 2021)** **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. .....2

- Updated the user's guide title ..... 2

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