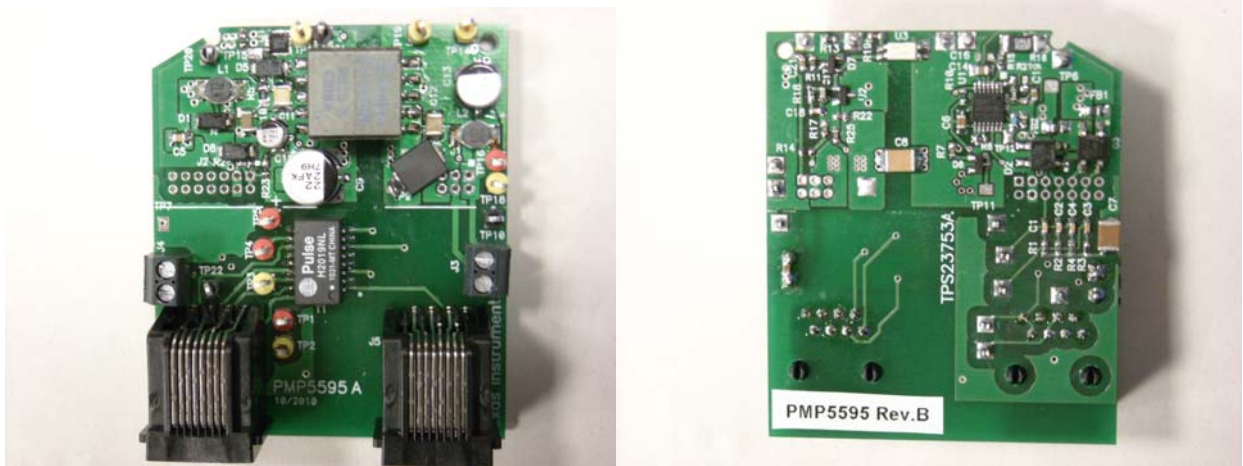


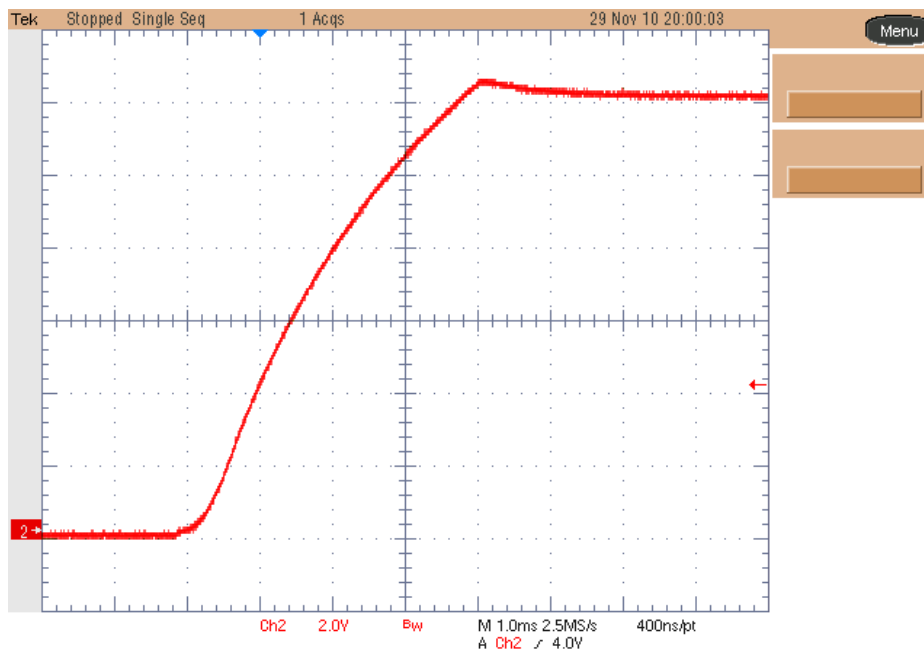
Photo of the prototype:

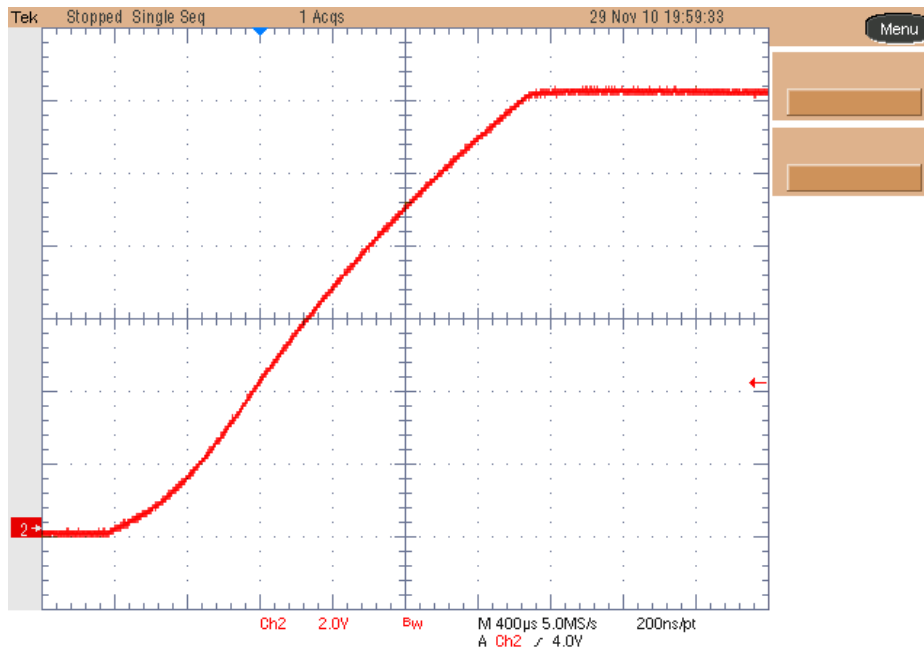


1. Startup

The output voltage behavior at startup is shown in the images below. The input voltage was set to 32V and the load was set to full load for the upper picture and no load for the lower one..

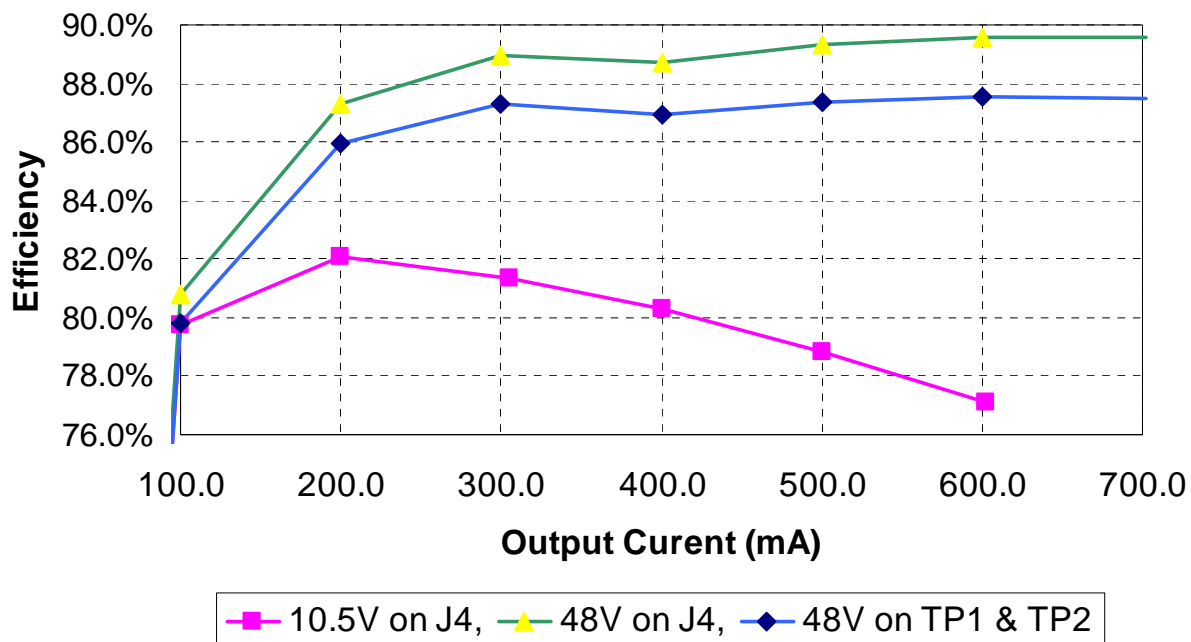
Channel 2: Output Voltage (2 V/div, 1msec/div and 400usec/div.).





2. Efficiency

The efficiency data is shown in the tables and graph below. The measurements were taken at 10.5V, 48V (connected to J4) and 48V (connected to TP1 and TP2) input voltage.



Vin connected to J4

Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff. (%)
0.0	12.085	0.00	10.8	10.52	0.11	0.11	0.0%
100.1	12.083	1.21	144.5	10.50	1.52	0.31	79.7%
200.0	12.082	2.42	280.1	10.51	2.94	0.53	82.1%
305.3	12.080	3.69	431	10.52	4.53	0.85	81.3%
400.0	12.079	4.83	572	10.52	6.02	1.19	80.3%
500.0	12.078	6.04	729	10.51	7.66	1.62	78.8%
602.3	12.076	7.27	897	10.52	9.44	2.16	77.1%

Vin connected to J4

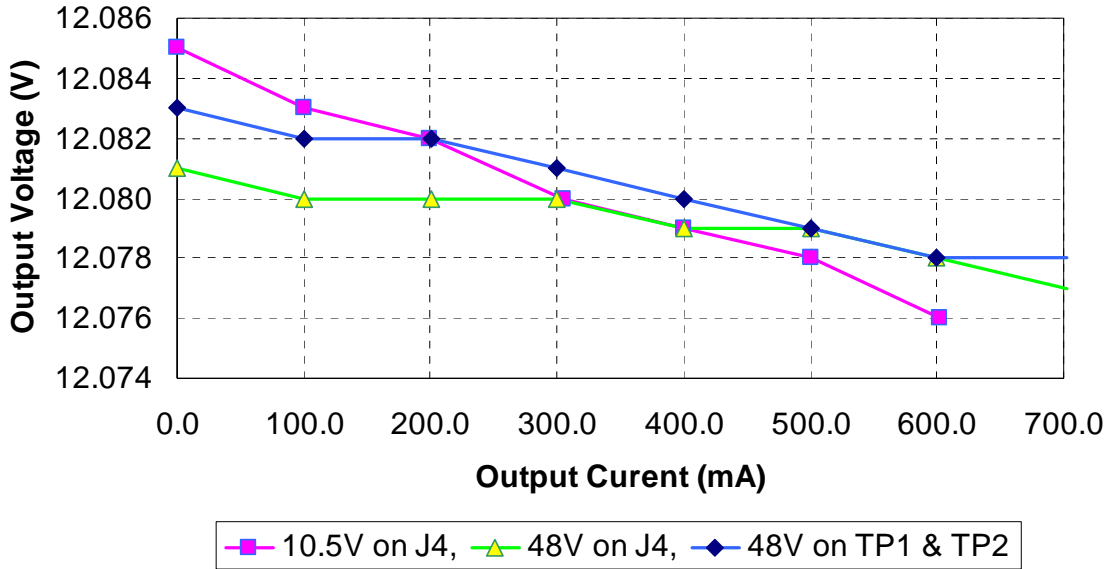
Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff. (%)
0.0	12.081	0.00	2.41	48.00	0.12	0.12	0.0%
100.2	12.080	1.21	31.2	48.00	1.50	0.29	80.8%
200.1	12.080	2.42	57.7	48.00	2.77	0.35	87.3%
300.0	12.080	3.62	84.9	48.00	4.08	0.45	88.9%
400.0	12.079	4.83	113.5	48.00	5.45	0.62	88.7%
500.0	12.079	6.04	140.9	48.00	6.76	0.72	89.3%
600.0	12.078	7.25	168.6	48.00	8.09	0.85	89.5%
702.2	12.077	8.48	197.3	48.00	9.47	0.99	89.5%

**Vin connected to TP1
and TP2**

Iout (mA)	Vout (V)	Pout (W)	Iin (mA)	Vin (V)	Pin (W)	Ploss (W)	Eff. (%)
0.0	12.083	0.00	2.30	48.00	0.11	0.11	0.0%
100.2	12.082	1.21	31.6	48.00	1.52	0.31	79.8%
200.1	12.082	2.42	58.6	48.00	2.81	0.40	86.0%
300.0	12.081	3.62	86.5	48.00	4.15	0.53	87.3%
400.0	12.080	4.83	115.8	48.00	5.56	0.73	86.9%
500.0	12.079	6.04	144.0	48.00	6.91	0.87	87.4%
600.0	12.078	7.25	172.5	48.00	8.28	1.03	87.5%
702.2	12.078	8.48	202.0	48.00	9.70	1.21	87.5%

3. Output Voltage Regulation

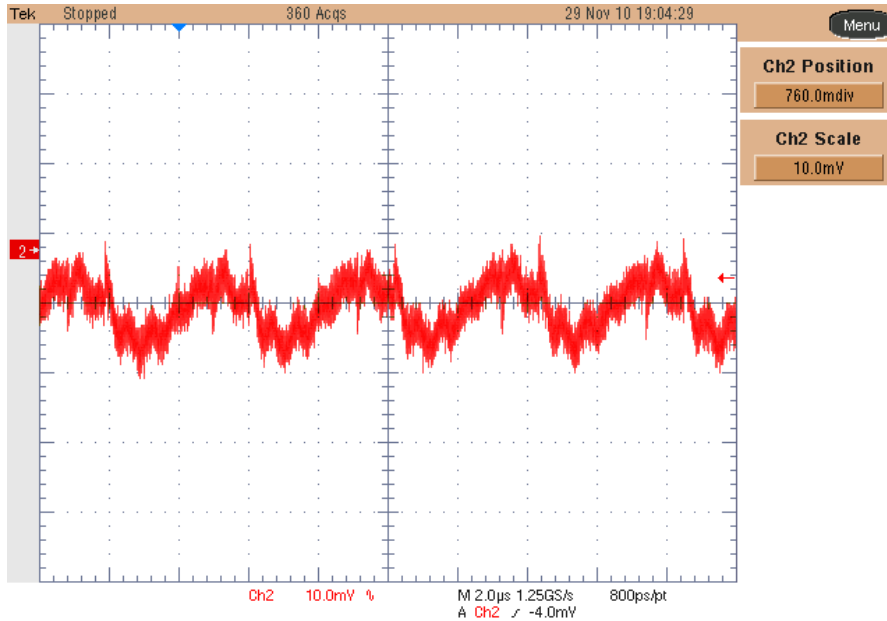
The output voltage regulation of the 12V output versus load has been taken at the same conditions as above.



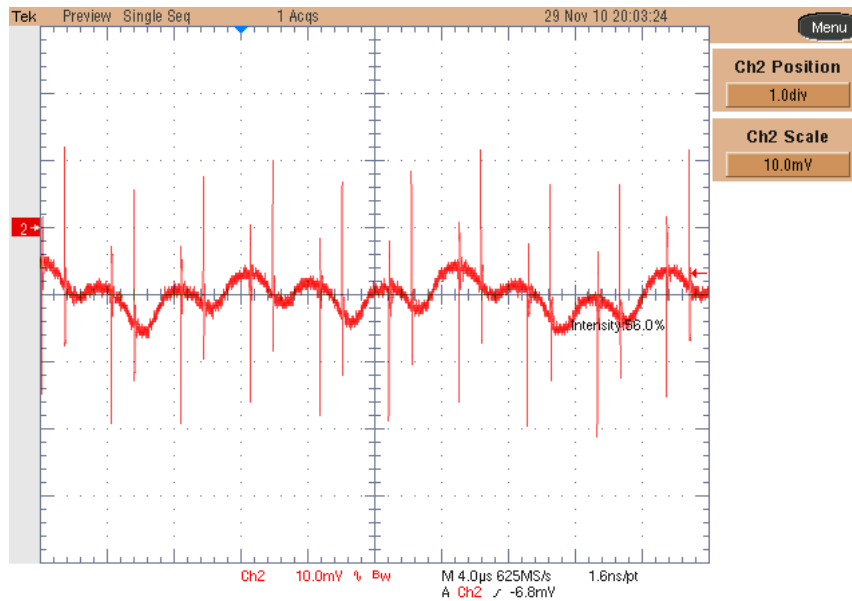
4. Input and Output Ripple Voltage

The ripple voltage waveforms measured at the terminal blocks are shown in the plots below. The input was set to 55V (worst case), while the load was set to 600mA.

Channel 2: **Output Voltage** (10 mV/div, 2usec/div, AC coupled, No BW limit).



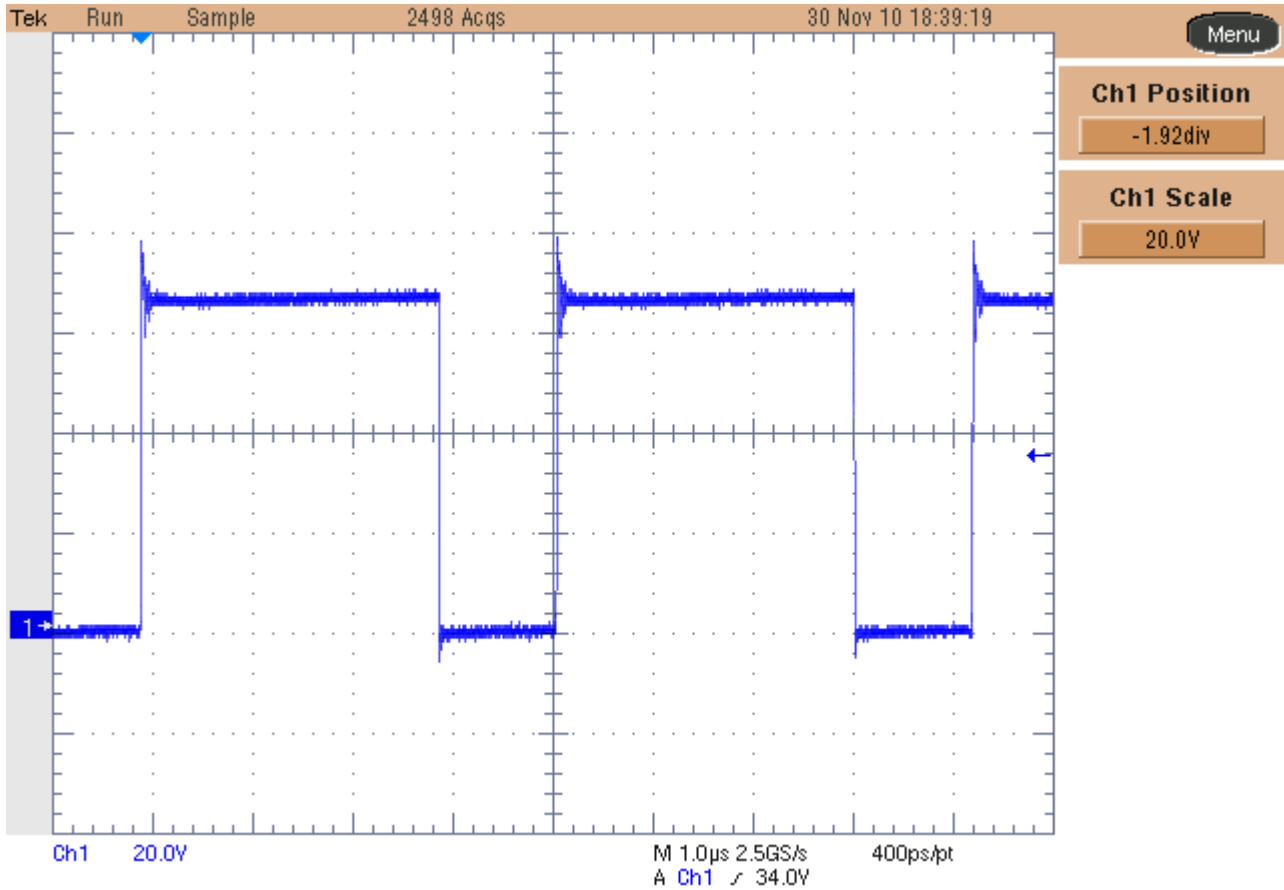
Channel 2: **Input Voltage**, measured on C5 (10 mV/div, 4usec/div, AC coupled, 20MHz BW limit).



5. Switching Waveforms

The images below show the drain-to-source waveforms of the power MOSFETs at full load. The input voltage was set to 48V_{in}.

Channel 2: “Q1 V_{ds}”, (20V/div, 1usec/div), no bandwidth reduction

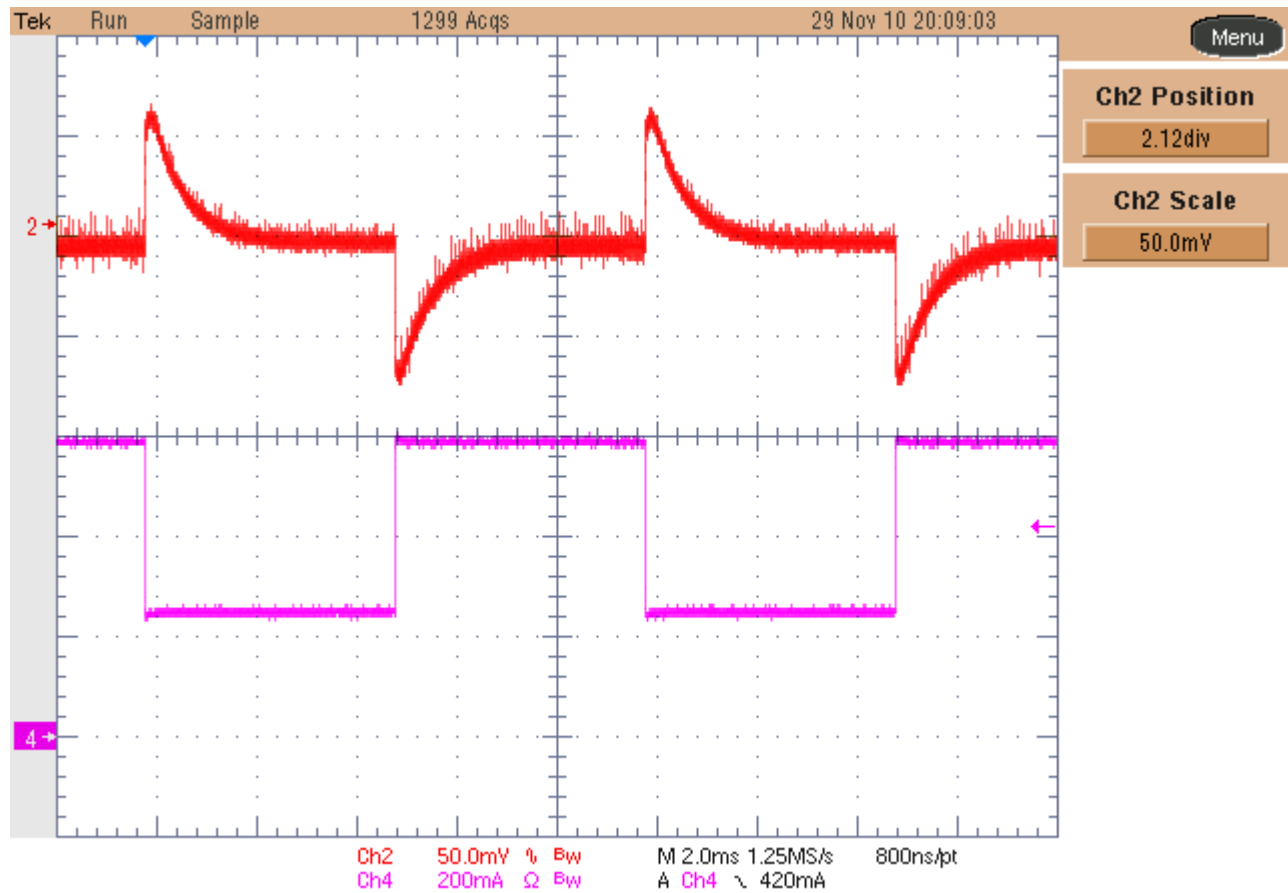


6. Transient Response

The image below shows the transient response behavior. The input voltage was set to the nominal voltage: 48V, and the load on the 12Vout switched from 250mA to 600mA.

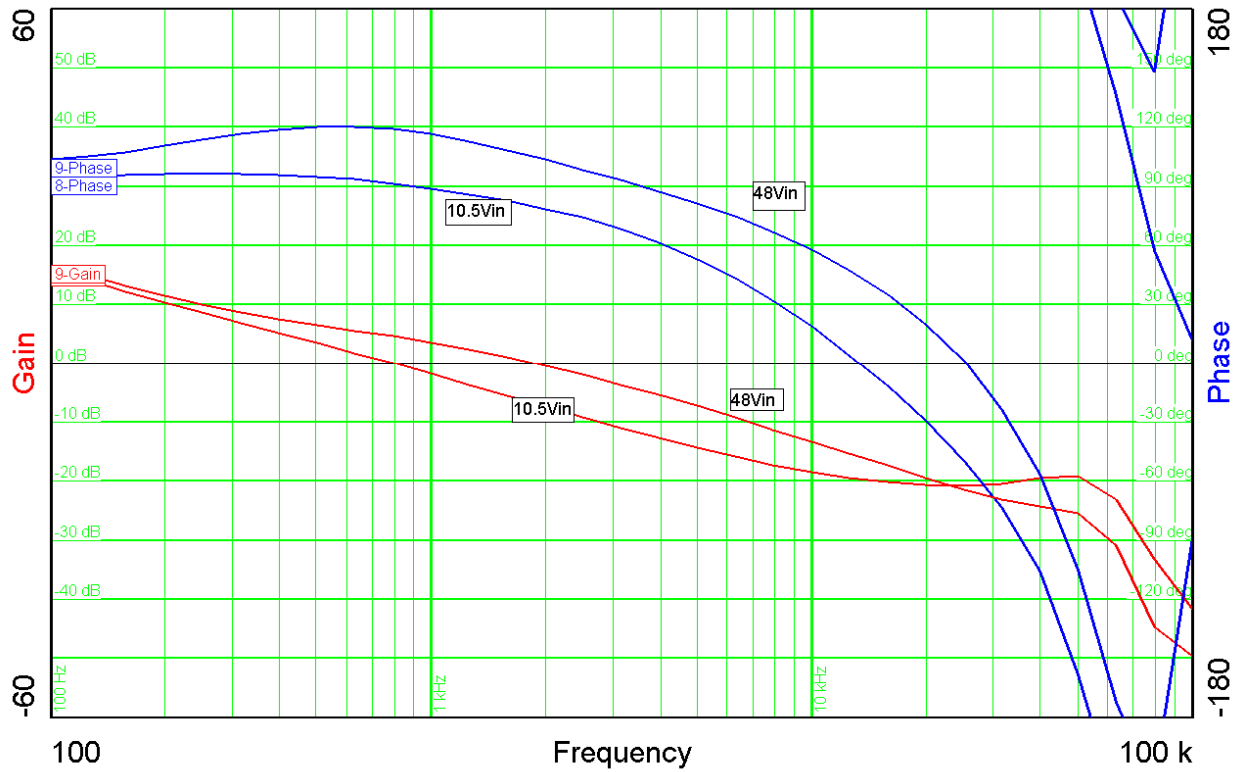
Channel 2: Output Voltage (50mV/div, AC coupled, 2msec/div, 20MHz bandwidth)

Channel 4: Switched current on the 12V output (200mA/div, DC coupled)



7. Loop Analysis

The graph below shows the loop measurement at 10.5V_{in} and 48V_{in} @ full load (700mA). The worst case crossover frequency was 800 Hz and the worst case phase margin 90 deg.



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