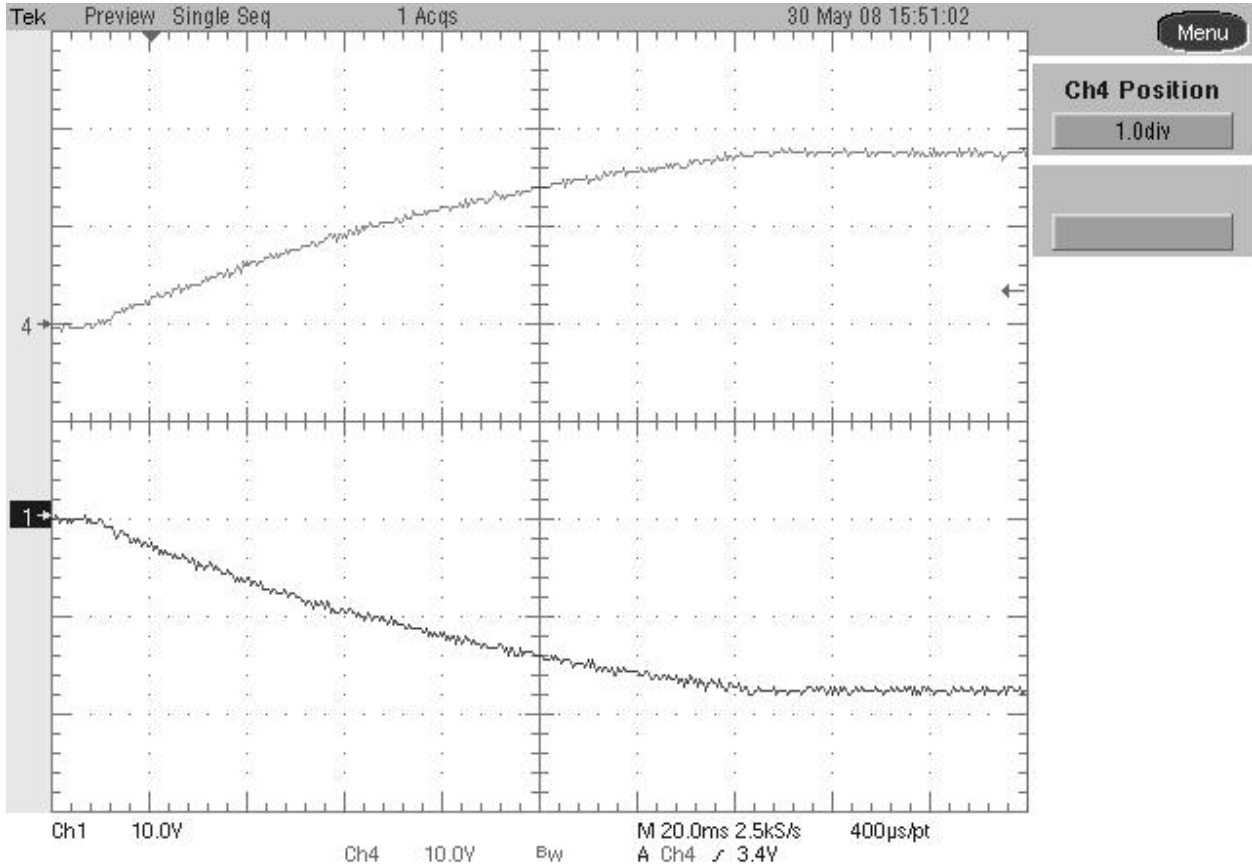


1 Startup

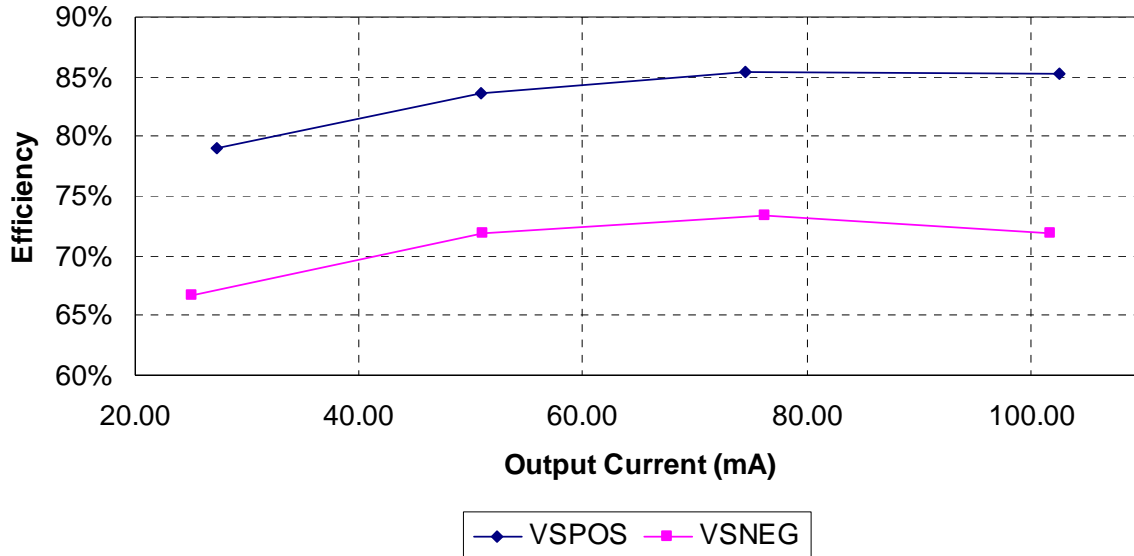
The output voltage at startup is shown in the image below. Battery voltage is 3.7V. The output was set at +/-18V and loaded with 10mA on each output.

Channel 4 shows the VSPOS output, and channel 1 shows the VSNEG output (both 10 V/div).



2 VSPOS and VSNEG converter efficiency

The efficiency data is shown in the tables and graph below. For simplicity and accuracy of measurements, the data was measured using a 5V PSU connected on +5V node. The VGPOS and VGNEG charge pump circuit has been disconnected.



I _{out} (mA)	V _{out} (V)	P _{out} (W)	I _{in} (mA)	V _{in} (V)	P _{in} (W)	P _{loss} (W)	Eff VSPOS
27.3	18	0.491	124	5.013	0.622	0.130	79.1%
50.9	18	0.916	220	4.984	1.096	0.180	83.6%
74.5	18	1.341	317	4.955	1.571	0.230	85.4%
102.5	18	1.845	440	4.917	2.163	0.318	85.3%

I _{out} (mA)	V _{out} (V)	P _{out} (W)	I _{in} (mA)	V _{in} (V)	P _{in} (W)	P _{loss} (W)	Eff VSNEG
25.0	18	0.450	135	4.999	0.675	0.225	66.7%
51.1	18	0.920	258	4.958	1.279	0.359	71.9%
76.2	18	1.372	372	5.021	1.868	0.496	73.4%
101.7	18	1.831	507	5.022	2.546	0.716	71.9%

3 Output Voltage Regulation

The VSPOS and VSNEG output voltage regulation have been characterized under the following conditions:

50% of load on VGPOS and VGNEG

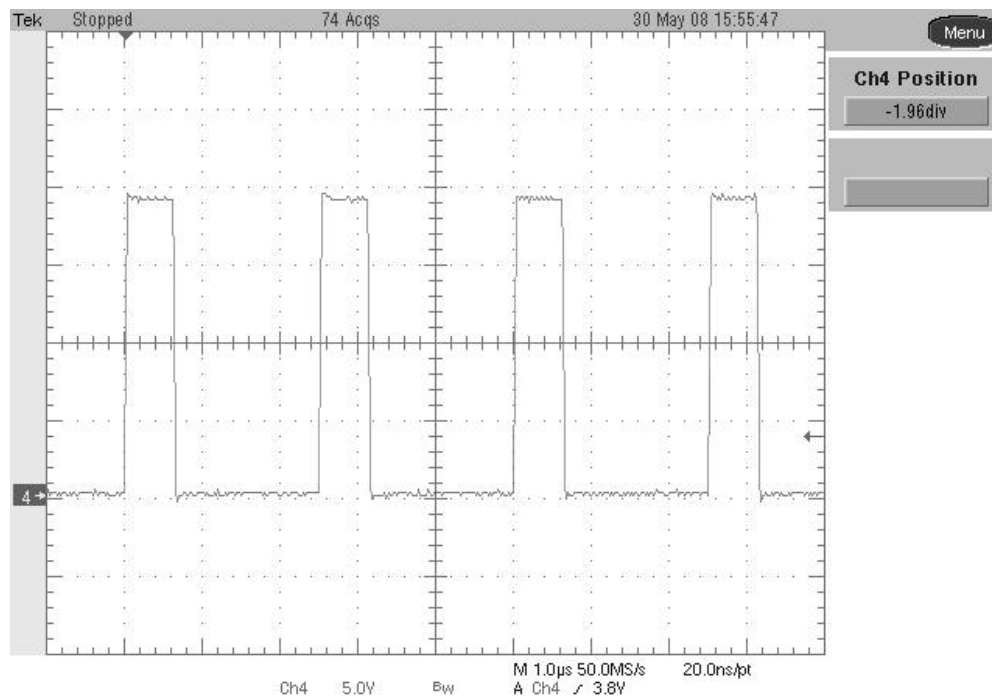
Output voltages swing from +/-14V to +/-18V

- 1) 0% load on VSPOS and VSNEG
- 2) 100% load on VSPOS and 0% load on VSNEG
- 3) 0% load on VSPOS and 100% load on VSNEG

The result is a maximum error between the +18V and the -18V of 0.02V (0.11%)

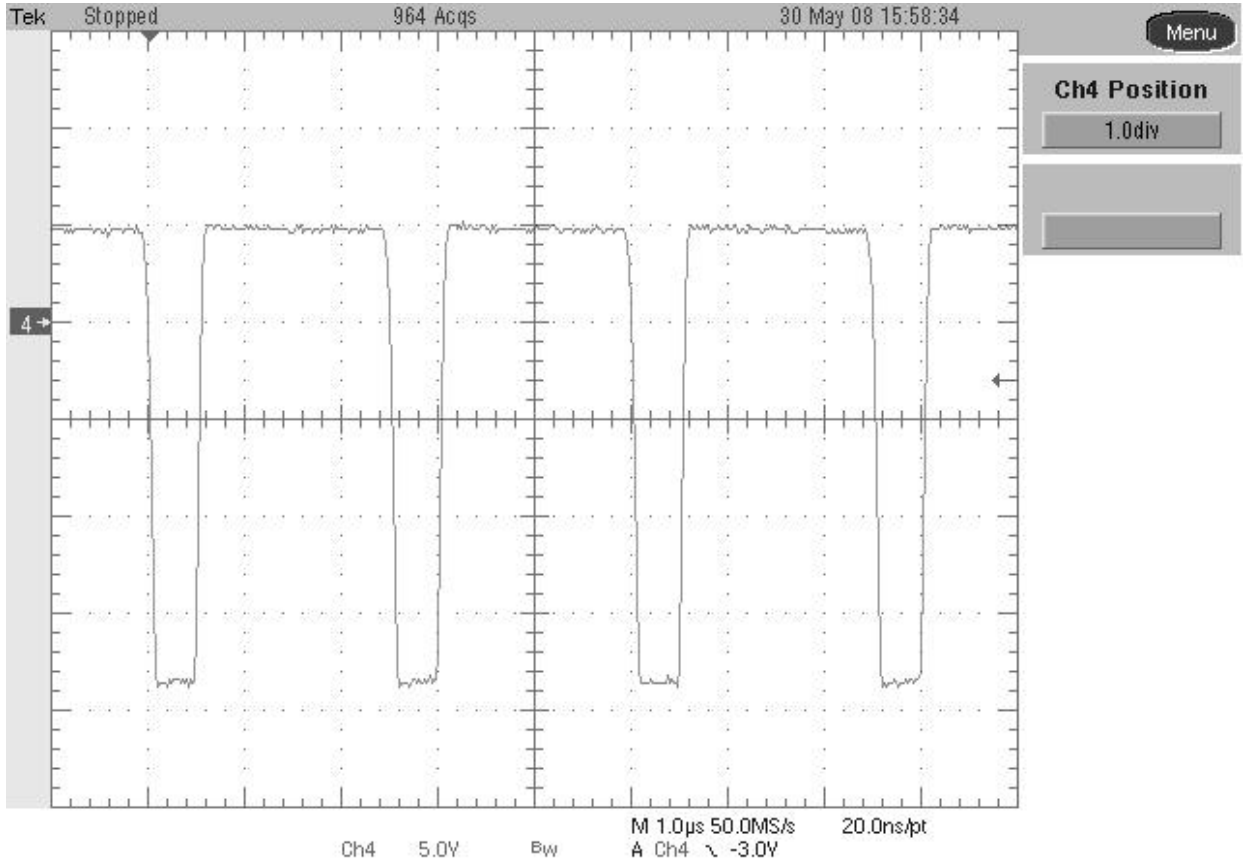
4 VSPOS SWITCH NODE

The VSPOS converter switch node is shown below. Channel 4 (5V/div)



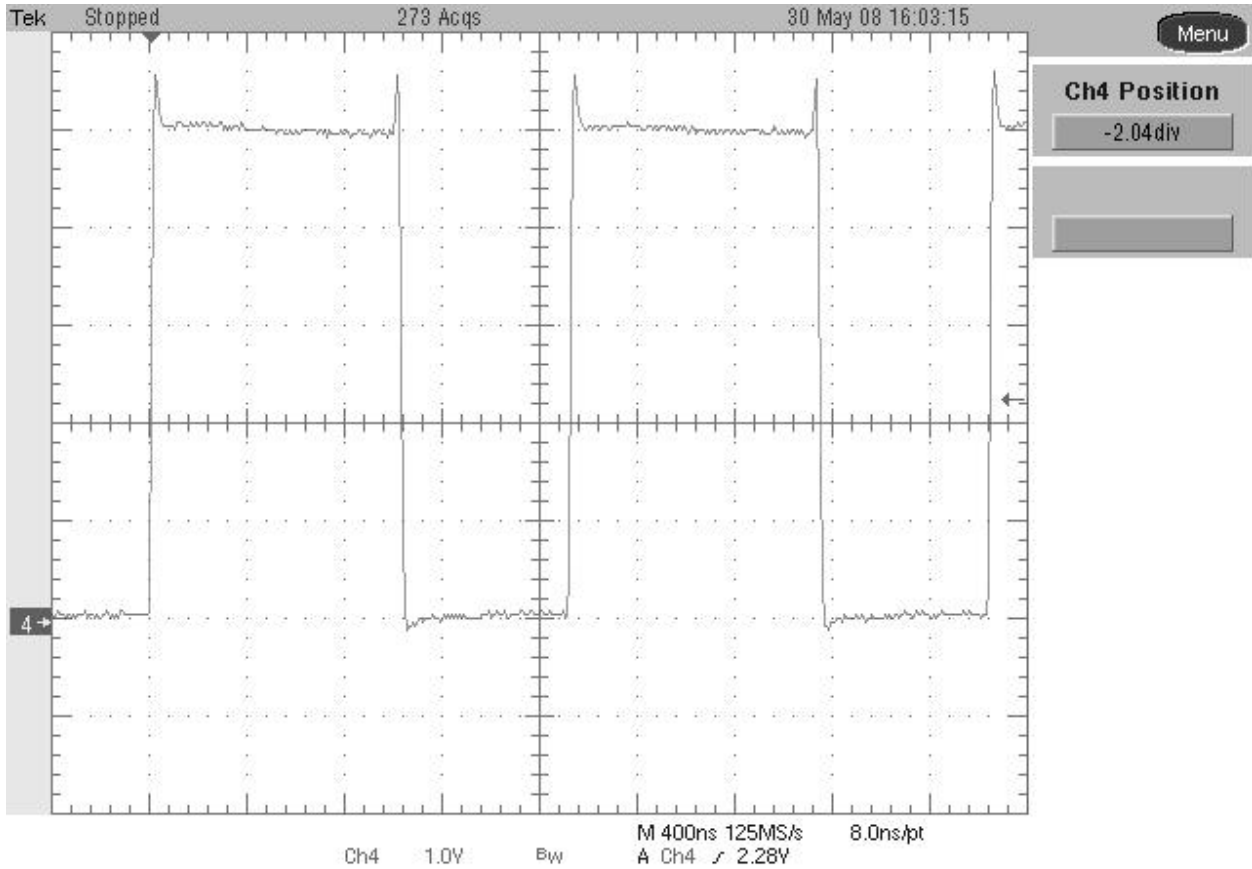
5 VSNEG SWITCH NODE

The VSNEG converter switch node is shown below. Channel 4 (5V/div)



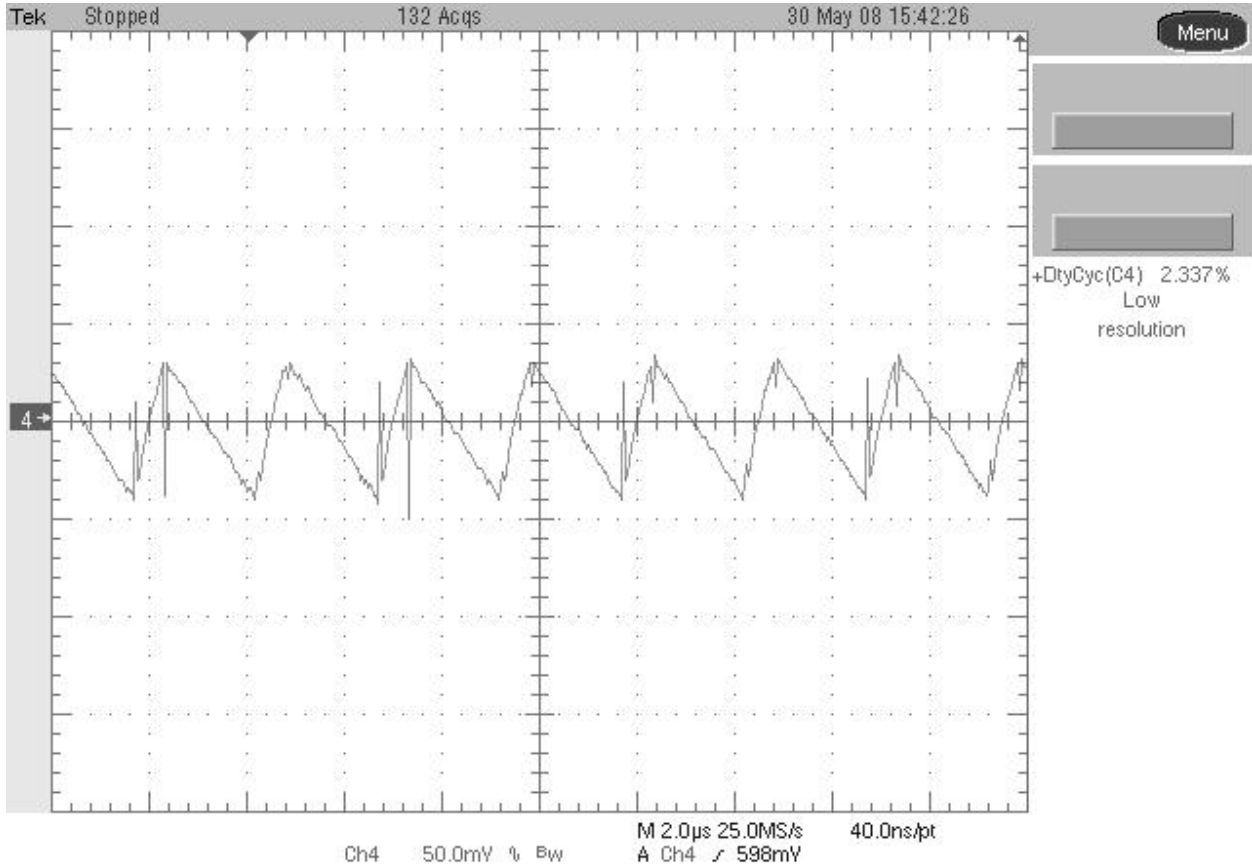
6 U2 SWITCH NODE

Channel 4 (1V/div) shows U2 switch node in the plot below. The battery voltage was set at 3.7V, the 5V output load was set to 1A.



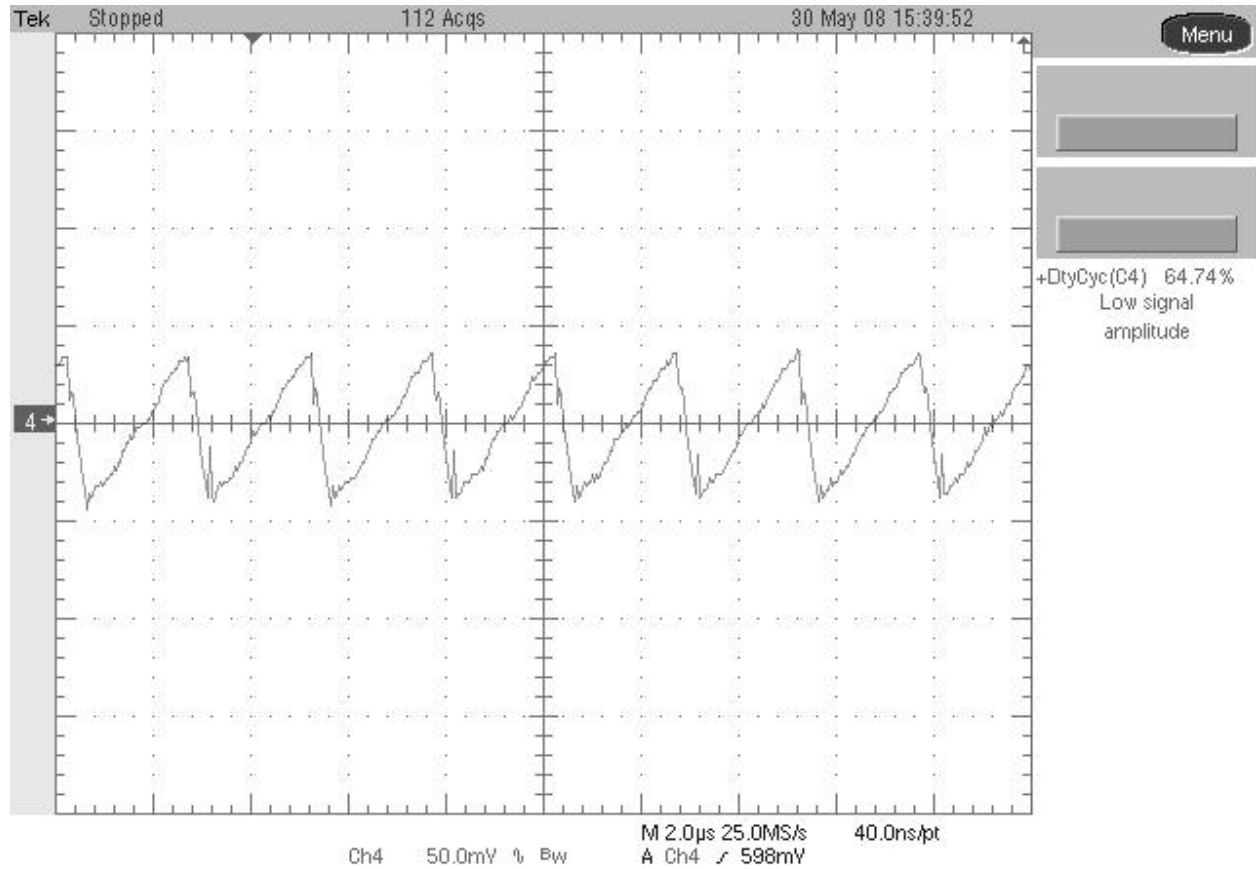
7 VSPOS Output Ripple Voltage

The VSPOS output ripple voltage is shown in the plot below. The battery voltage was set at 3.7V and the load was set to 0.1A.



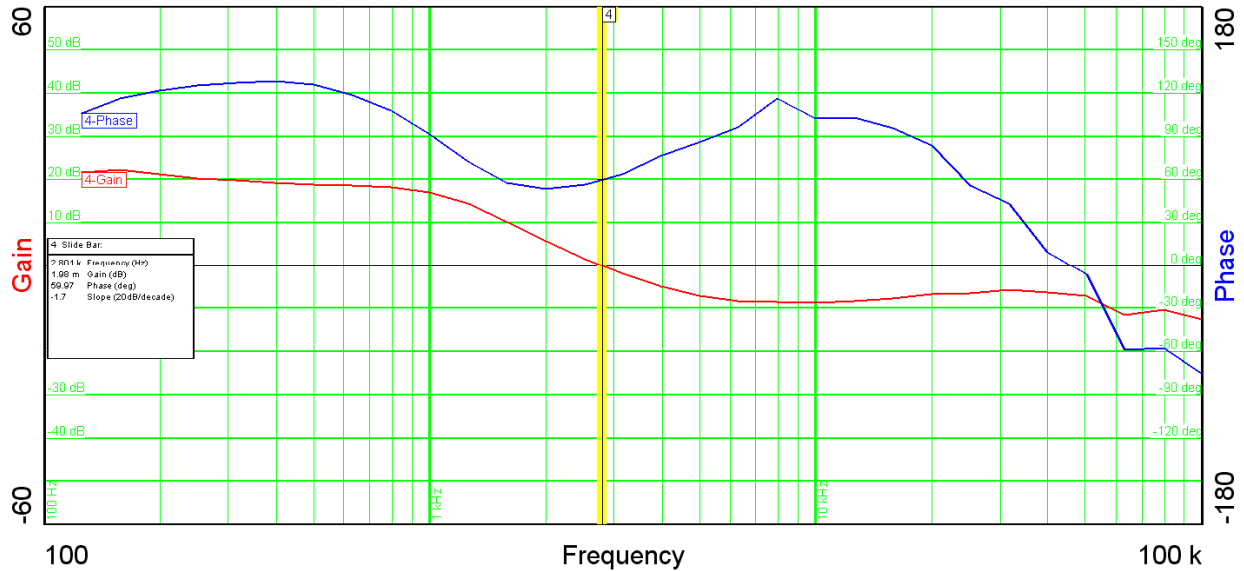
8 VSNEG Output Ripple Voltage

The VSNEG output ripple voltage is shown in the plot below. The battery voltage was set at 3.7V and the load was set to 0.1A.

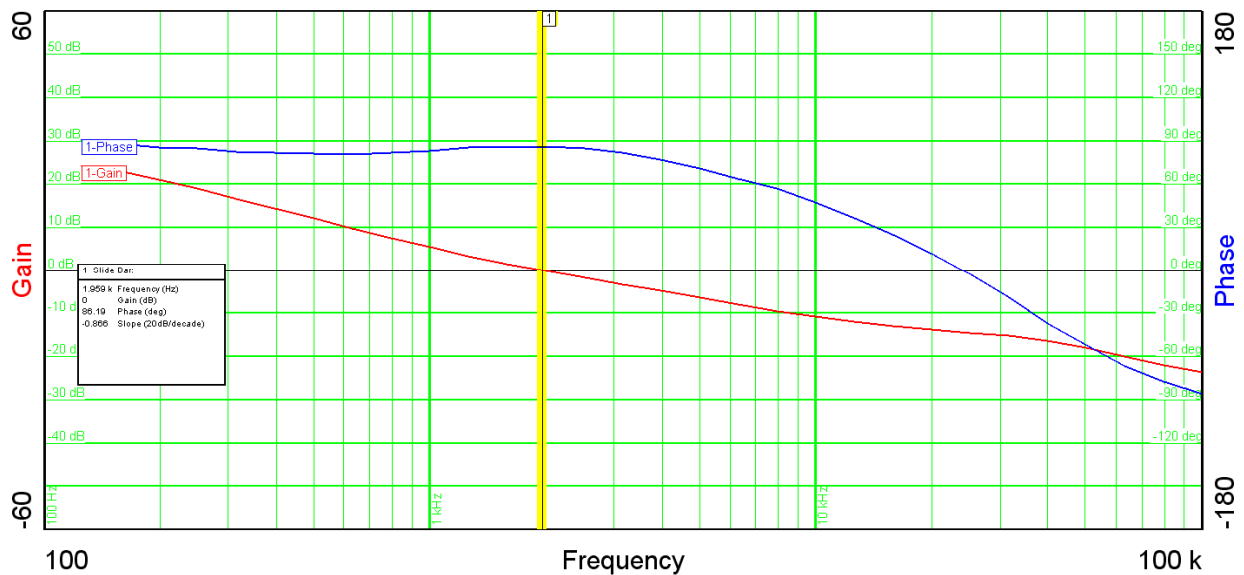


9 Loop Response

The image below shows the loop response of the VSPOS (set at 18V) converter measured with a 3.7V battery voltage, and a full load. Phase margin is 59.97 deg. and crossover frequency is 2.8 KHz.



The image below shows the loop response of the VSNEG (set at -18V) converter measured with a 3.7V battery voltage, and a full load. Phase margin is 86.19 deg. and crossover frequency is 1.96 KHz.



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