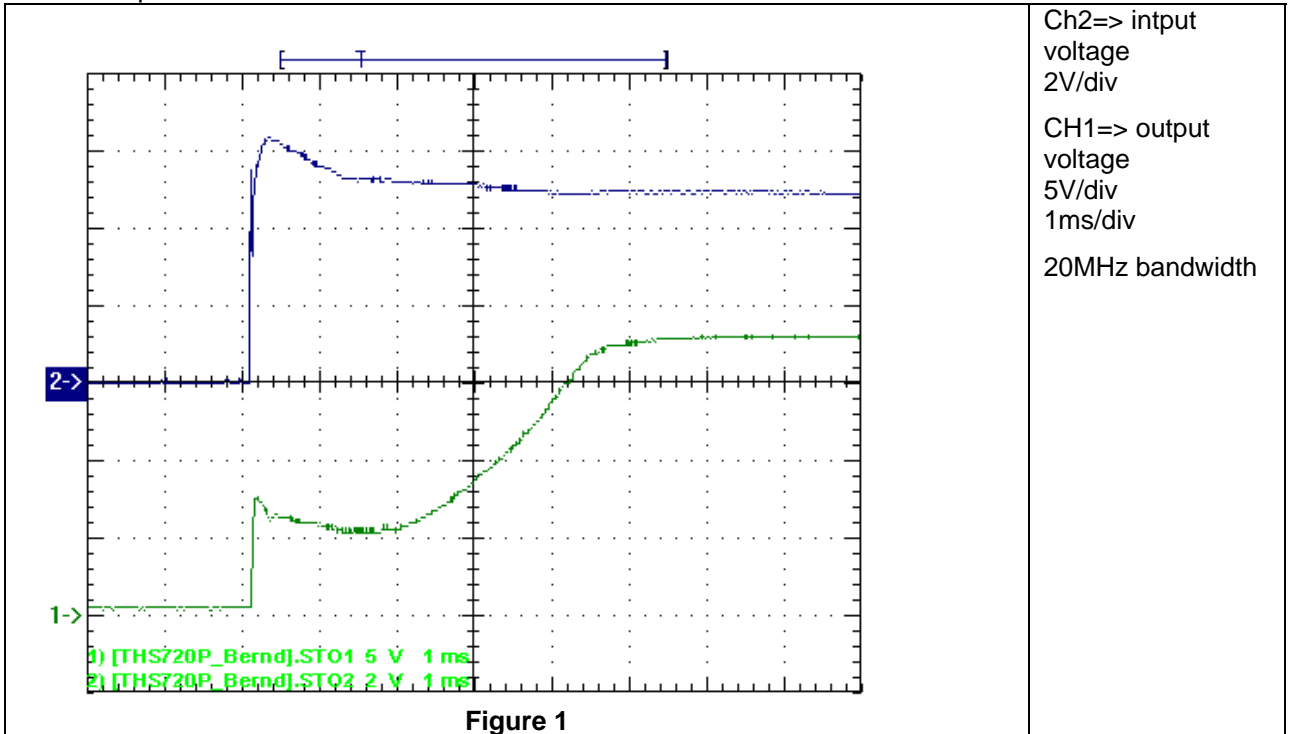


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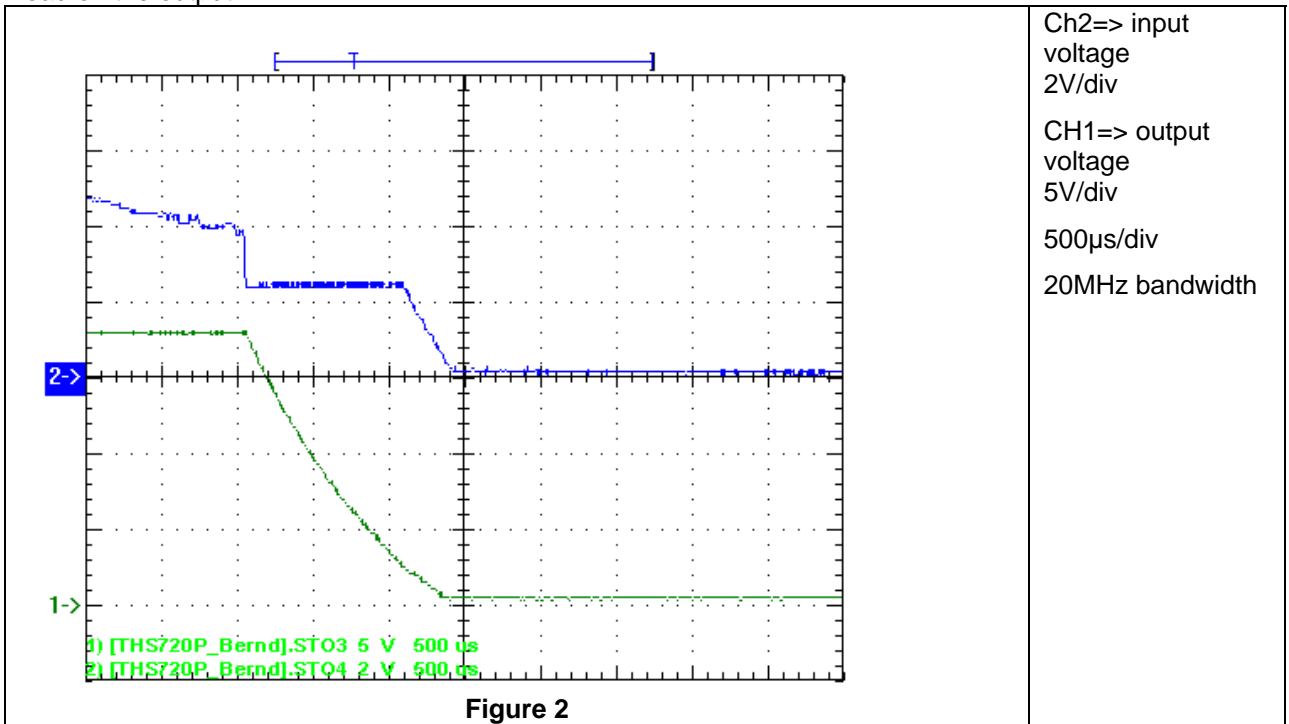
1. Startup

The startup waveform is shown in the Figure 1. The input voltage was set at ~5V, with 0.48A load on the output.



2. Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at ~5V, with 0.48A load on the output.



3. Efficiency

The efficiency is shown in the Figure 3 below.

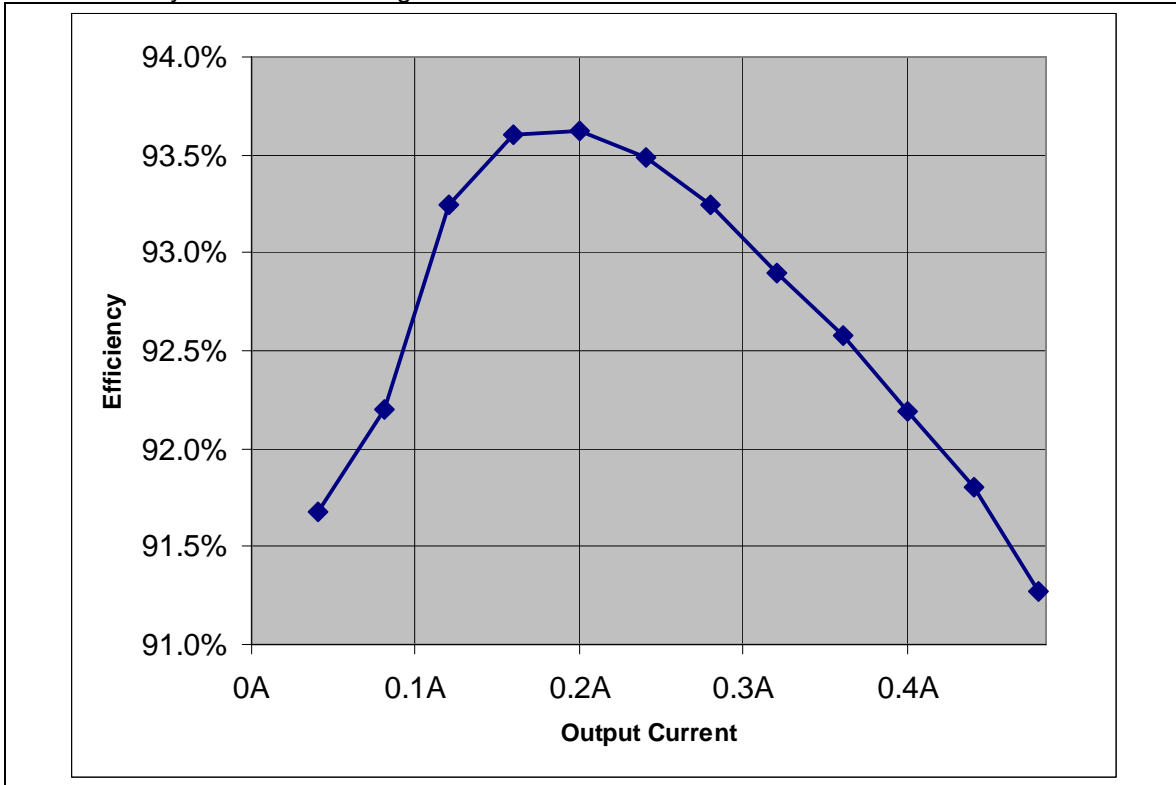


Figure 3

The corresponding values are shown in Table 1.

<i>V_{in}</i> (V)	<i>I_{in}</i> (A)	<i>V_{out}</i> (V)	<i>I_{out}</i> (A)	(measured)	<i>Pin</i> (W)	<i>P_{out}</i> (W)	<i>Eff</i>
5.0	0.159	18.041	0.04	0.0403	0.79	0.73	91.68%
5.0	0.315	18.044	0.08	0.0805	1.58	1.45	92.20%
5.0	0.467	18.044	0.12	0.1206	2.33	2.18	93.25%
5.0	0.617	18.046	0.16	0.1603	3.09	2.89	93.61%
5.0	0.772	18.047	0.2	0.2003	3.86	3.61	93.62%
5.0	0.928	18.048	0.24	0.2408	4.65	4.35	93.49%
5.0	1.085	18.049	0.28	0.2804	5.43	5.06	93.24%
5.0	1.243	18.051	0.32	0.3203	6.22	5.78	92.89%
5.0	1.406	18.052	0.36	0.3607	7.03	6.51	92.57%
5.0	1.566	18.053	0.4	0.4003	7.84	7.23	92.19%
5.0	1.730	18.055	0.44	0.4406	8.67	7.96	91.80%
5.0	1.899	18.058	0.48	0.4801	9.50	8.67	91.27%

Table 1

4 Load Regulation

The load regulation of the output is shown in the **Figure 4** below.

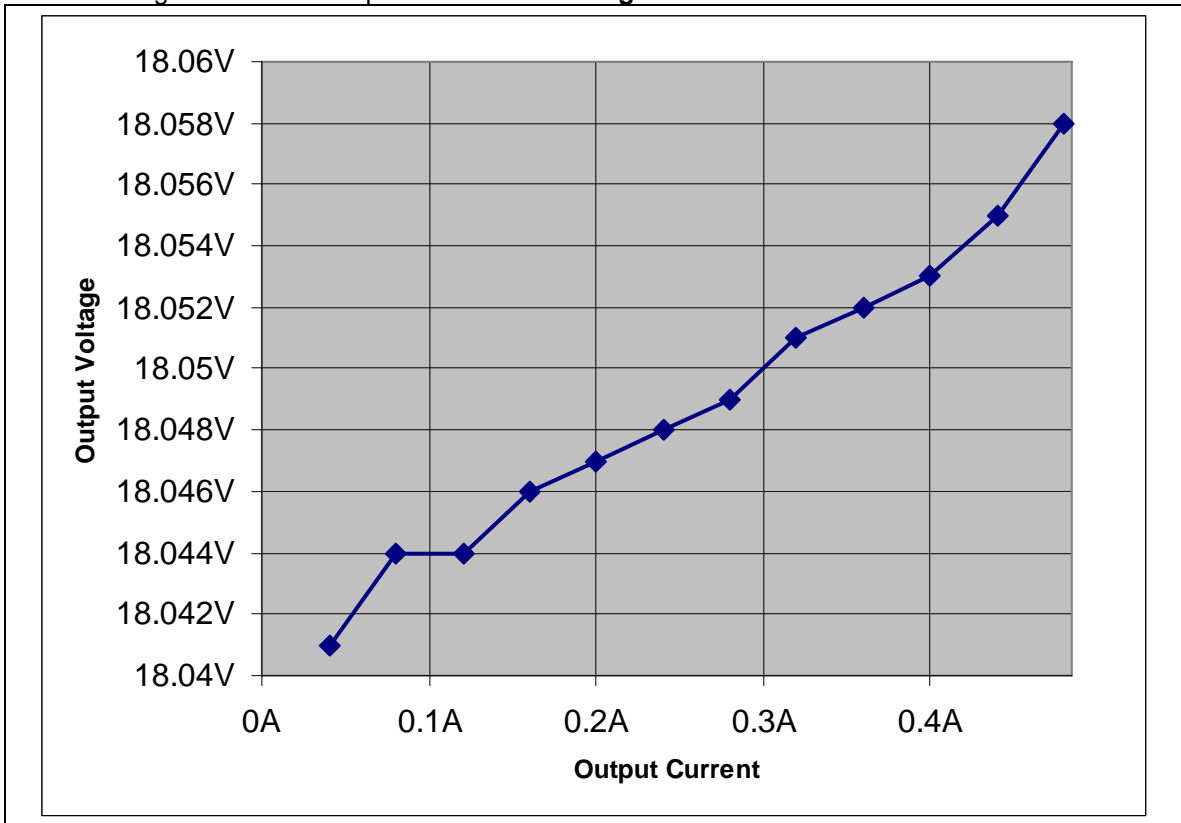
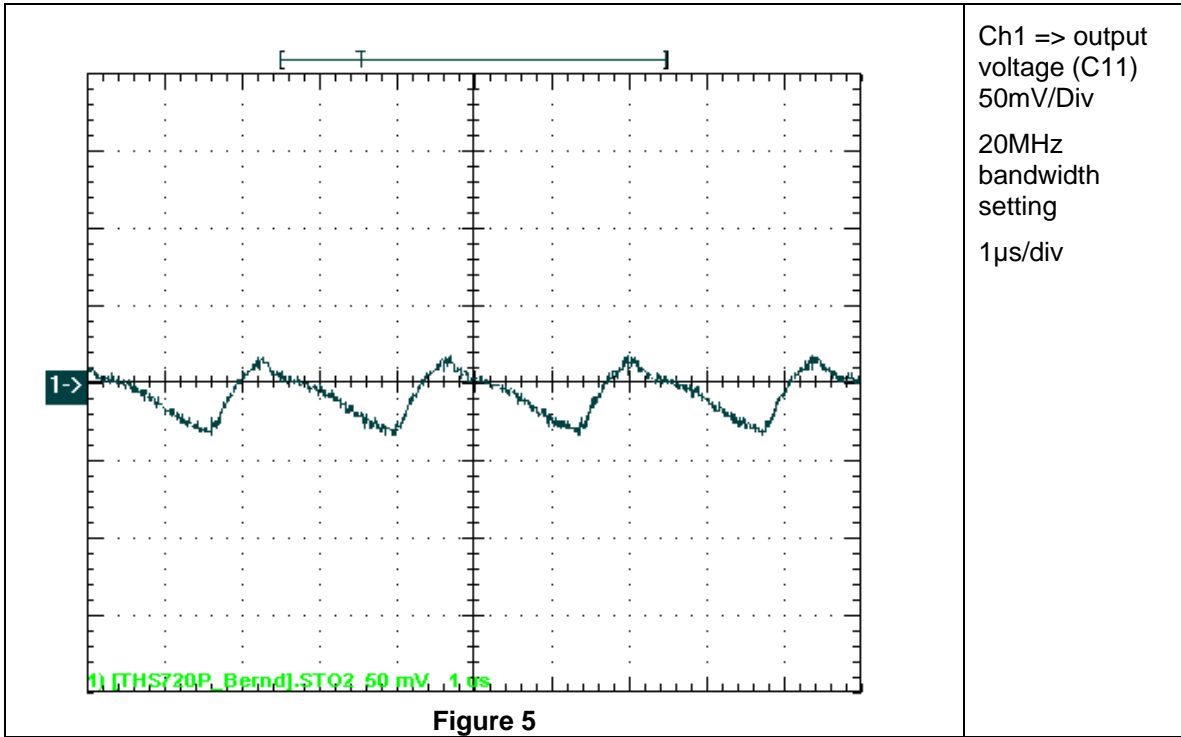


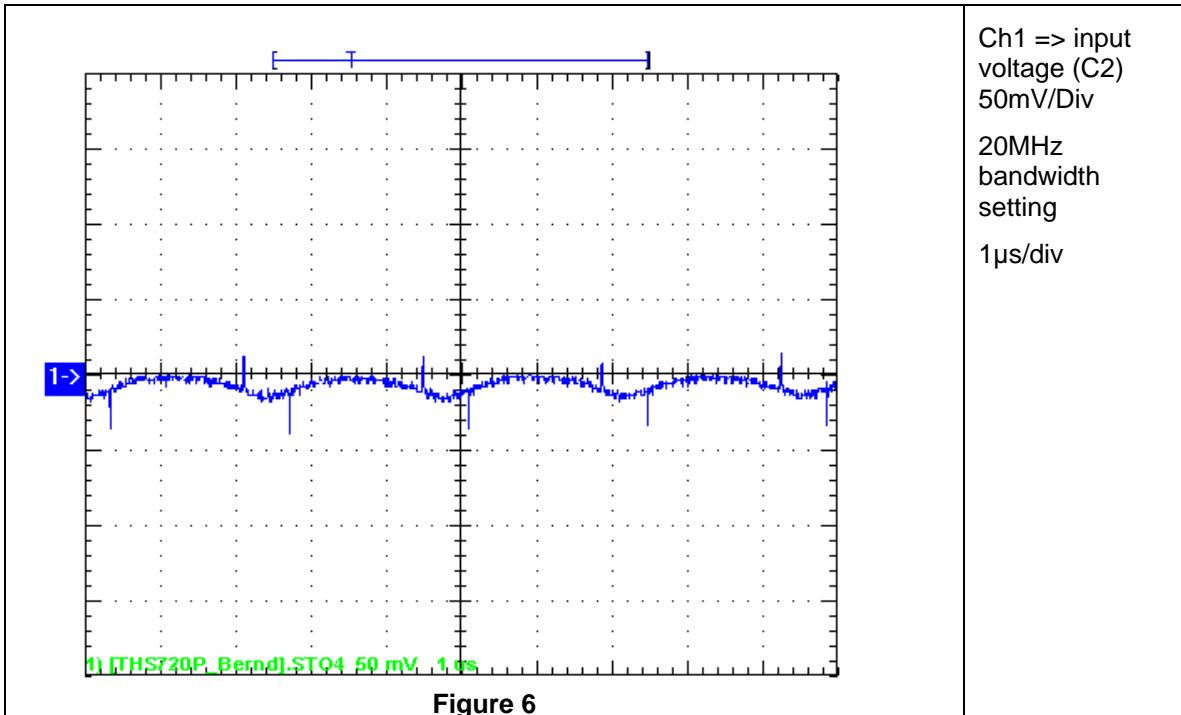
Figure 4

4. Ripple Voltage

The output ripple voltage is shown in Figure 5. The image was taken with a 0.48A load and ~5V at the input.

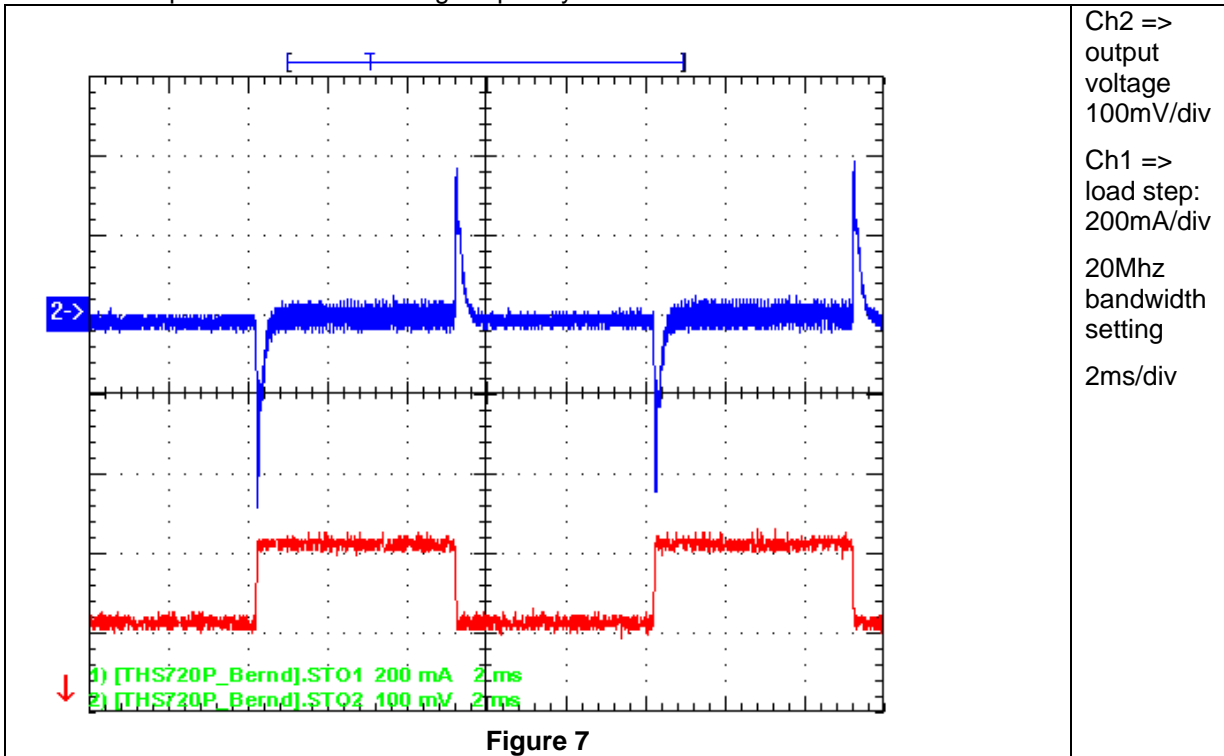


The input ripple voltage is shown in Figure 6. The image was taken with a 0.48A load and ~5V at the input.

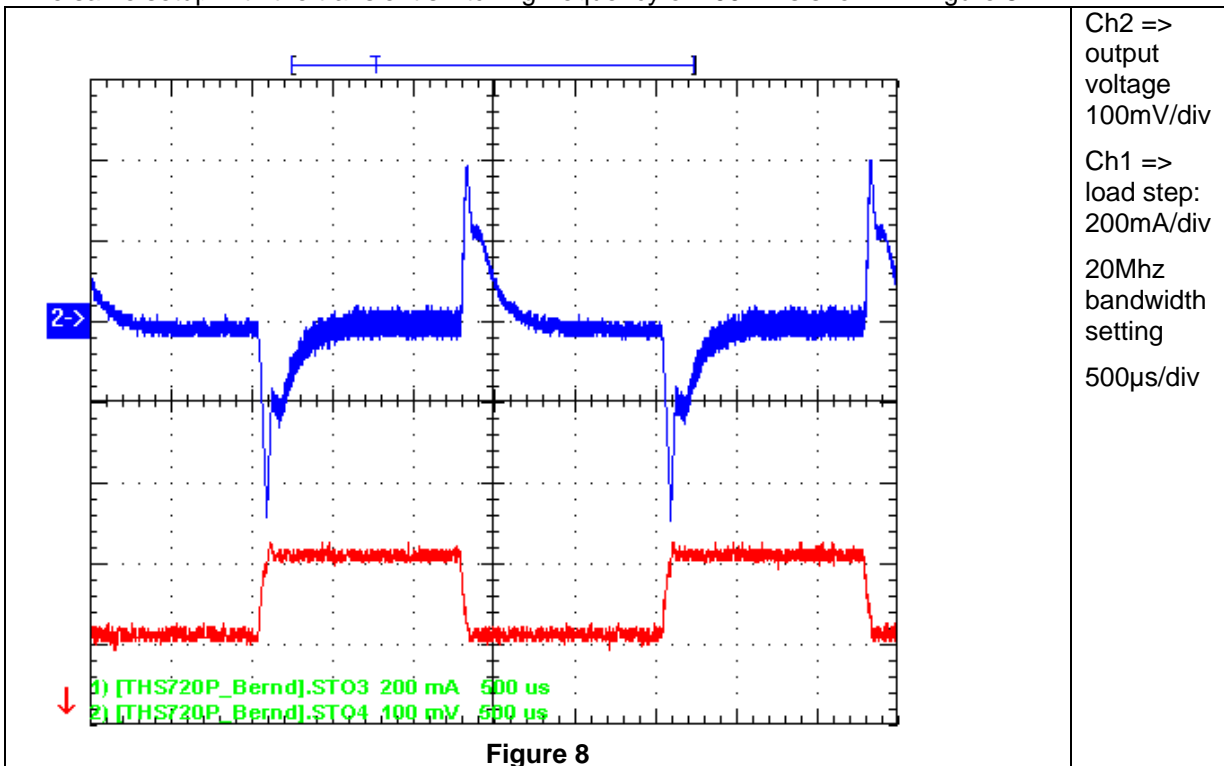


5. Load Transients

The Figure 7 shows the response to load transients. The load is switching from 0.2A to 0.4A with ~5V at the input. Transient switching frequency was set to 100Hz

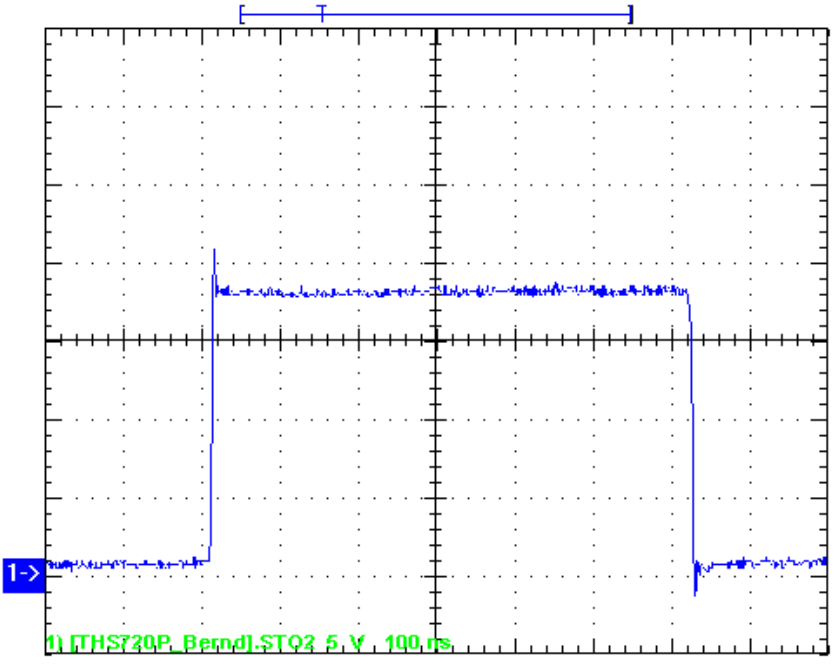
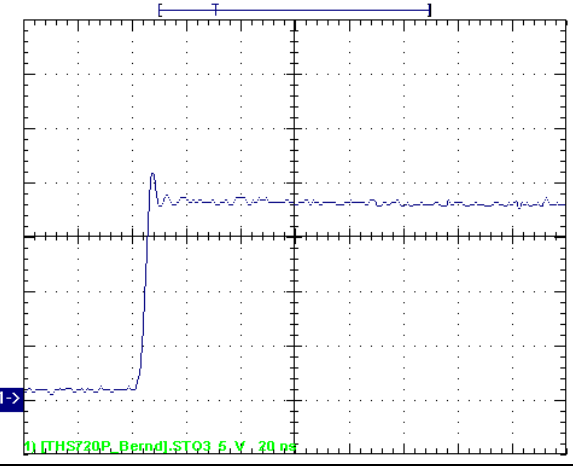
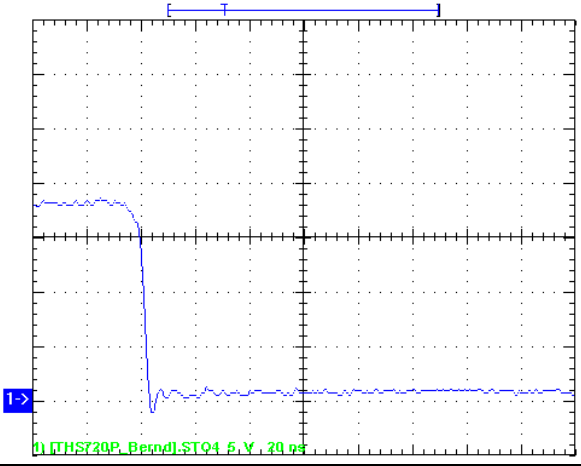


The same setup with the transient switching frequency of 400Hz is shown in Figure 8



6. Switch Node Waveform

With input voltage set to 12V result in the waveform shown in Figure 9 and Figure 10. Output current was set to 0.48A.

	<p>Ch1 => switch node 5V/div 100ns/div full bandwidth</p>	
<p>Figure 9</p>		
		<p>Ch1 => switchnode 5V/div 20ns/div full bandwidth</p>
<p>Figure 10</p>		

7. Control Loop Frequency Response

Figure 11 shows the control loop frequency response and in Table 2 are the corresponding values for gain and phase margin. The current were set to 0.4A.

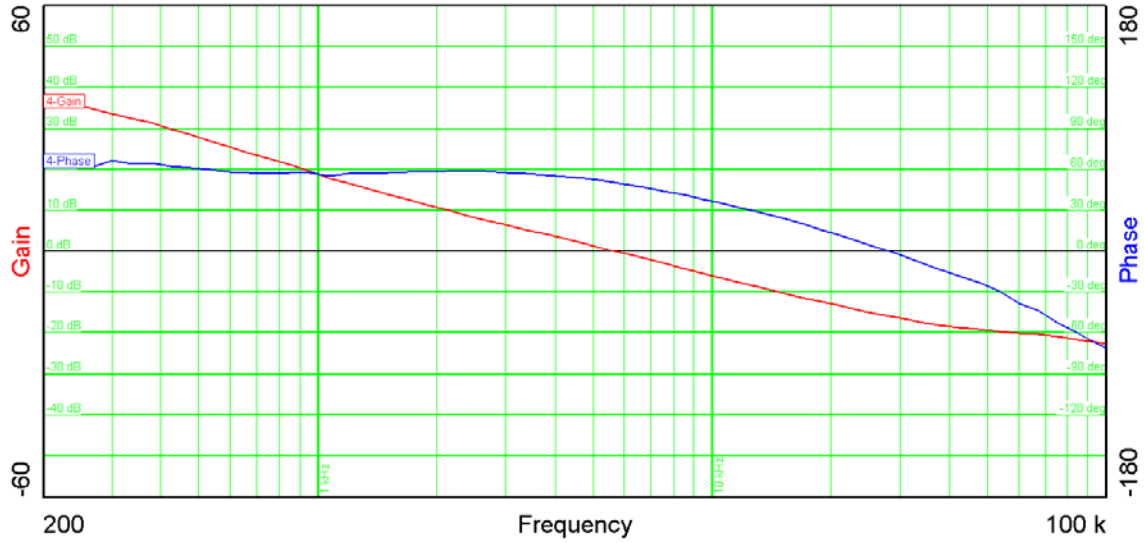


Figure 11

Bandwidth (kHz)	5.65
Phasemargin slope (20dB/decade)	-1.2
gain margin (dB) at frequency (kHz)	15.87
gain margin slope (20dB/decade)	-0.88

Table 2

8. Thermal Image

Figure 12 is the thermal image with a outputcurrent of 480mA.

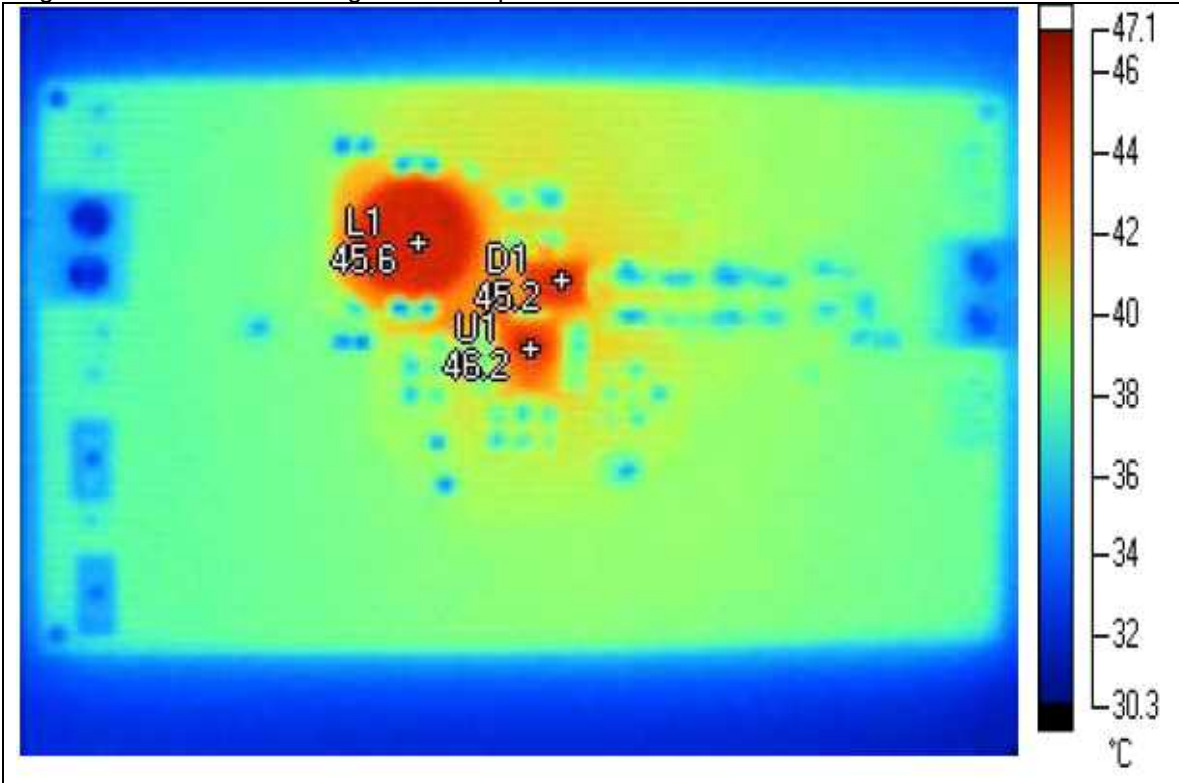


Figure 12

I

PMP4672RevA Test Results

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