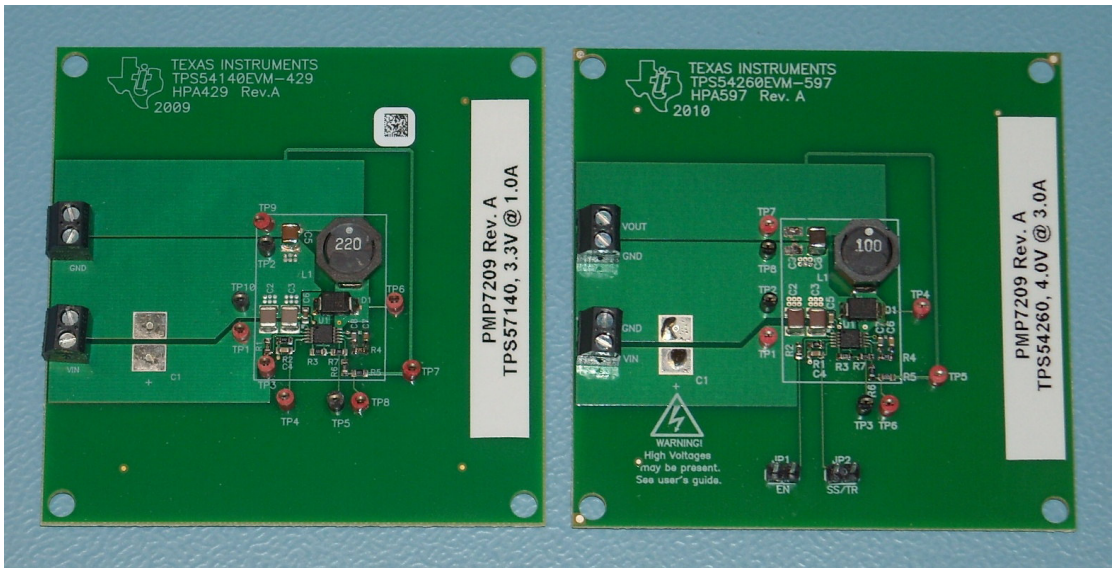
Two Bucks for Automotive Applications

- Input 6 .. 16V
- Switching Frequency 500 kHz
- Buck 1 TPS54260 4.0V @ 3.0A
- Buck 2 TPS57140 3.3V @ 1.0A
- Both bucks are optimized for a pulsed load and fast transient response



1 TPS54260 - 4.0V @ 3.0A

1.1 Startup

The startup waveform is shown in Figure 1. The input voltage is set at 12.0V, with no load on the 4.0V output.

Channel C1: **Input voltage**
2V/div, 2ms/div

Channel C2: **Output voltage**
1V/div, 2ms/div

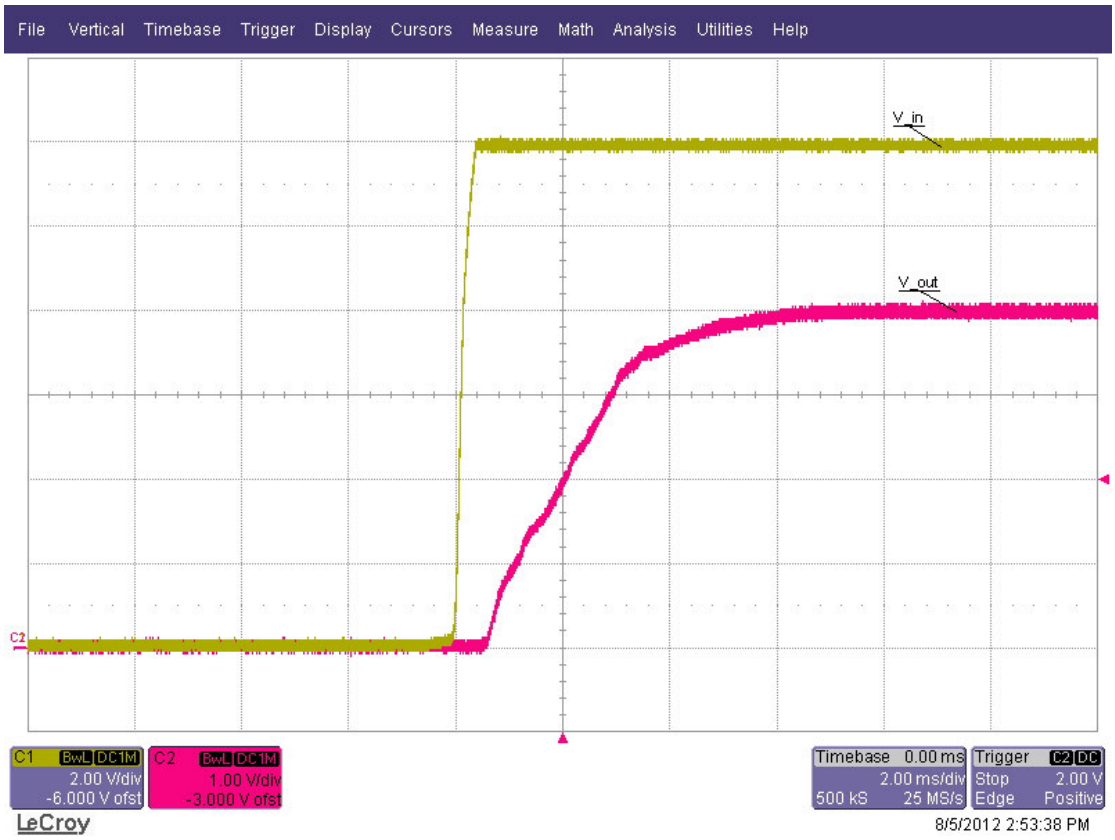


Figure 1

1.2 Shutdown

The shutdown waveform is shown in Figure 2. The input voltage is set at 12.0V with a 3.0A load on the 4.0V output.

Channel C1: **Input voltage**
2V/div, 100us/div

Channel C2: **Output voltage**
1V/div, 100us/div

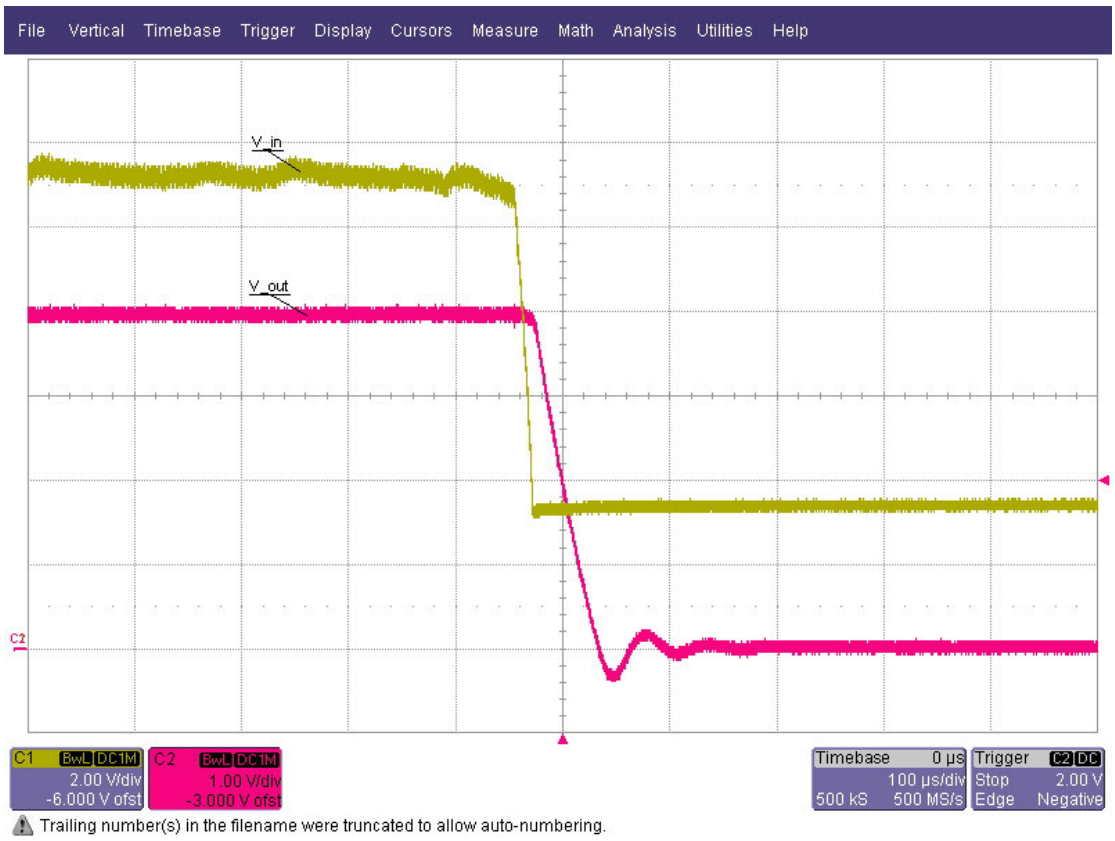


Figure 2

1.3 Efficiency

The efficiency is shown in Figure 3.

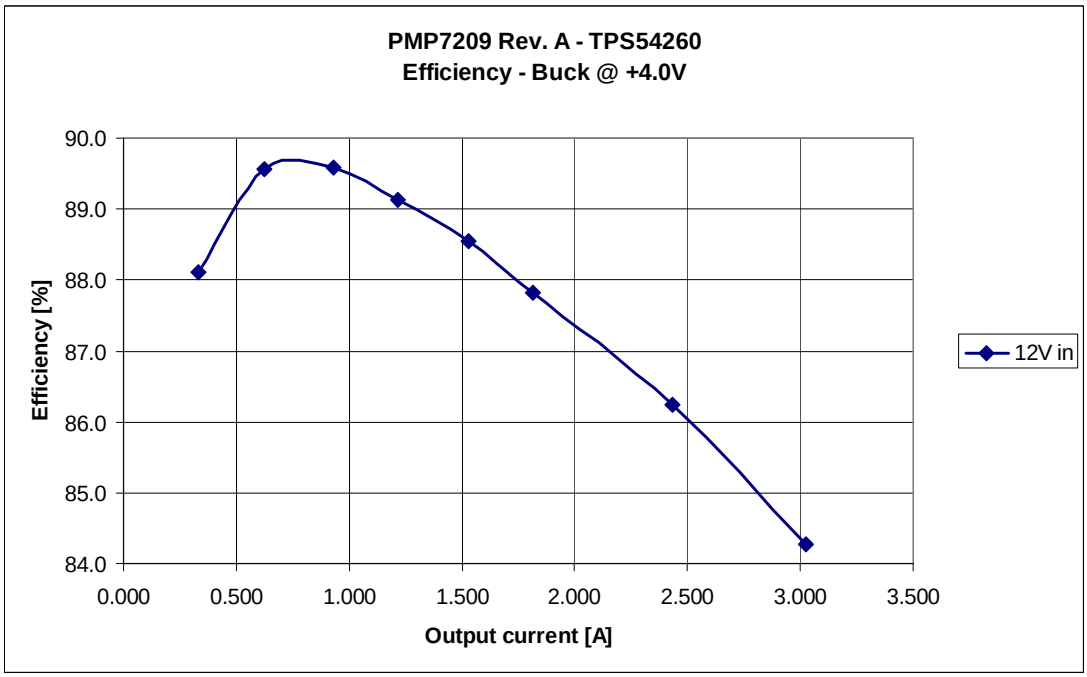


Figure 3

1.4 Load regulation

The load regulation of the 4.0V output is shown in Figure 4.

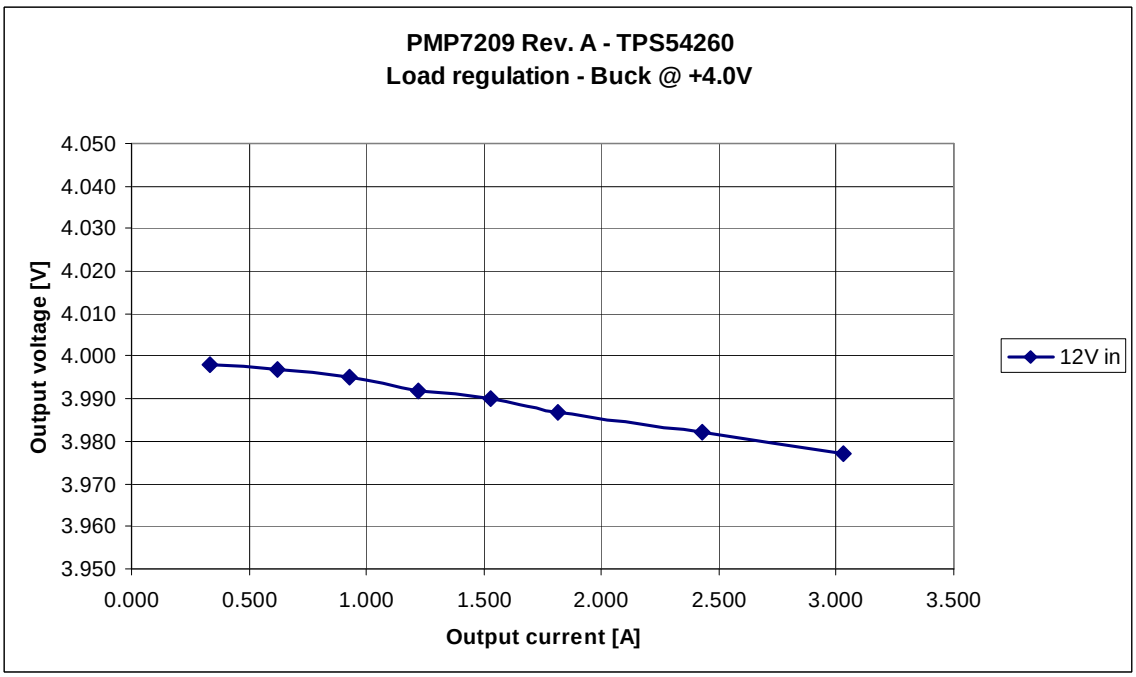


Figure 4

1.5 Output ripple voltage

The output ripple voltage at 4.0A load and 6, 12 and 16V input voltage is shown in Figure 5.

Channel M1: **Output voltage @ 6V input**, 5mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M2: **Output voltage @ 12V input**, 7mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M3: **Output voltage@ 16V input**, 9mV peak-peak
20mV/div, 5us/div, AC coupled

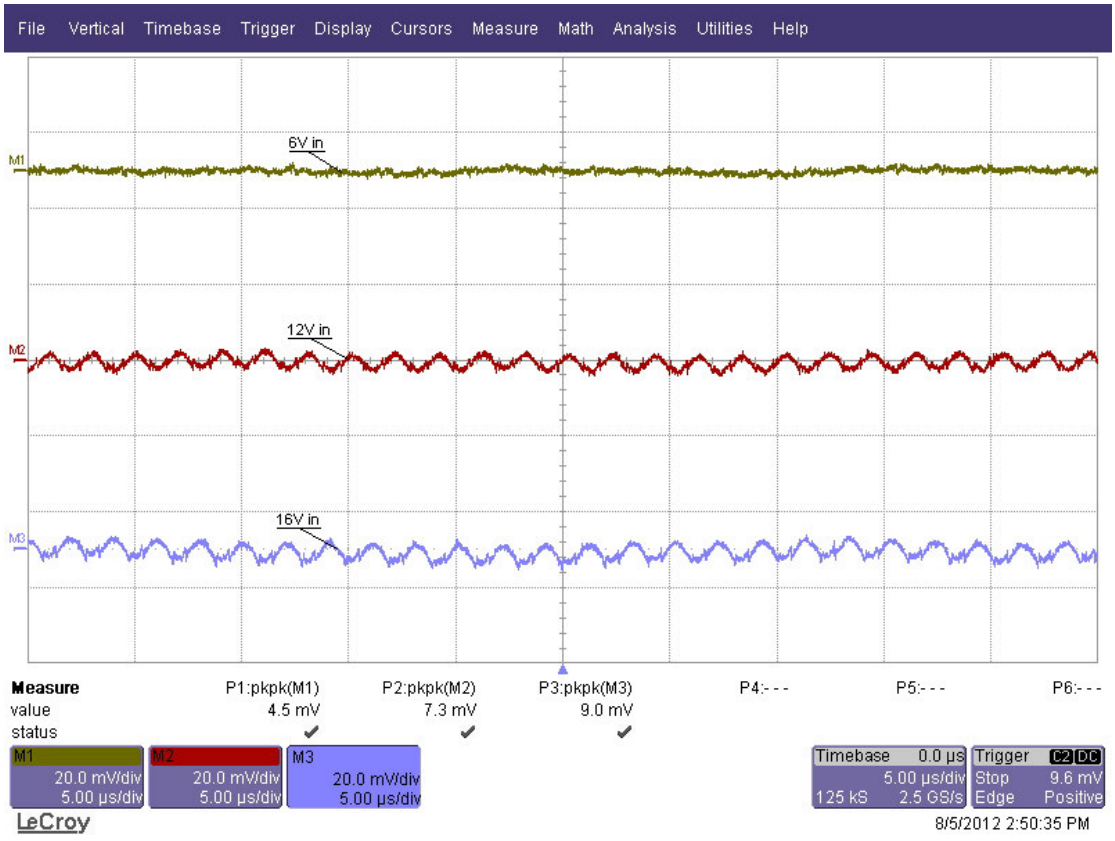


Figure 5

1.6 Load transients

The response to a load step and a load dump at an input voltage of 12.0V is shown in Figure 6 (1x 47uF output capacitance and optimized compensation) and Figure 7 (2x 47uF output capacitance and optimized compensation).

1.7 1x 47uF output capacitance (compensation optimized)

Channel C2: **Output voltage**, -392mV undershoot / 408mV overshoot
500mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.5A to 3.0A
1A/div, 1ms/div

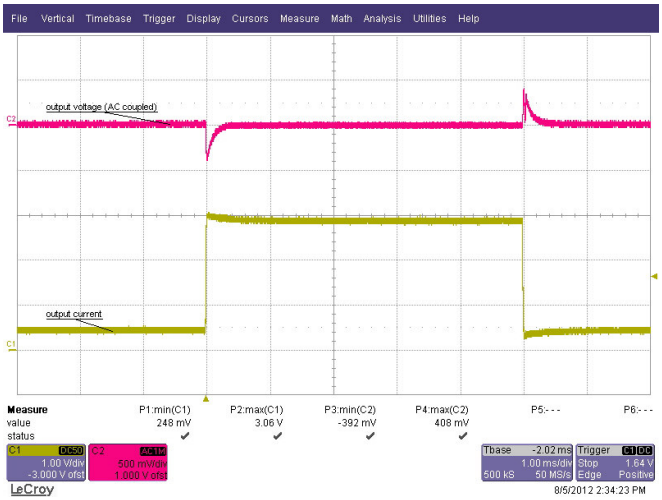


Figure 6

1.7.1 2x 47uF output capacitance (compensation optimized)

Channel C2: **Output voltage**, -202mV undershoot / 202mV overshoot
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.5A to 3.0A
1A/div, 1ms/div

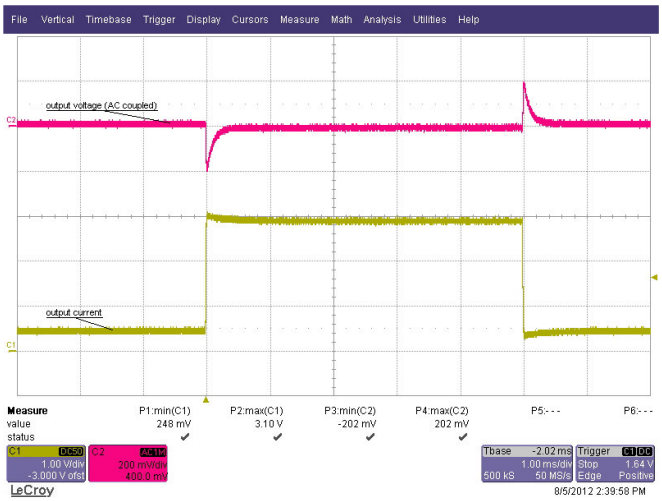


Figure 7

1.8 Frequency response

The frequency response with an input voltage of 6 and 16V and a load of 3A is shown in Figure 8 (1x 47uF output capacitance and optimized compensation) and Figure 9 (2x 47uF output capacitance and optimized compensation).

1.8.1 1x 47uF output capacitance (compensation optimized)

- 6V in 66 deg phase margin @ 22.1 kHz bandwidth, -19 dB gain margin
- 16V in 72 deg phase margin @ 23.9 kHz bandwidth, -19 dB gain margin

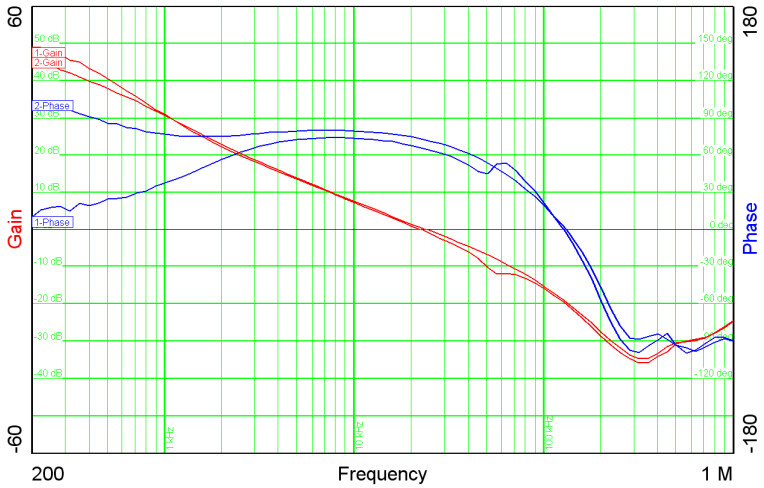


Figure 8

1.8.2 2x 47uF output capacitance (compensation optimized)

- 6V in 64 deg phase margin @ 22.2 kHz bandwidth, -22 dB gain margin
- 16V in 72 deg phase margin @ 23.9 kHz bandwidth, -20 dB gain margin

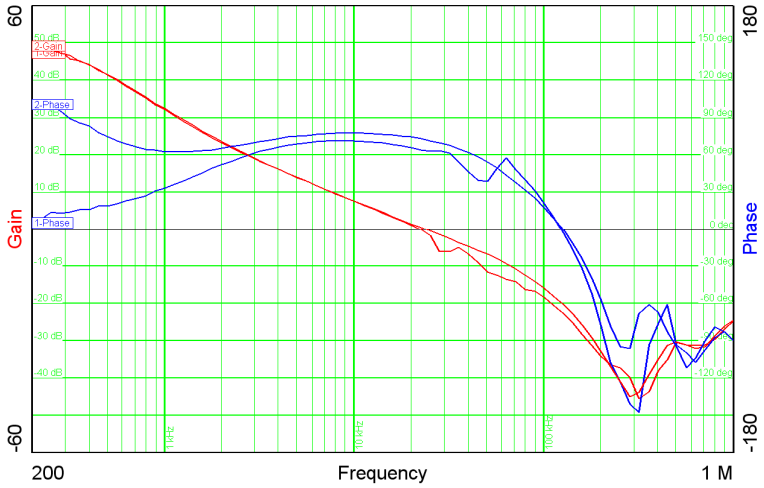


Figure 9

1.9 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 10. The image was captured with 16.0V input and a 3.0A load.

Channel C2: **Drain-source voltage**, -1.7V minimum voltage, 16.5V maximum voltage 5V/div, 1us/div

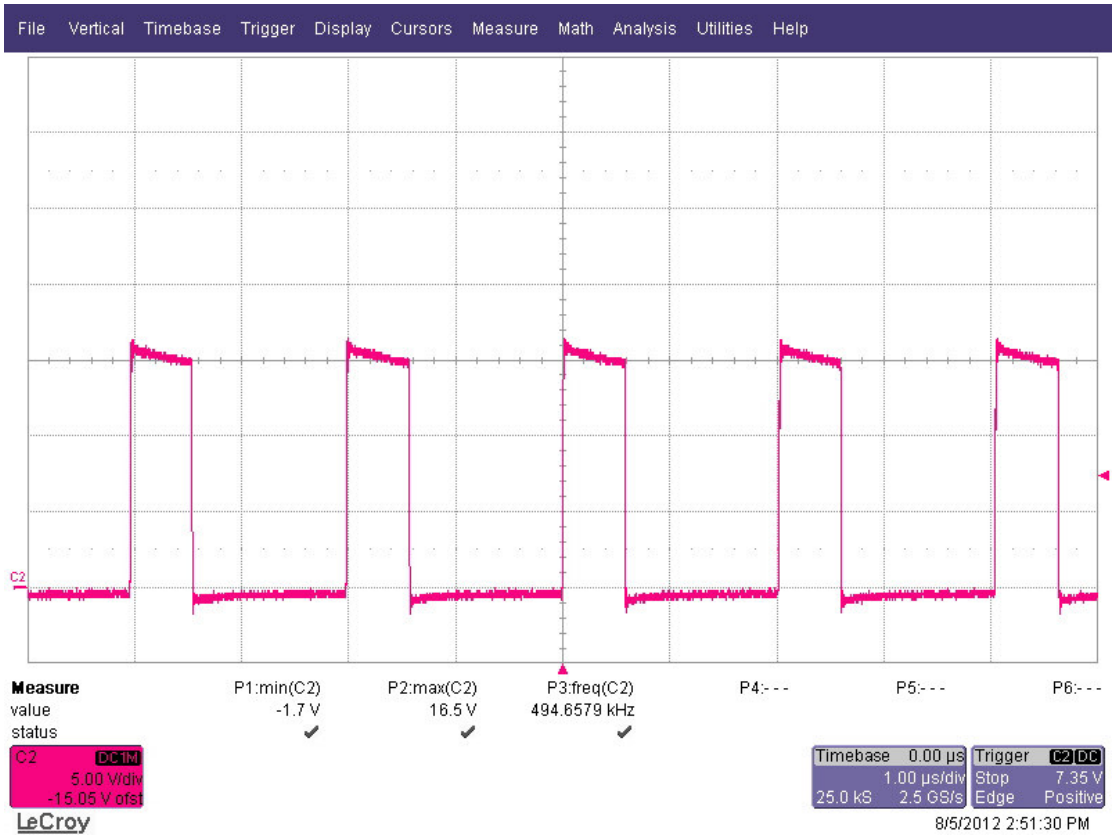


Figure 10

1.10 Thermal measurement

The thermal image (Figure 11) shows the circuit at an ambient temperature of 21 °C with an input voltage of 16.0V and a load of 3.0A.

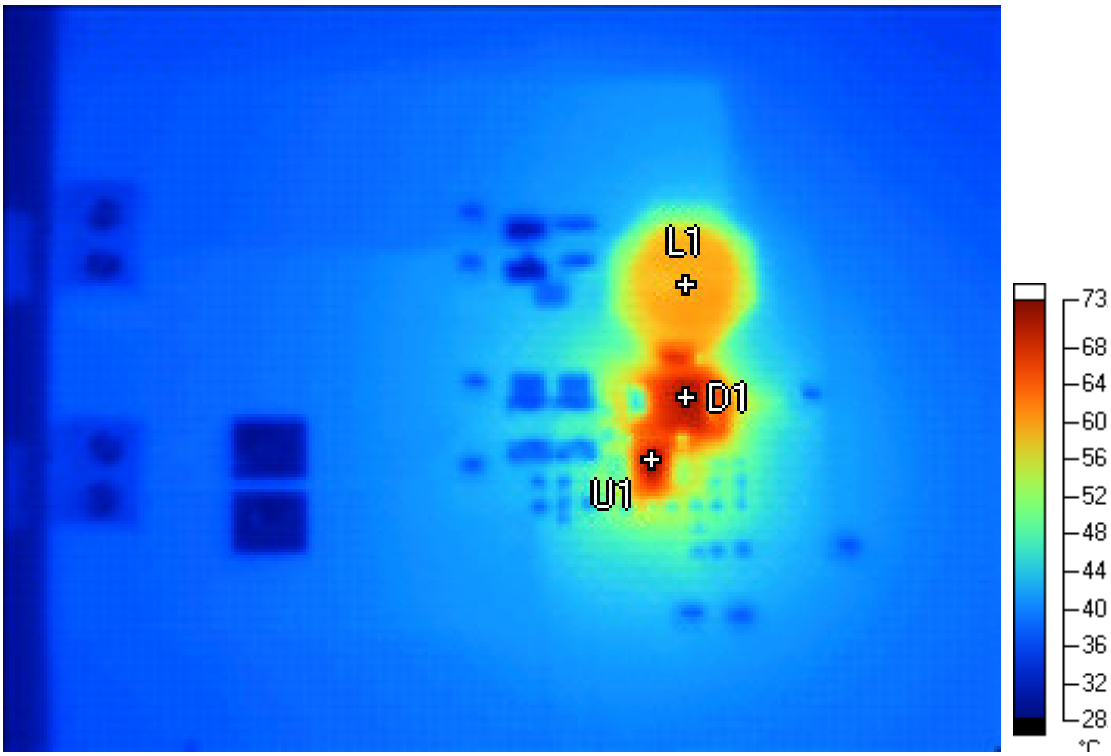


Figure 11

Markers

Label	Temperature	Emissivity	Background
L1	59.1 °C	0.95	21.0 °C
D1	70.8 °C	0.95	21.0 °C
U1	70.8 °C	0.95	21.0 °C

2 TPS57140 - 3.3V @ 1.0A

2.1 Startup

The startup waveform is shown in Figure 12. The input voltage is set at 12.0V, with no load on the 3.3V output.

Channel C1: **Input voltage**
2V/div, 2ms/div

Channel C2: **Output voltage**
1V/div, 2ms/div

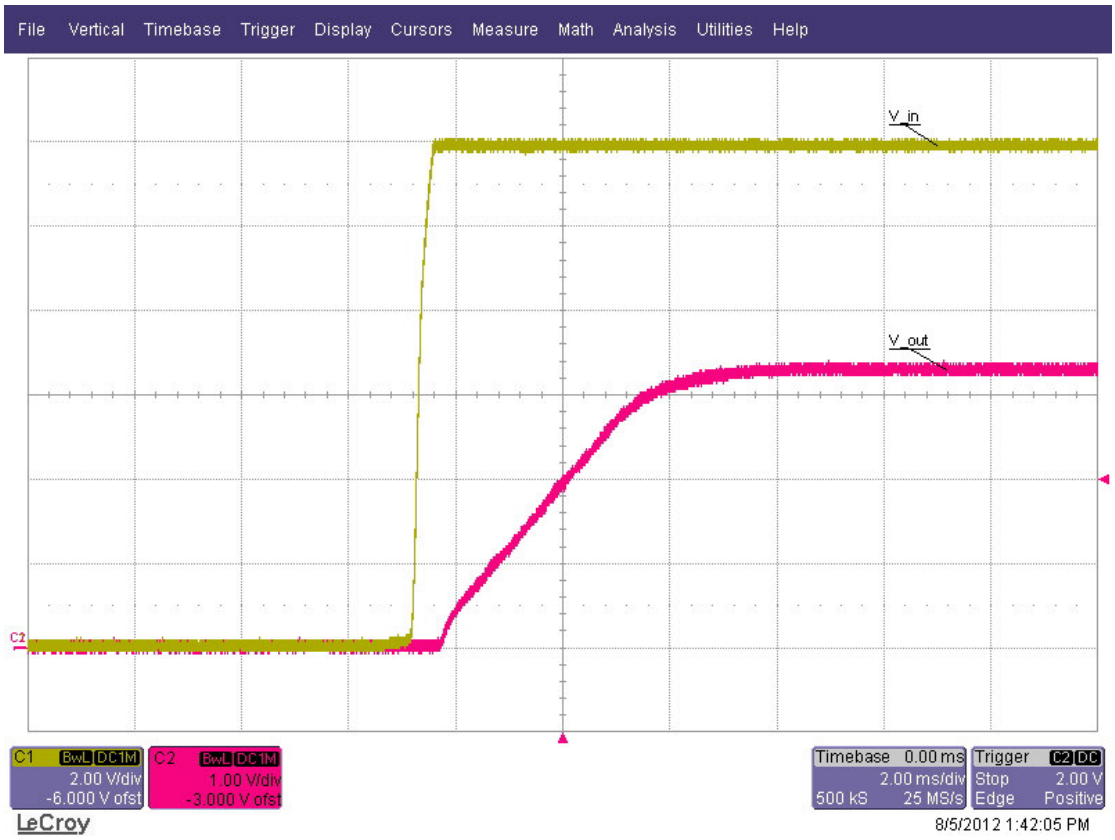


Figure 12

2.2 Shutdown

The shutdown waveform is shown in Figure 13. The input voltage is set at 12.0V with a 1.0A load on the 3.3V output.

Channel C1: **Input voltage**
2V/div, 100us/div

Channel C2: **Output voltage**
1V/div, 100us/div

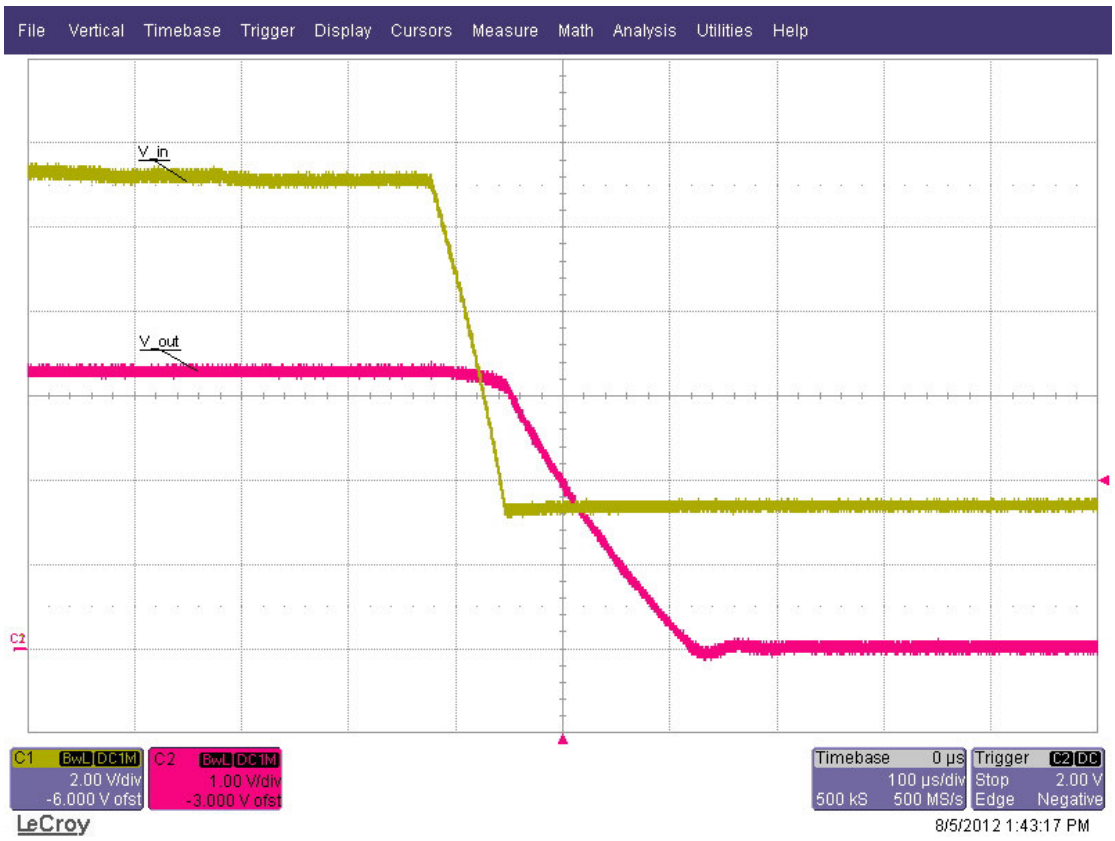


Figure 13

2.3 Efficiency

The efficiency is shown in Figure 14.

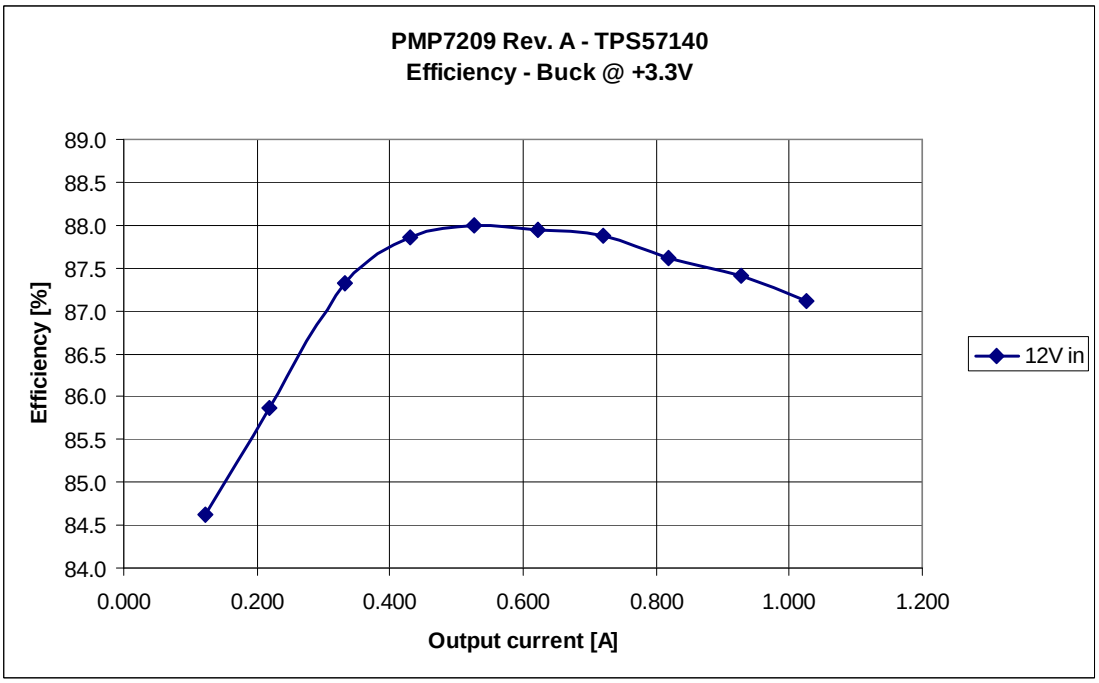


Figure 14

2.4 Load regulation

The load regulation of the 3.3V output is shown in Figure 15.

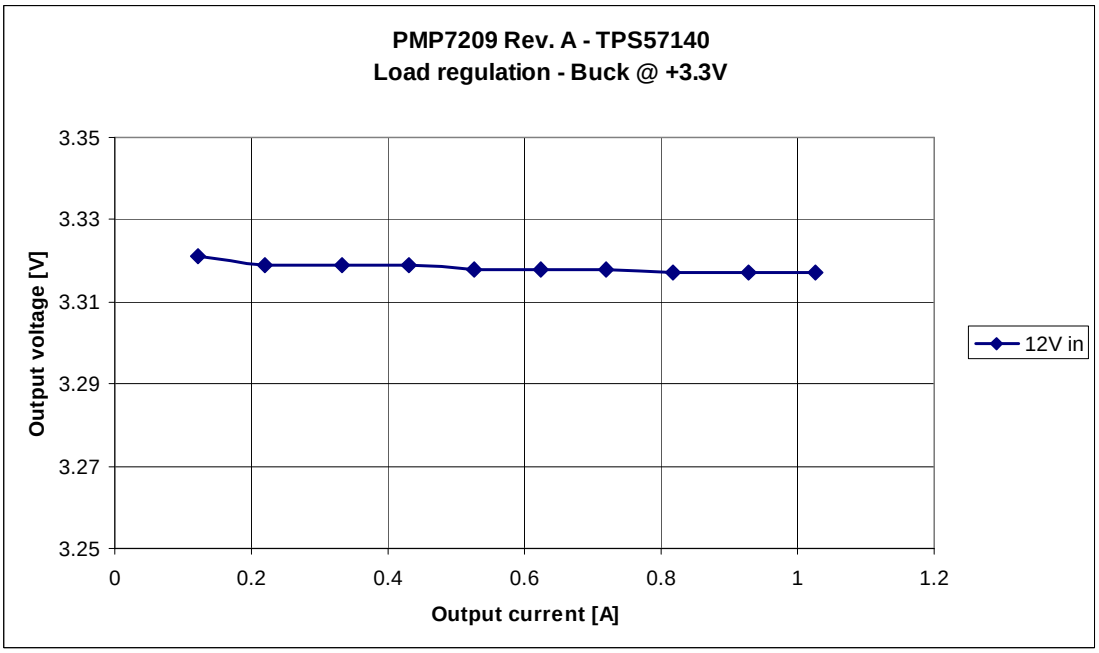


Figure 15

2.5 Output ripple voltage

The output ripple voltage at 1.0A load and 6, 12 and 16V input voltage is shown in Figure 16.

Channel M1: **Output voltage @ 6V input**, 6mV peak-peak
20mV/div, 5us/div, AC coupled

Channel M2: **Output voltage @ 12V input**, 7mV peak-peak
10mV/div, 5us/div, AC coupled

Channel M3: **Output voltage@ 16V input**, 7mV peak-peak
20mV/div, 5us/div, AC coupled

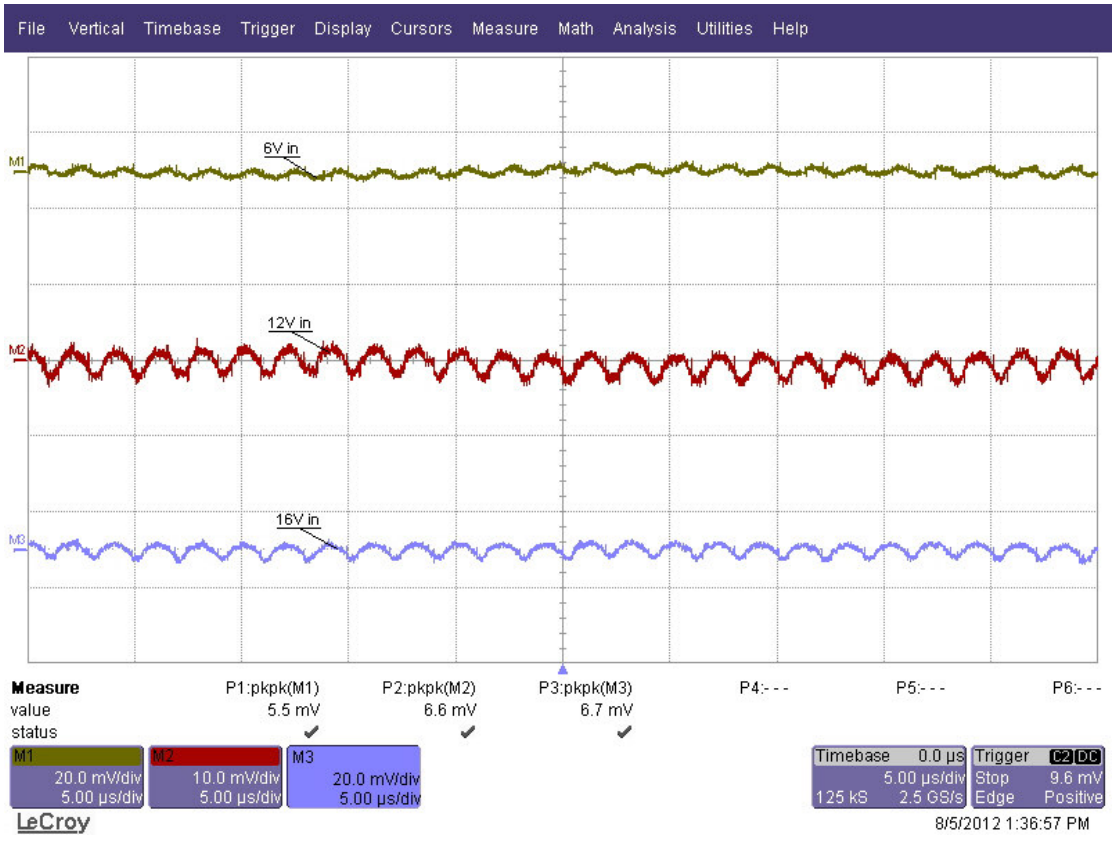


Figure 16

2.6 Load transients

The response to a load step and a load dump at an input voltage of 12.0V is shown in Figure 17 (1x 47uF output capacitance and optimized compensation) and Figure 18 (2x 47uF output capacitance and optimized compensation).

2.7 1x 47uF output capacitance (compensation optimized)

Channel C2: **Output voltage**, -240mV undershoot / 214mV overshoot
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.1A to 1.0A
500mA/div, 1ms/div

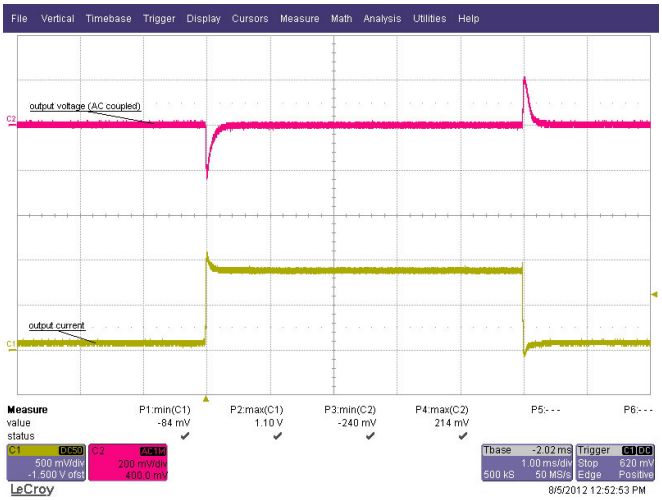


Figure 17

2.7.1 2x 47uF output capacitance (compensation optimized)

Channel C2: **Output voltage**, -131mV undershoot / 118mV overshoot
200mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.1A to 1.0A
500mA/div, 1ms/div

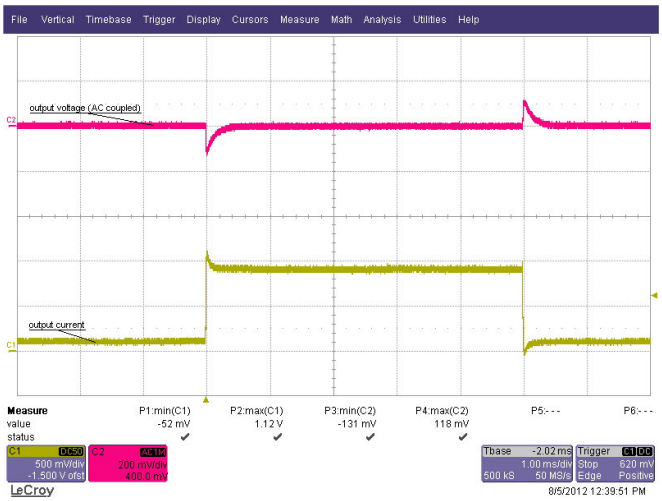


Figure 18

2.8 Frequency response

The frequency response with an input voltage of 6 and 16V and a load of 1A is shown in Figure 19 (1x 47uF output capacitance and optimized compensation) and Figure 20 (2x 47uF output capacitance and optimized compensation).

2.8.1 1x 47uF output capacitance (compensation optimized)

- 6V in 52 deg phase margin @ 18.1 kHz bandwidth, -20 dB gain margin
- 16V in 65 deg phase margin @ 21.6 kHz bandwidth, -18 dB gain margin

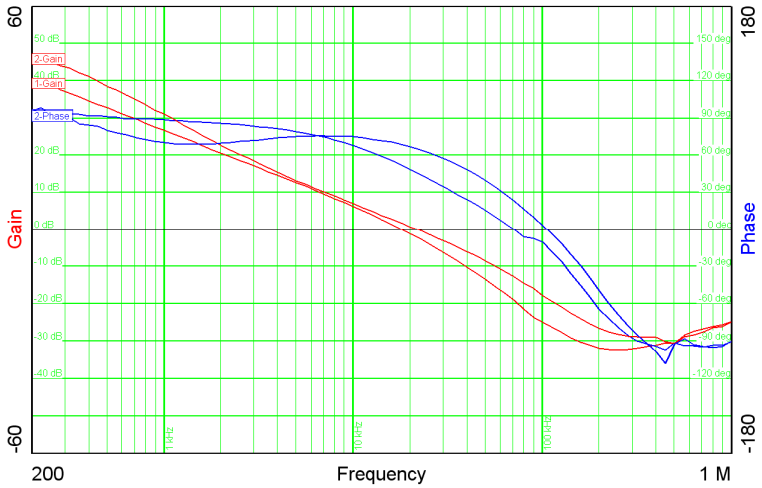


Figure 19

2.8.2 2x 47uF output capacitance (compensation optimized)

- 6V in 51 deg phase margin @ 19.2 kHz bandwidth, -17 dB gain margin
- 16V in 64 deg phase margin @ 22.8 kHz bandwidth, -16 dB gain margin

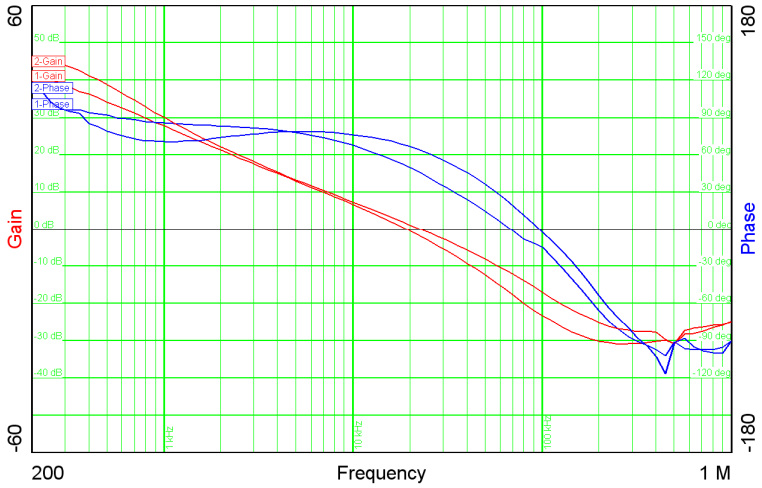


Figure 20

2.9 Miscellaneous waveforms

The drain-source voltage on the switching node is shown in Figure 21. The image was captured with 16.0V input and a 1.0A load.

Channel C2: **Drain-source voltage**, -1.1V minimum voltage, 18.2V maximum voltage 5V/div, 1us/div

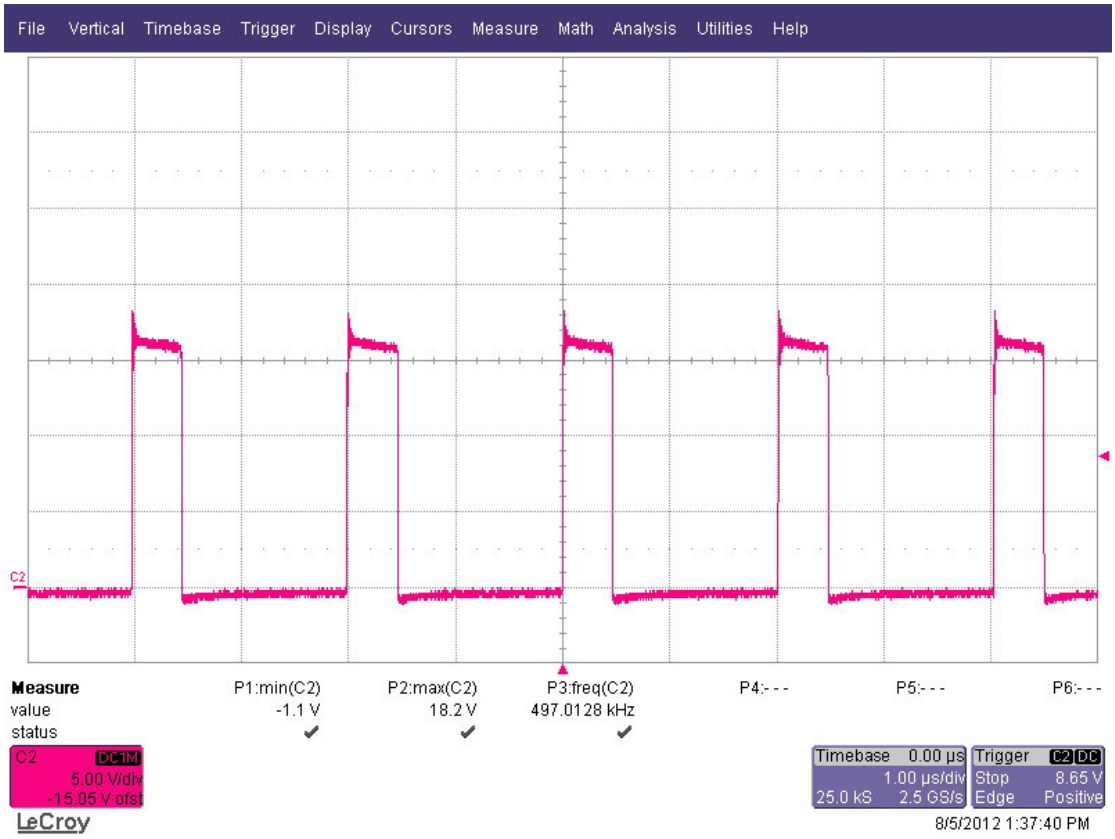


Figure 21

2.10 Thermal measurement

The thermal image (Figure 22) shows the circuit at an ambient temperature of 21 °C with an input voltage of 16.0V and a load of 1.0A.

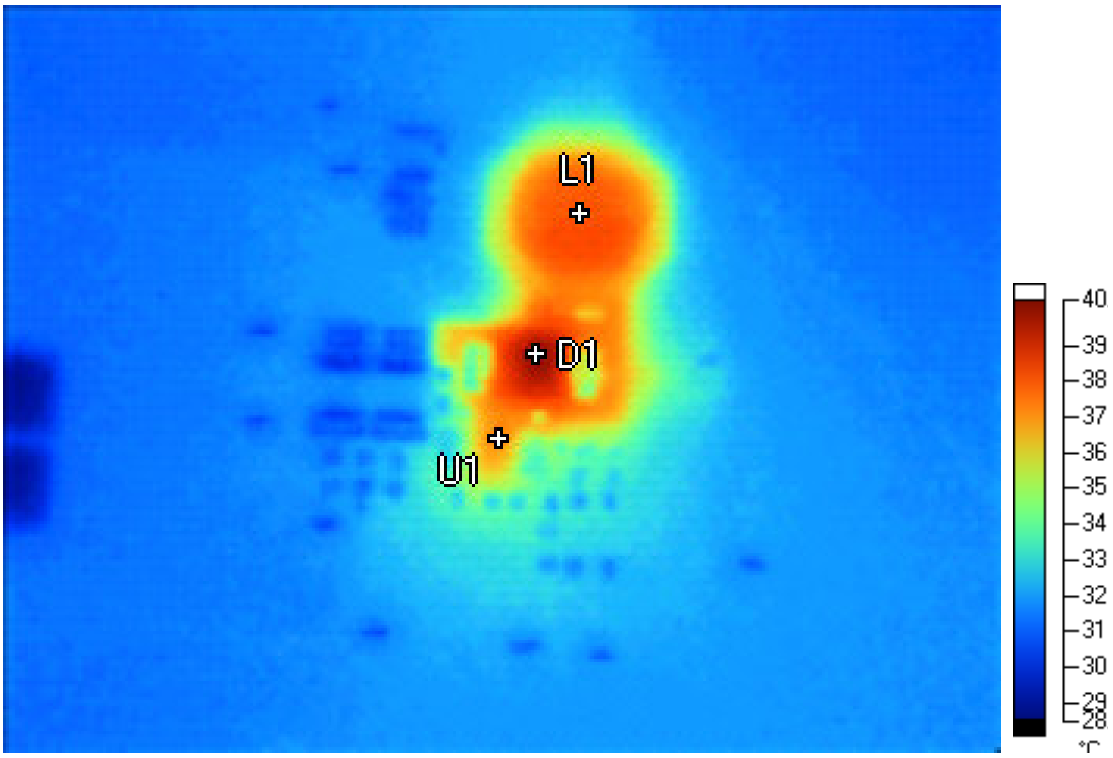


Figure 22

Markers

Label	Temperature	Emissivity	Background
L1	38.4 °C	0.95	21.0 °C
D1	40.0 °C	0.95	21.0 °C
U1	37.2 °C	0.95	21.0 °C

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