User's Guide
SLVU972 – September 2013

Evaluation Module for the TPS54340-Q1 Step-Down Converter

This user's guide contains information for the TPS54340-Q1EVM-593 evaluation module (PWR593) including the performance specifications, schematic, and the bill of materials.

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Eco-mode is a trademark of Texas Instruments.

1 Introduction

This user's guide contains background information for the TPS54340-Q1 as well as support documentation for the TPS54340-Q1EVM-593 evaluation module (PWR593). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54340-Q1EVM-593.

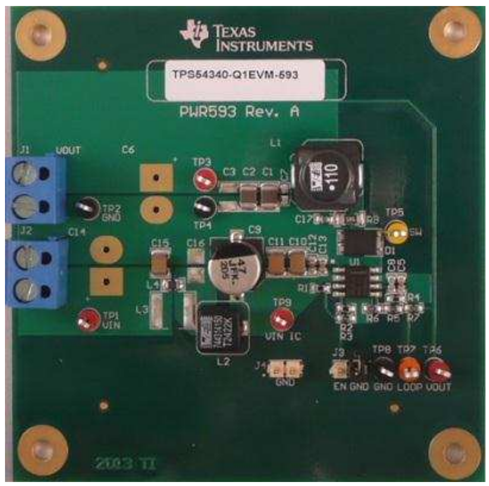


Figure 1. TPS54340-Q1EVM-593 Board

1.1 Background

The TPS54340-Q1 DC-DC converter is designed to provide up to a 3.5-A output from an input voltage source of 4.5 V to 42 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board (PCB) areas that may be achieved when designing with the TPS54340-Q1 regulator. The switching frequency is externally set at a nominal 400 kHz. This frequency was chosen to help with Electromagnetic Compatibility (EMC) by keeping the fundamental frequency out of the typical medium wave (MW) frequency range. The high-side MOSFET is incorporated inside the TPS54340-Q1 package along with the gate-drive circuitry. The compensation components are external to the integrated circuit (IC), and an external resistor divider allows for an adjustable output voltage. Additionally, the TPS54340-Q1 provides an adjustable undervoltage lockout with hysteresis through an external resistor divider. Lastly, the TPS54340-Q1EVM-593 includes additional input filtering and a snubber to reduce emissions. The absolute maximum input voltage for the TPS54340-Q1EVM-593 is 42 V.

Table 1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54340-Q1EVM-593	V_{IN} = 7.0 V to 42 V	I_{OUT} = 0 A to 3.5 A

1.2 Performance Specification Summary

A summary of the TPS54340-Q1EVM-593 (EVM) performance specifications is provided in Table 2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 5.0 V, unless otherwise specified. This EVM is designed and tested for V_{IN} = 7.0 V to 42 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 2. TPS54340-Q1EVM-593 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} voltage range			7	12	42	V
Output voltage set point				5.0		V
Output current range	V_{IN} = 7 V to 42 V		0		3.5	A
Line regulation	I_{OUT} = 3.5 A, V_{IN} = 7 V to 42 V			±0.02%		
Load regulation	V_{IN} = 12 V, I_{OUT} = 0.001 A to 3.5 A			±0.2%		
Load transient response	I_{OUT} = 0.8 A to 2.6 A	Voltage change		250		mV
		Recovery time		200		µs
	I_{OUT} = 2.6 A to 0.8 A	Voltage change		250		mV
		Recovery time		300		µs
Loop bandwidth	V_{IN} = 12 V, I_{OUT} = 3.5 A			13		kHz
Phase margin	V_{IN} = 12 V, I_{OUT} = 3.5 A			75		°
Input voltage ripple	I_{OUT} = 3.5 A, 20 MHz BWL			<10		mVpp
Output voltage ripple	I_{OUT} = 3.5 A			10		mVpp
Output rise time				2.6		ms
Operating frequency				400		kHz
Peak efficiency	TPS54340-Q1EVM-593, V_{IN} = 12 V, I_{OUT} = 1.1 A			91.7		%
DCM threshold	V_{IN} = 12 V			17		mA
Pulse skipping threshold	V_{IN} = 12 V			350		mA
No load input current	V_{IN} = 12 V			280		µA
UVLO start threshold				6.5		V
UVLO stop threshold				5.0		V

1.3 Schematic

Figure 2 is the schematic for the EVM.

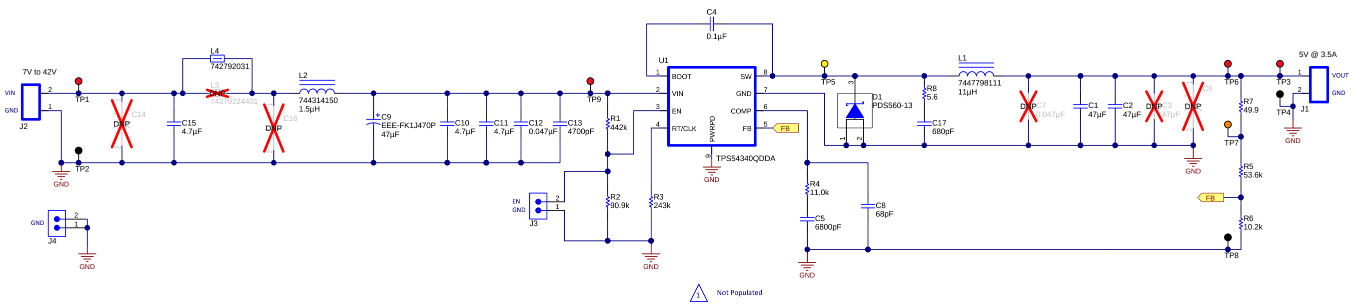


Figure 2. TPS54340-Q1EVM-593 Schematic

1.4 Modifications

These evaluation modules are designed to provide access to the features of the TPS54340-Q1. Some modifications can be made to this module. Component selection for modifications can be done with the aid of WEBENCH or the excel spreadsheet (SLVC452) located on the product page.

1.4.1 Output Voltage Set Point

To change the output voltage of the EVM, the value of resistor R5 (R_{HS}) should be changed while keeping R6 (R_{LS}) fixed. The output voltage can be adjusted to a minimum of the 0.8 V internal reference. The value of R5 for a specific output voltage can be calculated using Equation 1:

$$R_{HS} = R_{LS} \times \left(\frac{Vout - 0.8V}{0.8\ V} \right) \tag{1}$$

Table 3 lists the R5 values for some common output voltages assuming R6 = 10.2 kΩ. Note V_{IN} must be in a range to keep the on time greater than the minimum on-time. The values given in Table 3 are standard 1% values, not the exact value calculated using Equation 1.

Table 3. R5 Values for Common Output Voltages

Output Voltage (V)	R5 Value (kΩ)
1.8	12.7
2.5	21.5
3.3	31.6
5.0	53.6

Be aware, changing the output voltage can affect the loop response. It may be necessary to modify the compensation components. Please see the TPS54340-Q1 data sheet (SLVSBZ1) for details.

1.4.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R1 (R_{UVLO1}) and R2 (R_{UVLO2}). The EVM is set for a start voltage of 6.5 V and stop voltage of 5.0 V, using R1 = 442 kΩ and R2 = 90.9 kΩ. Use Equation 2 and Equation 3 to calculate the required resistor values for R1 and R2, respectively, for different start and stop voltages. The typical values of the constants in the two equations are as follows: I_{HYS} = 3.4 µA, V_{ENA} = 1.2 V, and I_1 = 1.2 µA.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \tag{2}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \tag{3}$$

2 Test Setup and Results

This section describes how to properly connect, set up, and use the EVM. The section also includes test results typical for the EVM covering efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start up, and shutdown.

2.1 I/O Connections

This EVM includes I/O connectors and test points as shown in Table 4. A power supply capable of supplying at least 3.5 A must be connected to J2 through a pair of 20-AWG wires. The load must be connected to J1 through a pair of 20-AWG wires. The maximum load-current capability must be 3.5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

Table 4. EVM Connectors and Test points

Reference Designator	Function
J1	V_{OUT}, 5.0 V at 3.5-A maximum
J2	V_{IN} (see Table 1 for V_{IN} range)
J3	EN jumper. Connect EN to ground to disable, open to enable.
J4	GND jumper for additional ground connections
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	Output voltage test point at V_{OUT} connector
TP4	GND test point at V_{OUT} connector
TP5	SW test point
TP6	V_{OUT} test point used for loop response measurements
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8	GND test point
TP9	V_{IN} test point at the TPS54340-Q1 VIN pin

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 1.1 A with V_{IN} = 12 V, and then decreases as the load current increases towards full load. Figure 3 shows the efficiency for the EVM. Figure 4 shows the light-load efficiency for the EVM using a semi-log scale. Measurements are taken at an ambient temperature of 25°C. The efficiency may be lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the internal MOSFET.

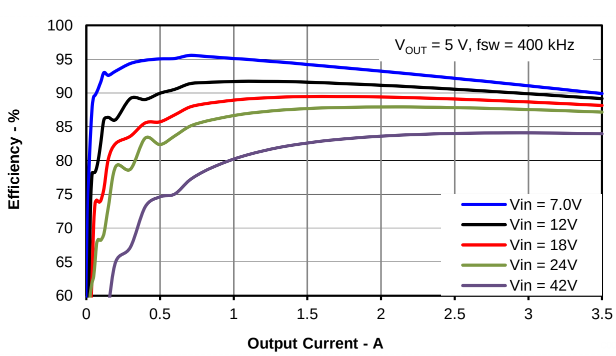


Figure 3. Efficiency versus Load Current

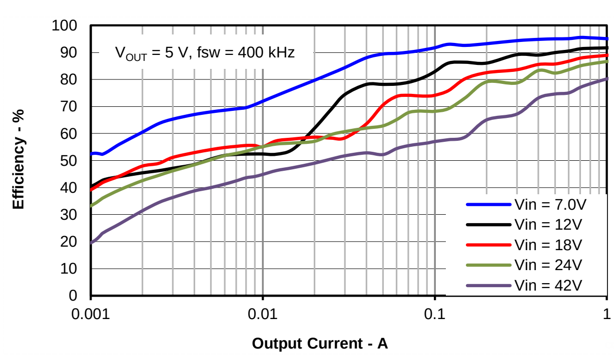


Figure 4. Light Load Efficiency

2.3 Output Voltage Regulation

The load regulation for the EVM is shown in Figure 5. The line regulation for the EVM is shown in Figure 6. Measurements are given for an ambient temperature of 25°C.

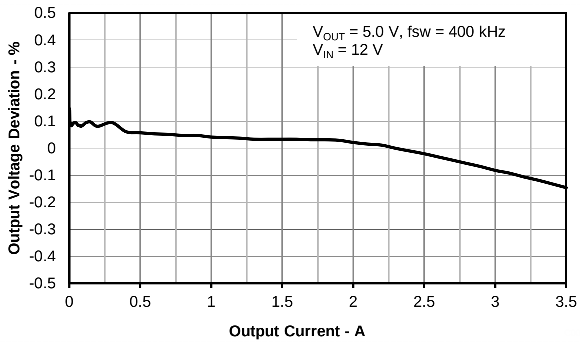


Figure 5. Regulation versus Output Current

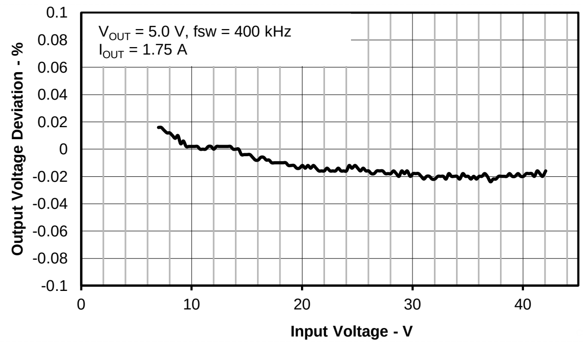
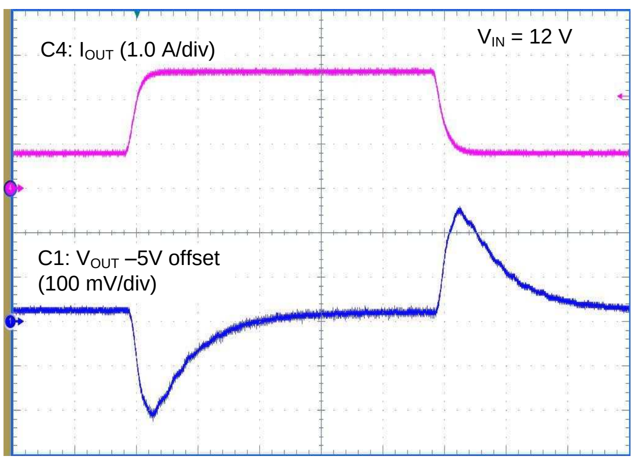


Figure 6. Regulation versus Input Voltage

2.4 Load Transients and Loop Response

The EVM response to load transients is shown in Figure 7. The current step is from 25% to 75% of the maximum rated load at 12-V input. The current step slew rate is 100 mA/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

The EVM loop-response characteristics are shown in Figure 8. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 3.5 A.



Time: 100 µs/div

Figure 7. Load Transient Response

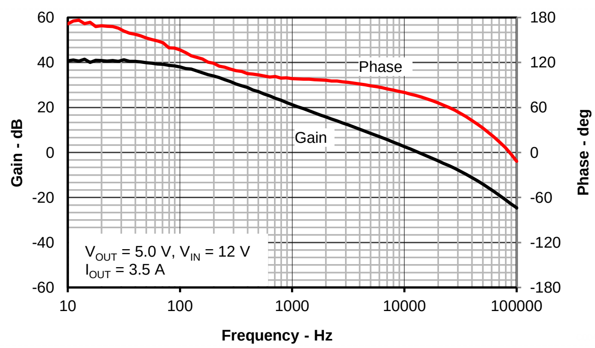


Figure 8. Loop Response

2.5 Line Transients

The EVM response to line transients is shown in Figure 9. The input voltage step is from 8.0 V to 40 V. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

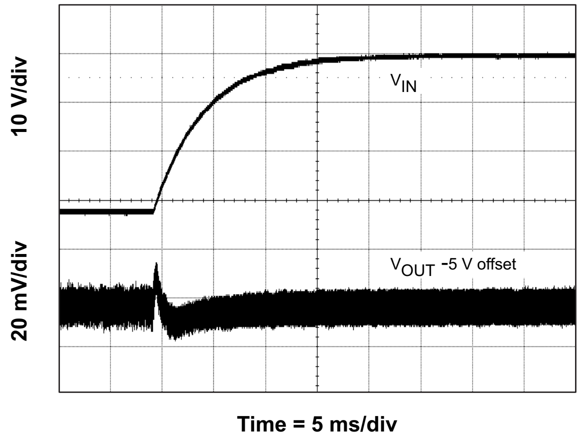


Figure 9. Line Transient Response

2.6 Input Voltage Ripple

The EVM CCM input voltage ripple is shown in Figure 10. The output current is the rated full load of 3.5 A and V_{IN} = 12 V. The voltage ripple is measured directly across the capacitors located at the VIN pin of the IC (C9-C13) and at the input to the board (C15) showing the attenuation of the input filter. The input voltage ripple measurements are taken with a 250-MHz bandwidth limit.

The DCM input voltage ripple is shown in Figure 11. The output current is 0.1 A and V_{IN} = 12 V.

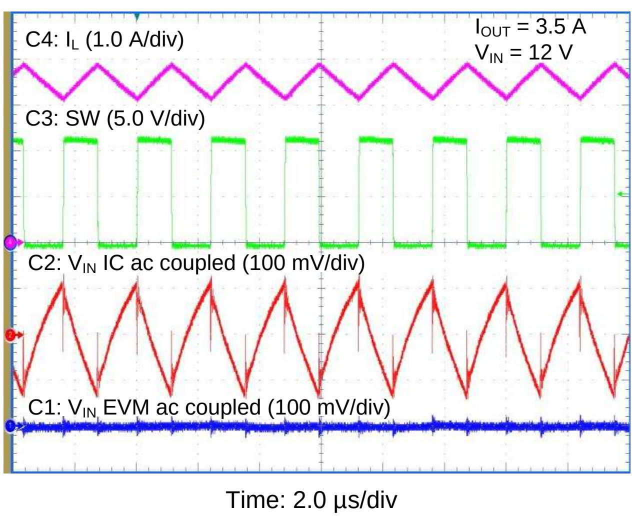


Figure 10. Input Voltage Ripple CCM

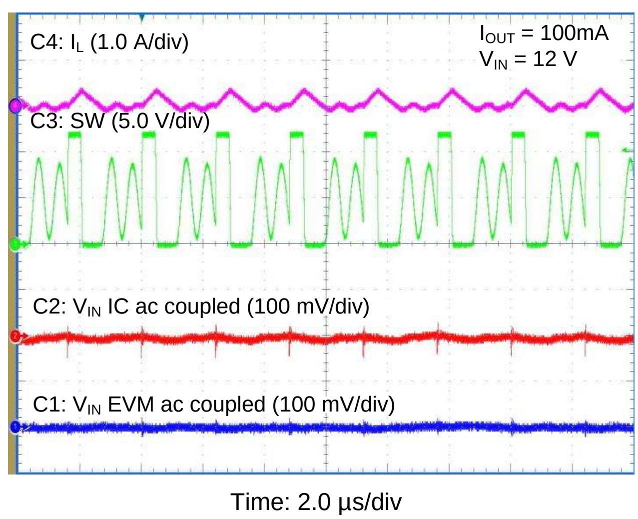


Figure 11. Input Voltage Ripple DCM

2.7 Output Voltage Ripple

The EVM CCM output voltage ripple is shown in Figure 12. The output current is the rated full load of 3.5 A and V_{IN} = 12 V. The voltage ripple is measured directly across the output capacitors.

The DCM output voltage ripple is shown in Figure 13. The output current is 0.1 A and V_{IN} = 12 V.

The Pulse Skip Eco-mode™ output voltage ripple is shown in Figure 14. There is no external load on the output and V_{IN} = 12 V.

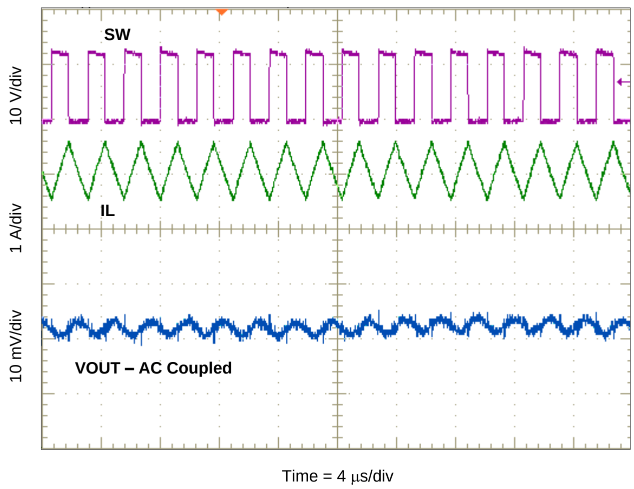


Figure 12. Output Voltage Ripple CCM

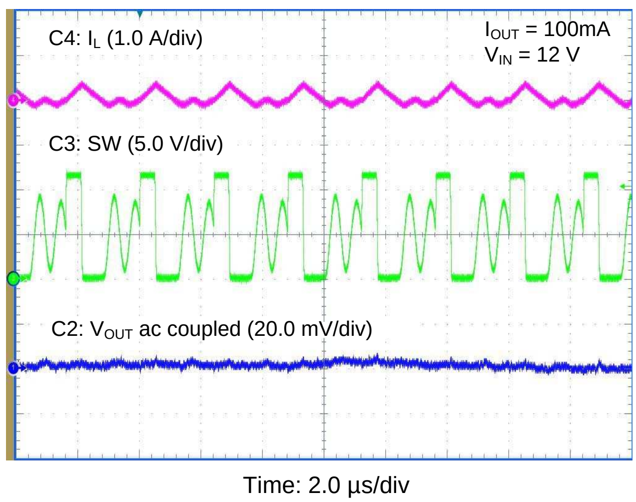


Figure 13. Output Voltage Ripple DCM

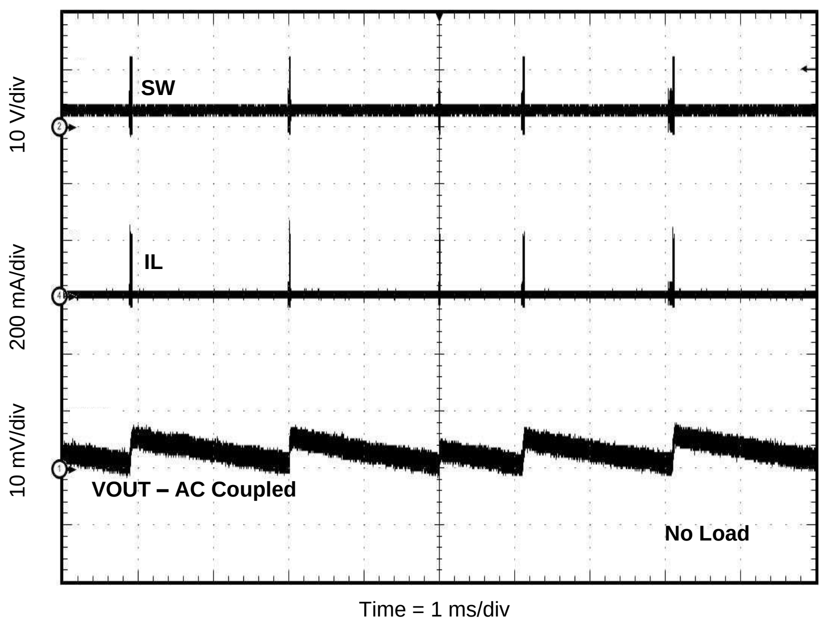


Figure 14. Output Voltage Ripple Eco-mode

2.8 Switching Waveform

This design uses a snubber to reduce ringing at the SW pin of the TPS54340-Q1, reducing emissions of the EVM. Figure 15 shows the ringing at the SW pin before the snubber is added. Figure 16 shows the performance with the snubber. The input voltage for these plots is 12 V with a 3.5-A resistive load.

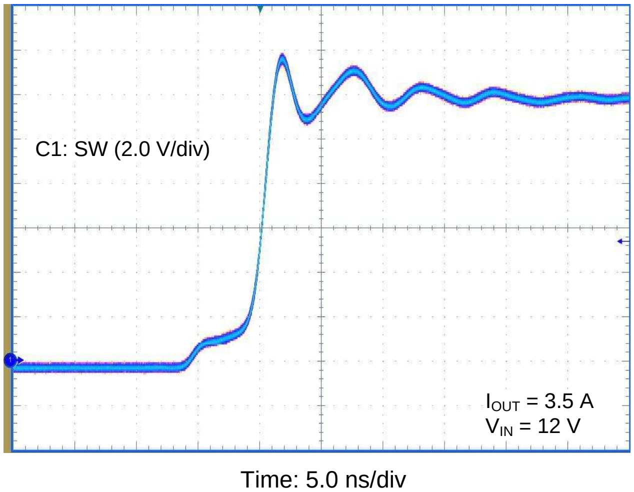


Figure 15. Switching Waveform Without Snubber

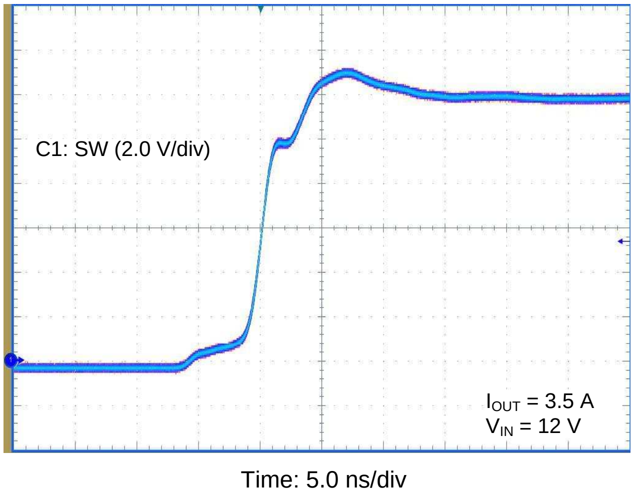


Figure 16. Switching Waveform With Snubber

2.9 Start Up

The start up waveforms are shown in Figure 17, Figure 18, and Figure 19. The input voltage for these plots is 12 V with a 3.5-A resistive load. In Figure 17 the top trace shows V_{IN}, the middle trace shows EN, and the bottom trace shows V_{OUT}. The input voltage is initially applied, and when the input reaches the undervoltage lockout threshold, the start up sequence begins and the output ramps up toward the set value of 5.0 V.

In Figure 18 the input voltage is initially applied with EN held low. When EN is released, the start up sequence begins and the output ramps up toward the set value of 5.0 V.

In Figure 19 the input voltage is initially applied with EN held low. An external voltage of 3.3 V is supplied to V_{OUT}. When EN is released, the start up sequence begins and the internal reference ramps up from 0 V with the internal soft-start. When the internal reference reaches the FB voltage the output begins ramping toward the set value of 5.0 V.

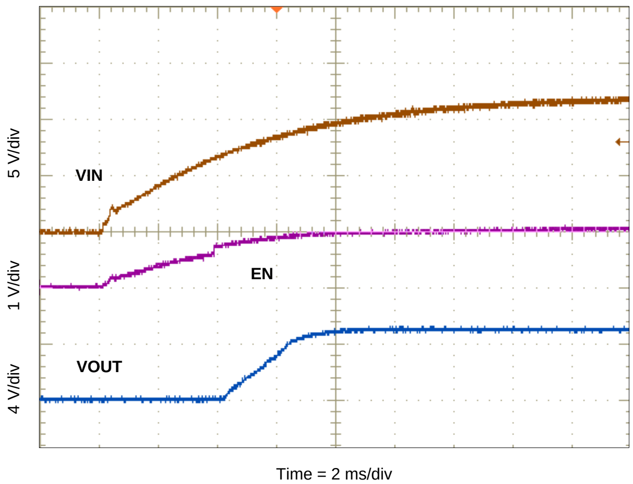


Figure 17. Start Up With V_{IN} Ramping Up

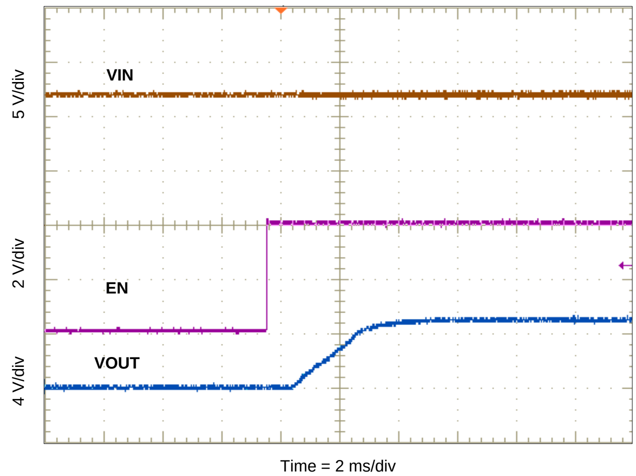


Figure 18. Start Up Using EN

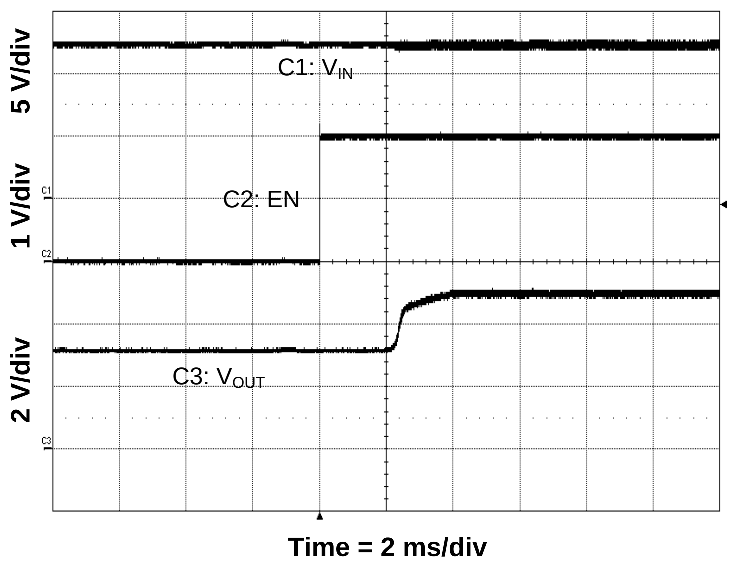
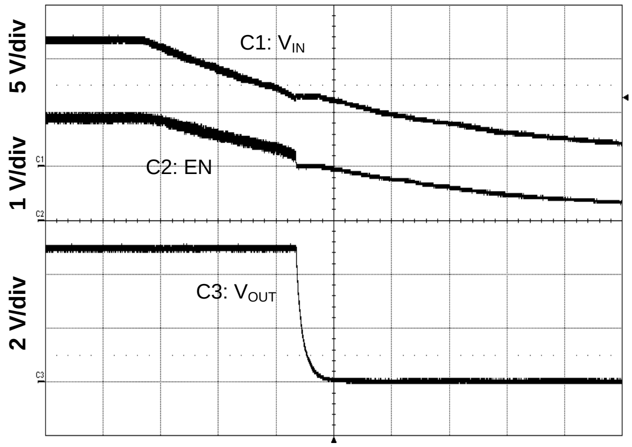


Figure 19. Prebias Start Up Using EN

2.10 Shutdown

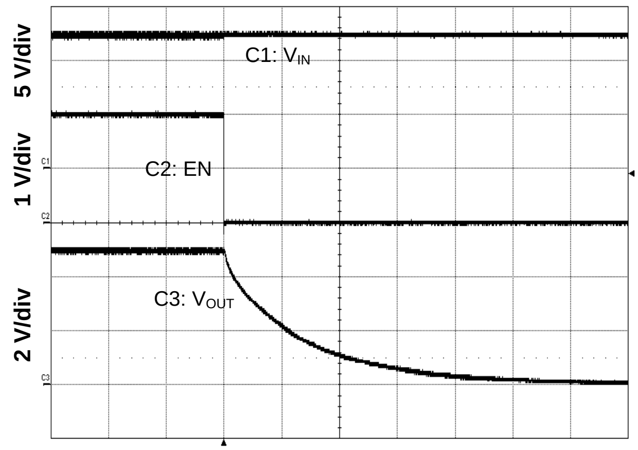
The shutdown waveforms are shown in Figure 20 and Figure 21. The input voltage for these plots is 12 V with a 3.5-A resistive load. The top trace shows V_{IN}, the middle trace shows EN, and the bottom trace shows V_{OUT}. In Figure 20 the input voltage is removed, and when the input falls below the undervoltage lockout threshold, the TPS54340-Q1 shuts down and the output falls to ground.

In Figure 21, the input voltage is held at 12 V, and EN is shorted to ground. When EN is grounded, the TPS54340-Q1 is disabled, and the output voltage discharges to ground.



Time = 1 ms/div

Figure 20. Shutdown With V_{IN} Ramping Down

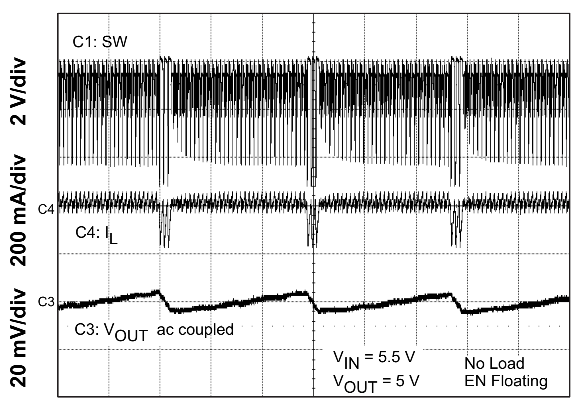


Time = 200 µs/div

Figure 21. Shutdown Using EN

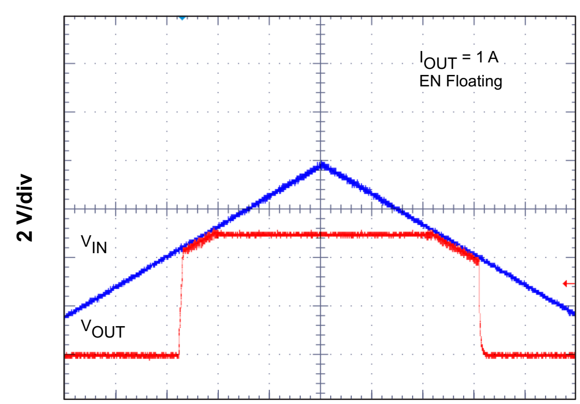
2.11 Low Dropout Operation

For improved low dropout operation, the TPS54340-Q1 includes a small integrated low-side MOSFET to pull SW to GND when the BOOT to SW voltage drops below 2.1 V. This recharges the BOOT capacitor for driving the high-side MOSFET. Figure 22 shows the steady state operation and Figure 23 shows the start up and shutdown in a low dropout condition. Both measurements are taken with a 5-V output.



Time = 20 µs/div

Figure 22. Low Dropout Operation



Time = 40 µs/div

Figure 23. Low Dropout Start Up and Shutdown

3 Board Layout

This section provides a description of the EVM, board layout, and layer illustrations.

3.1 Layout

The board layout for the EVM is shown in Figure 24 through Figure 27. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and SW. Also on the top layer are connections for the remaining pins of the TPS54340-Q1 and a large area filled with ground. The bottom layer contains ground and a signal route for the bootstrap capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54340-Q1 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane. Multiple vias are also placed near the Schottky diode (D1) to provide a nearby thermal path to improve its thermal performance.

The input decoupling capacitors (C10–C13), bootstrap capacitor (C4), and frequency set resistor (R3) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC, especially the bottom resistor (R6). The voltage divider network ties to the output voltage at the point of regulation. For the TPS54340-Q1EVM-593, an additional input bulk capacitor may be required (C14), depending on the EVM connection to the input supply.

Layout considerations to reduce emissions are as follows. The bootstrap capacitor (C4) is placed on the bottom side of the board so the Schottky diode (D1) can be placed directly next to the IC. The diode should be as close as possible to the SW pin and GND of the input decoupling capacitors. The smaller sized input decoupling capacitors (C12 and C13) are located closest to the IC to reduce any board parasitics to improve their effectiveness of filtering high frequency noise. The snubber (R8 and C17) is located directly next to the diode to improve its performance. Lastly, the SW copper area is kept as small as possible because it is a high dv/dt node which can radiate noise.

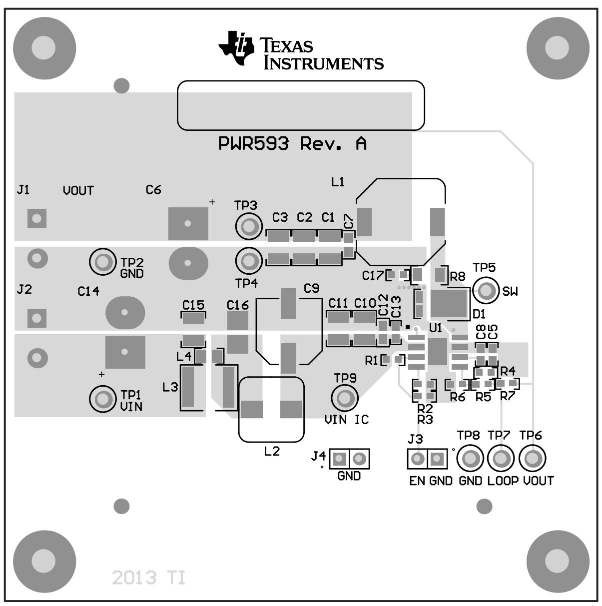


Figure 24. TPS54340-Q1EVM-593 Top Assembly and Silkscreen

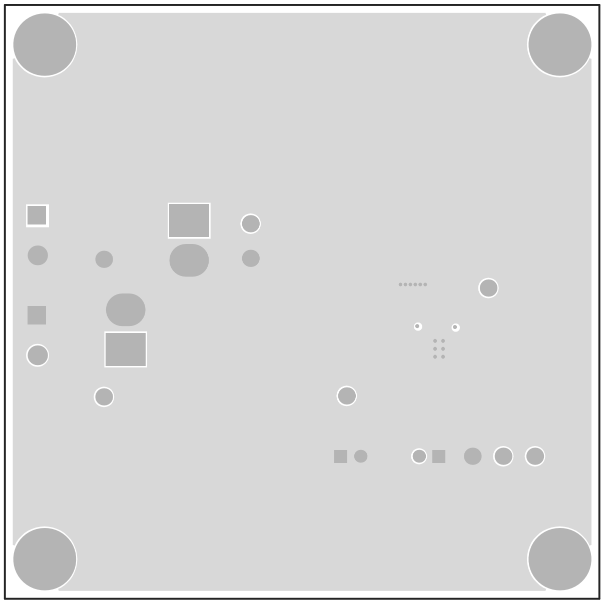


Figure 25. TPS54340-Q1EVM-593 Layer 2 Layout

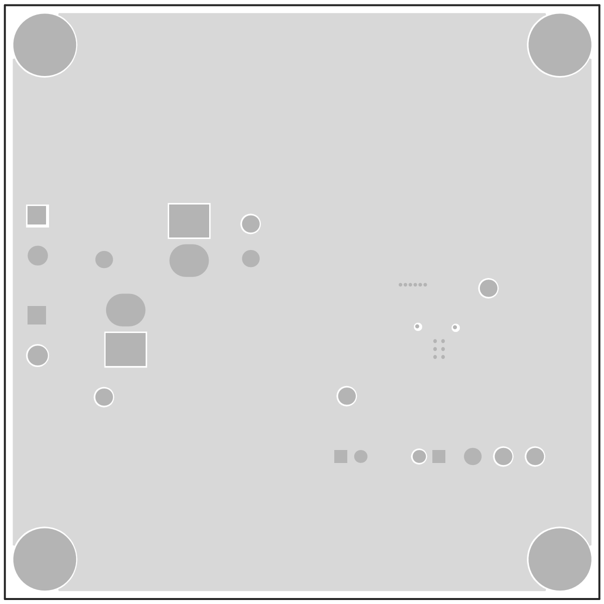


Figure 26. TPS54340-Q1EVM-593 Layer 3 Layout

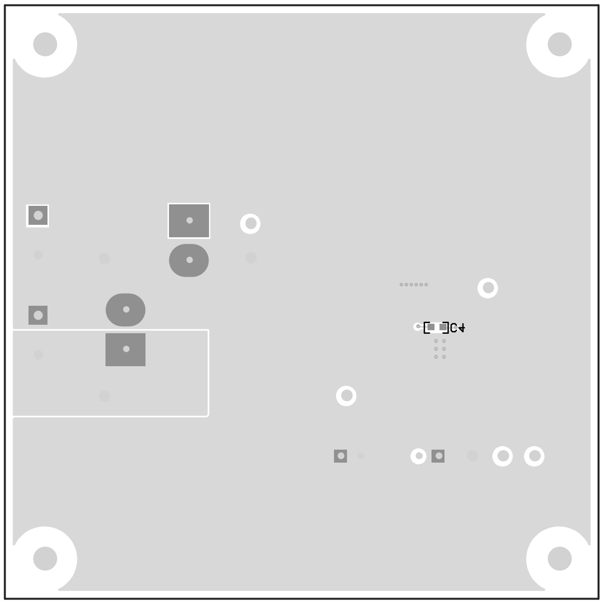


Figure 27. TPS54340-Q1EVM-593 Bottom-Side Assembly and Silkscreen (Viewed From Top)

3.2 Estimated Circuit Area

The estimated printed-circuit-board area in this design by simply boxing in the components on the top layer is 1.43 in^2 (923 mm^2). This area does not include test points or connectors. This design uses 0603 components for easy modifications. The area can be reduced by using smaller-sized components.

4 Bill of Materials

Table 5 presents the bill of materials for the EVM.

Table 5. TPS54340-Q1EVM-593 Bill of Materials

Designator	Quantity	Value	Description	Package	Part Number	Manufacturer
C1, C2	2	47uF	CAP, CERM, 47uF, 16V, +/-20%, X5R, 1210	1210	GRM32ER61C476ME15L	MuRata
C4	1	0.1uF	CAP, CERM, 0.1uF, 10V, +/-10%, X7R, 0603	0603	STD	STD
C5	1	6800pF	CAP, CERM, 6800pF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C8	1	68pF	CAP, CERM, 68pF, 50V, +/-5%, C0G/NP0, 0603	0603	STD	STD
C9	1	47uF	CAP, AL, 47uF, 63V, +/-20%, 0.65 ohm, SMD	SMT Radial F	EEE-FK1J470P	Panasonic
C10, C11, C15	3	4.7uF	CAP, CERM, 4.7uF, 50V, +/-10%, X7R, 1210	1210	STD	STD
C12	1	0.047uF	CAP, CERM, 0.047uF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C13	1	4700pF	CAP, CERM, 4700pF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C17	1	680pF	CAP, CERM, 680pF, 50V, +/-10%, X7R, 0603	0603	STD	STD
D1	1	0.52V	Diode, Schottky, 60V, 5A, PowerDI5	PowerDI5	PDS560-13	Diodes Inc.
J1, J2	2	ED120/2DS	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35 inch	ED120/2DS	OST
J3, J4	2		Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	TSW-102-07-G-S	TSW-102-07-G-S	Samtec, Inc.
L1	1	11uH	Inductor, Shielded Flat Iron, Ferrite, 11uH, 5.3A, 0.014 ohm, SMD	WE-PDF	7447798111	Wurth Elektronik eiSos
L2	1	1.5uH	Inductor, Shielded Drum Core, Superflux, 1.5uH, 11A, 0.0046 ohm, SMD	WE-HC3	744314150	Wurth Elektronik eiSos
L4	1	300 ohm	3000mA Ferrite Bead, 300 ohm @ 100MHz, SMD	0805	742792031	Wurth Elektronik eiSos
R1	1	442k	RES, 442k ohm, 1%, 0.1W, 0603	0603	STD	STD
R2	1	90.9k	RES, 90.9k ohm, 1%, 0.1W, 0603	0603	STD	STD
R3	1	243k	RES, 243k ohm, 1%, 0.1W, 0603	0603	STD	STD
R4	1	11.0k	RES, 11.0k ohm, 1%, 0.1W, 0603	0603	STD	STD
R5	1	53.6k	RES, 53.6k ohm, 1%, 0.1W, 0603	0603	STD	STD
R6	1	10.2k	RES, 10.2k ohm, 1%, 0.1W, 0603	0603	STD	STD
R7	1	49.9	RES, 49.9 ohm, 1%, 0.1W, 0603	0603	STD	STD
R8	1	5.6	RES, 5.6 ohm, 5%, 0.25W, 1206	1206	STD	STD
SH-J3	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP3, TP6, TP9	4	Red	Test Point, TH, Multipurpose, Red	Keystone5010	5010	Keystone
TP2, TP4, TP8	3	Black	Test Point, TH, Multipurpose, Black	Keystone5011	5011	Keystone
TP5	1	Yellow	Test Point, TH Multipurpose, Yellow	Keystone5014	5014	Keystone
TP7	1	Orange	Test Point, TH, Multipurpose, Orange	Keystone5013	5013	Keystone
U1	1	TPS54340QDDA	IC, 42V, 3.5A, Low Iq, Current Mode, Non-Synchronous Monolithic Buck, AEC-Q100 Qualified	SON	TPS54340QDDA	TI
C3	0	47uF	CAP, CERM, 47uF, 16V, +/-20%, X5R, 1210	1210	GRM32ER61C476ME15L	MuRata
C6, C14	0	Open	Capacitor, Aluminum, vvV, 20%	Multi sizes	Engineering Only	
C7	0	0.047uF	CAP, CERM, 0.047uF, 50V, +/-10%, X7R, 0603	0603	STD	STD
C16	0	Open	Capacitor, Ceramic, 500V, X7R, ±10 %	Multi sizes	Engineering Only	
L3	0	400 ohm	4500mA Ferrite Bead, 400 ohm @ 100MHz, SMD	2220	74279224401	Wurth Elektronik eiSos

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