

## 1 Introduction

PMP9013A is an IEEE802.3at, Type 2 compliant powered device. The EVM is a low cost self driven synchronous flyback designed for 22.5W output power at 5V/4.5A from either an adapter (21.6V – 57VDC) or power over Ethernet (PoE) input.

## 2 Configurable features

### 1.1 Features

- Good efficiency, self driven, synchronous flyback design.
- Gigabit Ethernet pass through interface
- 21.6V and 57V adapter input capability
- IEEE 802.3at type-2 hardware classification with secondary side status flag (T2P)
- 5V @ 4.5A DC output.
- Ultra-Low Power Sleep Modes

### 1.2 Applications

- IEEE 802.3at-compliant devices
- Video and VoIP telephones
- Multiband access points
- Security cameras
- Pico-base stations

### 3 Electrical specifications

#### TPS23751EVM-104 Electrical and Performance Specifications

Parameter	Condition	Min	Typ	Max	Units	
<b>Power Interface</b>						
Input Voltage	Applied to the power pins of connectors J1 or J3	0	-	57	Volts	
Operating Voltage	After start up.	30	-	57		
Input UVLO, POE input J1	Rising input voltage	-	-	40		
	Falling input voltage	30	-	-		
Input UVLO, adapter J3	Rising input voltage		18.7			
Detection voltage	@ device terminals	1.4	-	10.1		
Classification voltage	@ device terminals	11.9	-	23.0		
Classification current	Rclass = 63.4 ohms	38	-	42	mA	
Inrush current-limit		100	-	180		
Operating current-limit		850	-	1200		
<b>DC/DC Converter</b>						
Output Voltage	$21.6V \leq V_{in} \leq 57V$ , $I_{LOAD} \leq I_{LOAD} (max)$	5V output	4.75	5.00	5.25	Volts
Output Current	$21.6V \leq V_{in} \leq 57V$	5V output	-	-	4.5	Amps
Output ripple voltage, pk-to-pk	$V_{in} = 44V$ , $I_{LOAD} = 4.5A$	5V output	-	30	-	mV
Efficiency, dc-dc converter	$V_{in} = 48V$ , $I_{LOAD} = 4.5A$	5V output	-	91	-	%
Efficiency, end-to-end	$V_{in} = 48V$ , $I_{LOAD} = 4.5A$	5V output	-	88	-	%
Switching frequency			225	-	275	kHz

## 4 Efficiency

Efficiency is shown below with 48V applied to the adapter input connector (J3). Adapter efficiency measured from the input J3 to output connector, J6 is represented as Nadp. DC-DC converter only efficiency measured from the input (VDD-PWRGND test points, TP6/TP19) to output connector, J6 is represented as Ncnvrtr.

Vin	Vcnvrtr	Iin	Vout	Iout	Nadp	Ncnvrtr
48.00	47.64	0.025	4.970	0.000	0.00	0.00
47.98	47.58	0.079	4.970	0.506	66.77	67.33
47.97	47.54	0.131	4.970	1.005	79.48	80.20
47.95	47.46	0.239	4.970	2.004	86.91	87.81
47.92	47.39	0.348	4.960	2.999	89.20	90.20
47.89	47.33	0.461	4.960	4.000	89.87	90.93
47.88	47.29	0.519	4.960	4.500	89.82	90.94

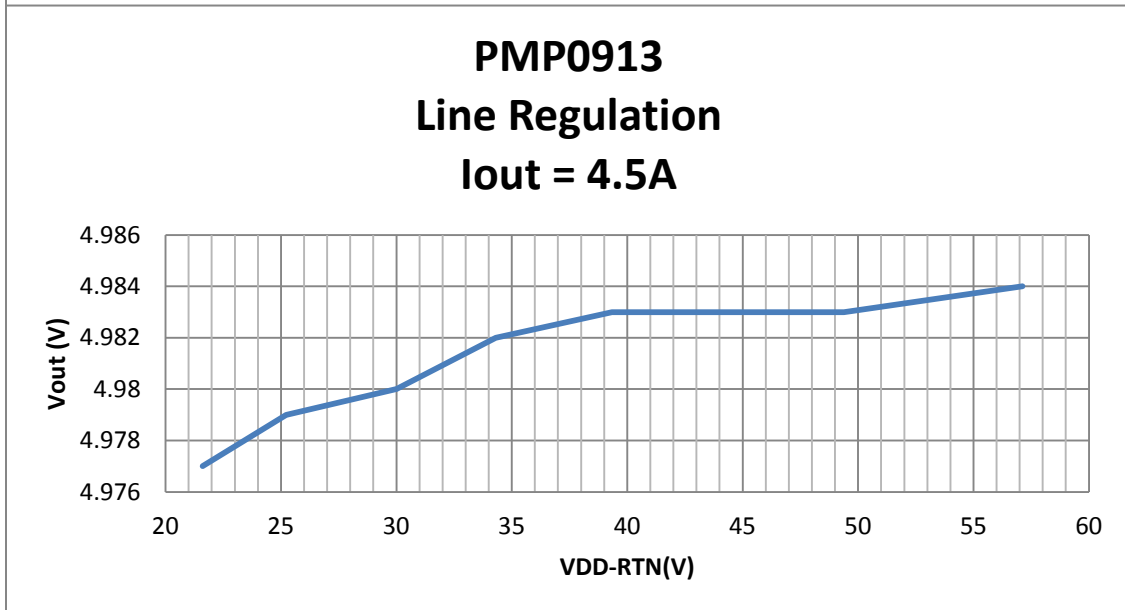
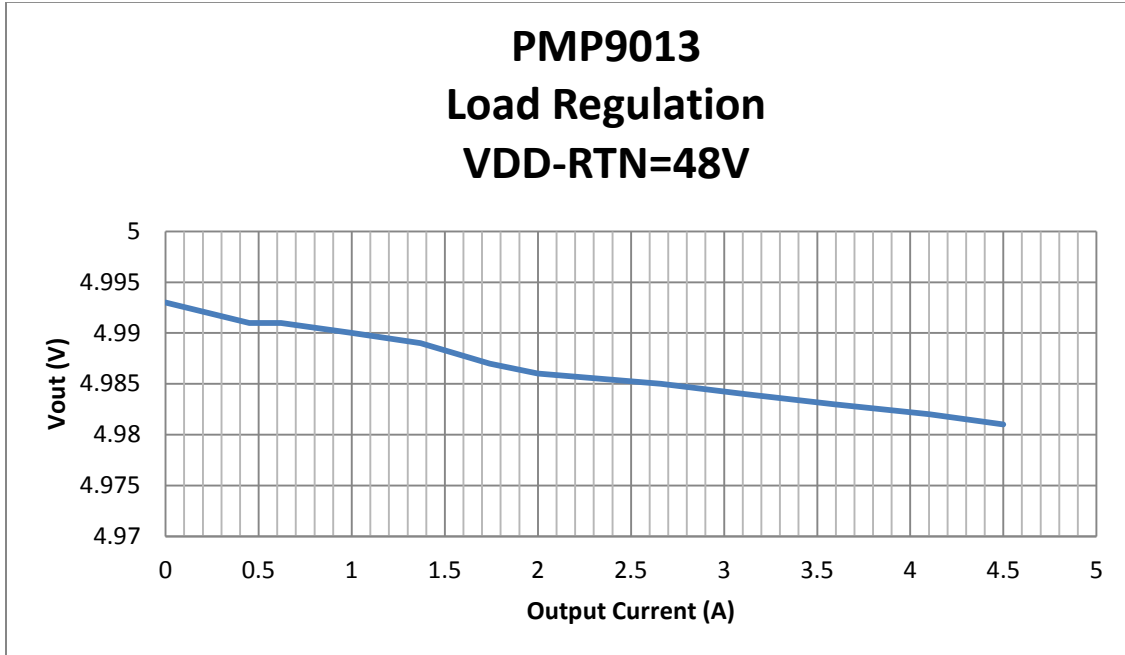
## 5 End-end efficiency

End to end efficiency is shown below with 48V input from the J1 ethernet connector to output connector, J6 is represented as Npoe.

Vin	Iin	Vout	Iout	Npoe
48.00	0.025	4.970	0.000	0.00
47.98	0.079	4.970	0.506	66.77
47.97	0.132	4.970	1.005	78.88
47.95	0.242	4.970	2.004	86.01
47.92	0.353	4.960	2.999	87.94
47.89	0.470	4.960	4.000	88.24
47.88	0.529	4.960	4.500	88.12

## 6 Load Regulation

PMP9013A load regulation is less than +/-10mV.

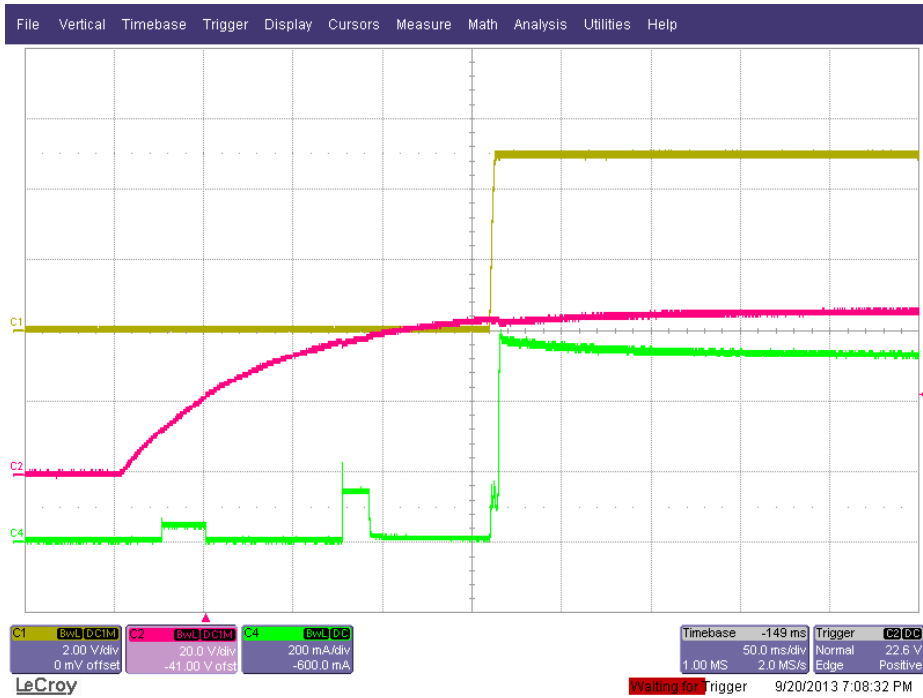


## 7 Start up

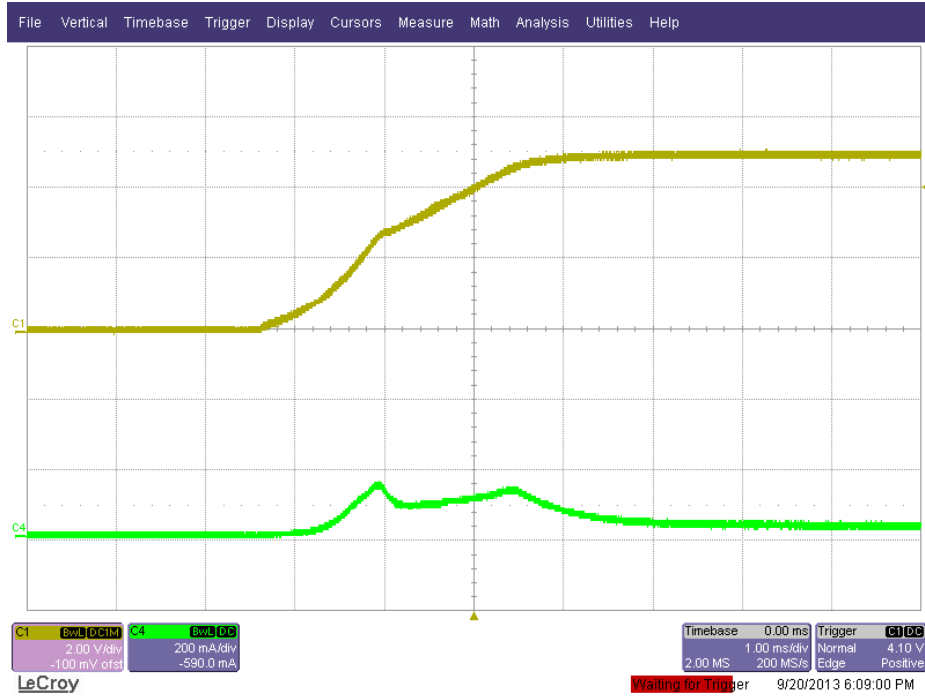
The scope plot below shows the 5V output voltage startup waveform after the application of 48Vdc at J1 (Ethernet connector. The output was loaded to 0A.



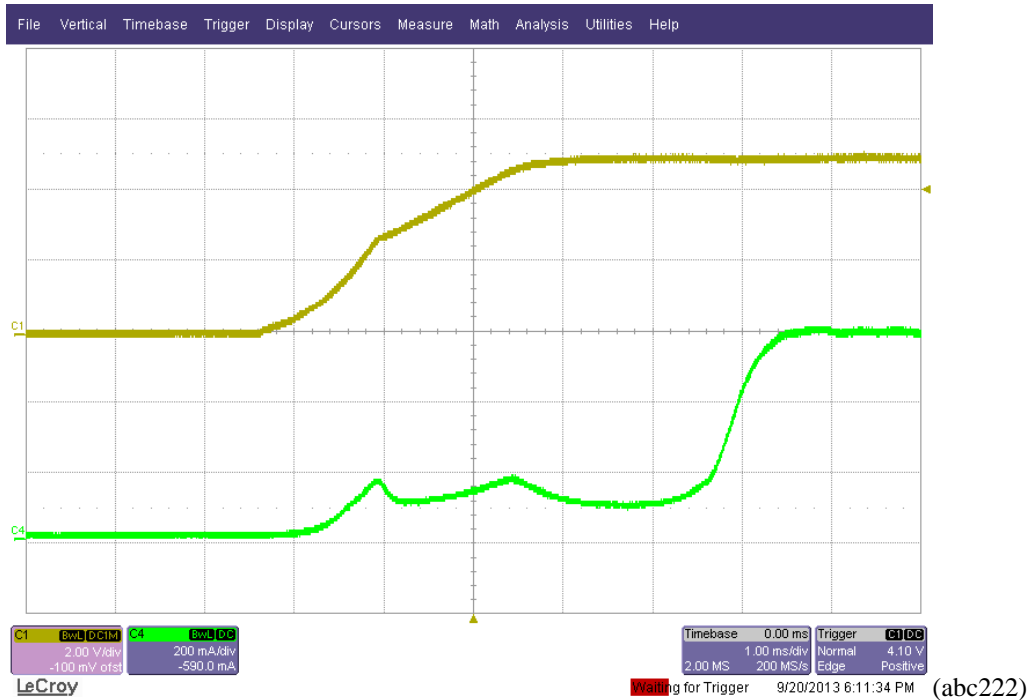
The scope plot below shows the 5V output voltage startup waveform after the application of 48Vdc at J1 (Ethernet connector. The output was loaded to 4.5A using an electronic load in CR mode.



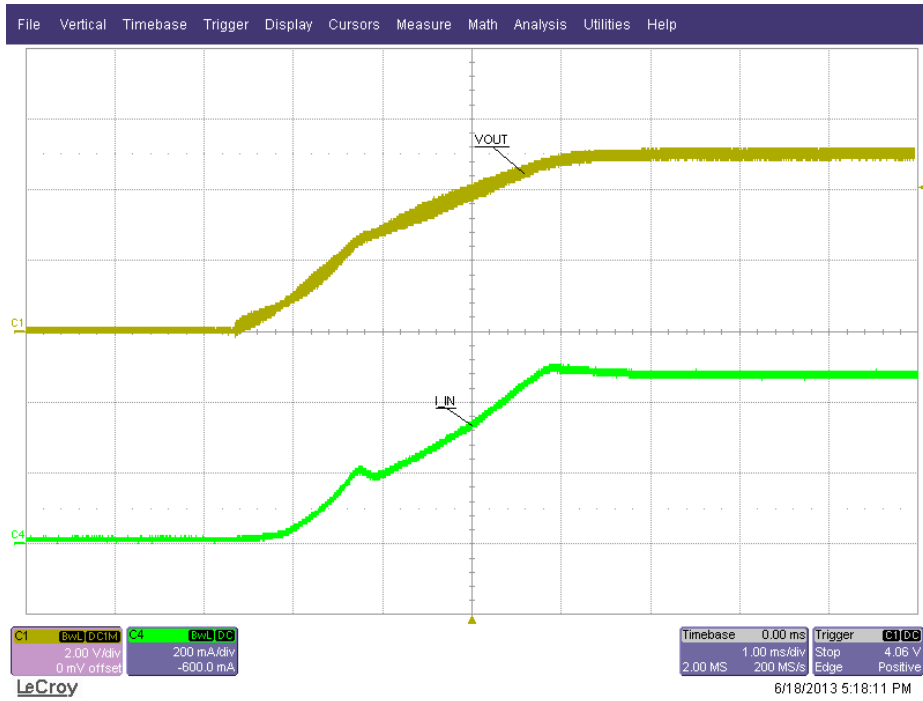
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The scope plot below shows the 5V output voltage startup waveform after the application of 48Vdc at J1 (Ethernet connector. The output was loaded to ~4A using a decade box.



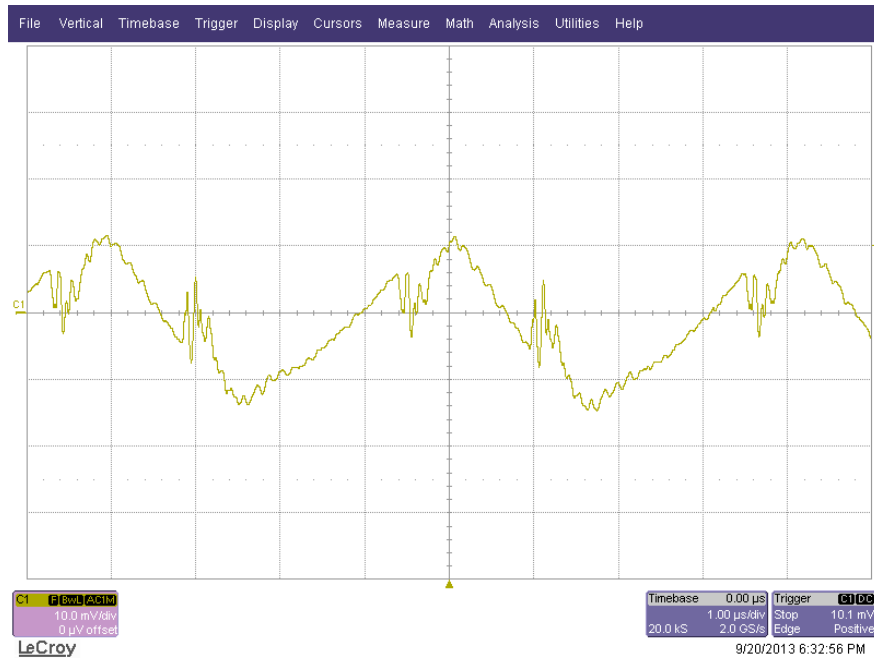
## 8 Switch Node Waveforms

The scope plot below shows the waveforms on the drain of the secondary side FET (CH1) and primary side FET (CH2). The output is loaded at 4.0A.  $V_{in} = 48V_{dc}$  at J1



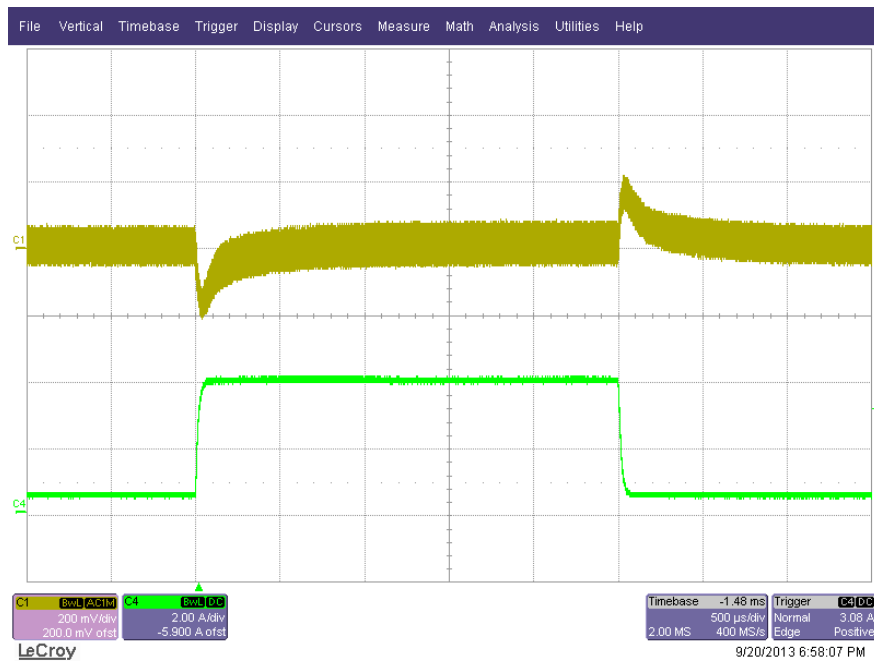
## 9 Output Ripple Voltage

The 5V output ripple voltage is shown in the scope plot below (J6 connector across pins w/tip and ring). The scope plot was taken with the output loaded to 4.5A.  $V_{in} = 48V_{dc}$  at J1.



## 10 Load Transients

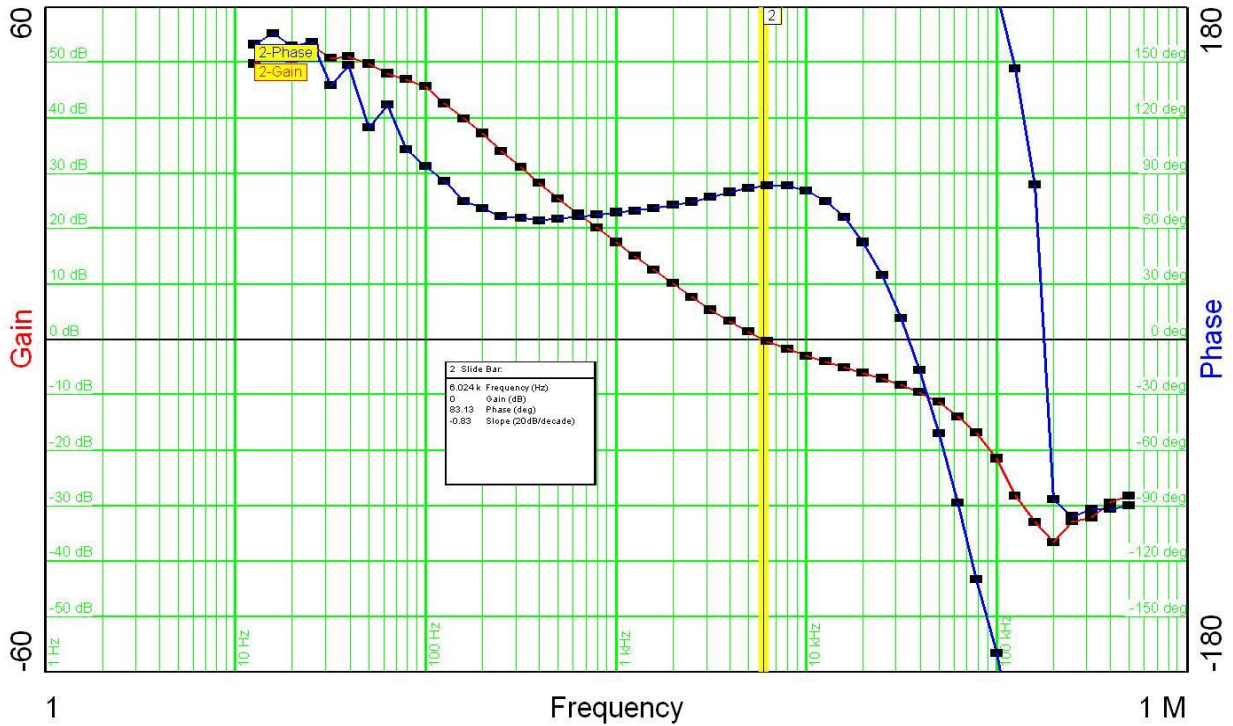
The scope plot below shows the 5V output voltage (at J6) when the load current is pulsed from 0.5 to 4.0A at a 300A/ms slew rate.  $V_{in} = 48V_{dc}$  at J1.





### 11 Control Loop Gain / Stability

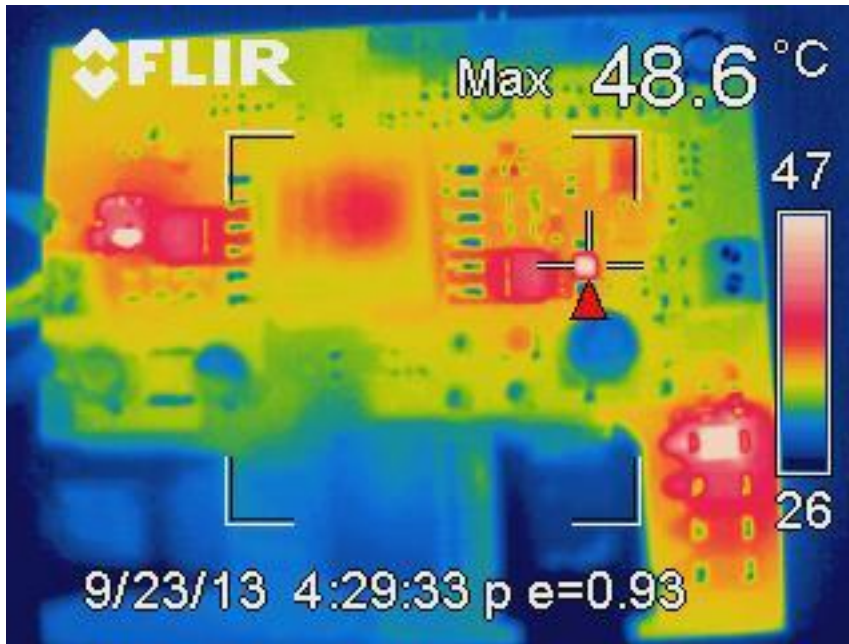
The figure below shows the closed loop response of the PMP9013 at 48V input and a 4.5A electronic load.



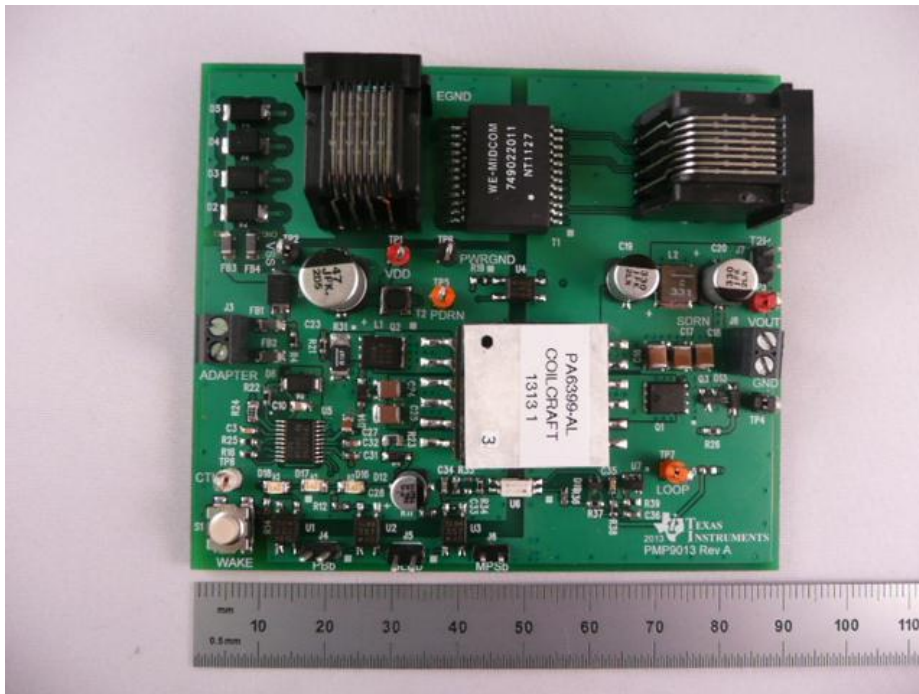
The table below shows the loop gain and phase margin.

Input voltage	48VDC	
Gain/Phase	Crossover	Phase Margin
PMP9013A	6.0kHz	83°

The image below shows the board with a 48VDC input. The ambient temperature was 25C with no forced air flow. The output was loaded with 4.5A



The below image shows the PMP9013 board and relative solution size.



The table below shows the results of the Sifos Technologies PoE Powered Device Analyzer using a 1A load.

Test Parameter	Description	Analyzer Results	Pass/Fail
Rdet	Detection resistance (2.7 to 10.1 Volt band)	24.62k ohms	P
Cdet	Detection capacitance (2.7 to 10.1 Volt band)	0.113uF	P
Iclass	Classification signature current (15 – 20 Volt band)	39.5mA	P
Class	PD Class determined from classification	4	P
Type	PD Type determined from classification	2	-
Von	Voltage at which PD draws load current	39.1V	P
Voff	Voltage at which PD stops load current	33.8V	P
Einr	Capacitive charging energy (watt-sec) over worst 20msec sub-interval of Inrush interval – a failure indicates an linrush_pd violation while a pass indicates very low inrush interoperability risk	0.123Ws	P
<b>Single-Event Classification</b>			
Power	Average PD power draw following the 50msec inrush interval	5.76W	P
Peak	Maximum PD transient load following the 50msec inrush interval	5.84W	P
Imax	Maximum transient load current sampled following the 50msec inrush interval	122.1mA	-
Imin	Minimum load current sampled after power-up. (Note: PD's meeting DC MPS signature criteria described in IEEE 802.3at paragraph 33.3.8 will report 10mA or higher.)	119.1mA	P
Iavg	Average load current following the 50msec inrush interval	120.2mA	-
<b>Two-Event Classification</b>			
Imark	Class pulse discharge current measured between class pulses	0.84mA	P
Power	Average PD power draw following the 50msec inrush interval	5.89W	P
Peak	Maximum PD transient load following the 50msec inrush interval	6W	P
Init	Power load measured between end of inrush interval (50msec) and Tdelay (80msec) (see IEEE 802.3at paragraph 33.3.7.3)	0.13W	P
Imax	Maximum transient load current sampled following the 50msec inrush interval	111.1mA	-
Imin	Minimum load current sampled after power-up. (Note: PD's meeting DC MPS signature criteria described in IEEE 802.3at paragraph 33.3.8 will report 10mA or higher.)	108.2mA	P
Iavg	Average load current following the 50msec inrush interval	109.3mA	-

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